Dual 12-/10-/8-Bit PWM to V_{OUT} DACs with 10ppm/°C Reference

FEATURES

- No Latency PWM-to-Voltage Conversion
- Voltage Output Updates and Settles within 8µs
- 100kHz to 30Hz PWM Input Frequency
- ±2.5LSB Max INL; ±1LSB Max DNL (LTC2644-12)
- Guaranteed Monotonic
- Pin-Selectable Internal or External Reference
- 2.7V to 5.5V Supply Range
- 1.71V to 5.5V Input Voltage Range
- Low Power: 2.7mA at 3V, <1µA Power-Down
- Guaranteed Operation from –40°C to 125°C
- 12-Lead MSOP Package

APPLICATIONS

- Digital Calibration
- Trimming and Adjustment
- Level Setting
- Process Control and Industrial Automation
- Instrumentation
- Automotive

DESCRIPTION

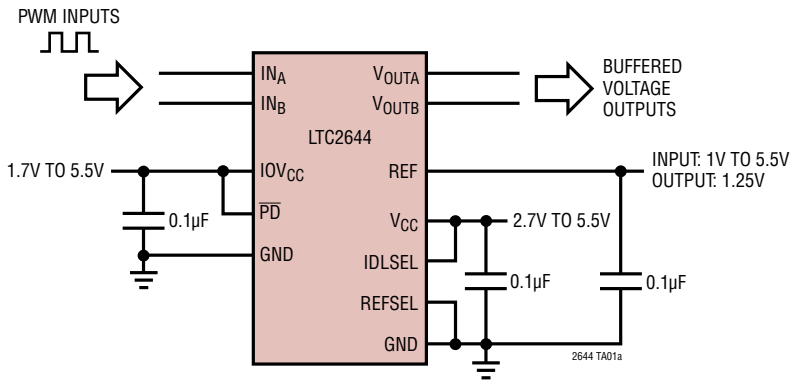
The LTC®2644 is a family of dual 12-, 10-, and 8-bit PWM-to-voltage output DACs with an integrated high accuracy, low drift, 10ppm/°C reference in a 12-lead MSOP package. It has rail-to-rail output buffers and is guaranteed monotonic.

The LTC2644 measures the period and pulse width of the PWM input signals and updates the voltage output DACs after each corresponding PWM input rising edge. The DAC outputs update and settle to 12-bit accuracy within 8µs typically and are capable of sourcing and sinking up to 5mA (3V) or 10mA (5V), eliminating voltage ripple and replacing slow analog filters and buffer amplifiers.

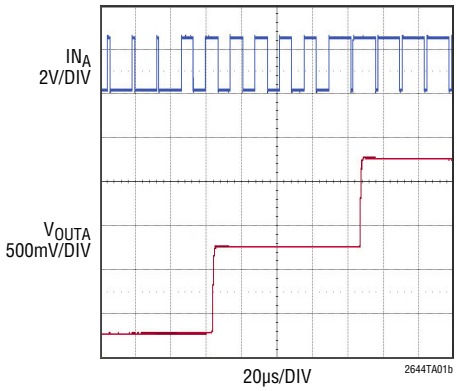
The LTC2644 has a full-scale output of 2.5V using the 10ppm/°C internal reference. It can operate with an external reference, which sets the full-scale output equal to the external reference voltage. Each DAC enters a pin-selectable idle state when the PWM input is held unchanged for more than 60ms. The part operates from a single 2.7V to 5.5V supply and supports PWM input voltages from 1.71V to 5.5V.

TYPICAL APPLICATION

2-Channel PWM to Voltage Output DAC



PWM Input to DAC Output

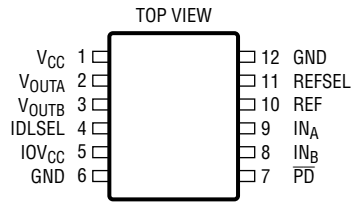


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltages (V_{CC}, IOV_{CC}) ..... –0.3V to 6V
IN_A, IN_B ..... –0.3V to 6V
IDLSEL, $\overline{PD}$, REFSEL ..... –0.3V to 6V
V_{OUTA}, V_{OUTB} ..... –0.3V to Min (V_{CC} + 0.3V, 6V)
REF ..... –0.3V to Min (V_{CC} + 0.3V, 6V)
Operating Temperature Range
LTC2644C ..... 0°C to 70°C
LTC2644I ..... –40°C to 85°C
LTC2644H ..... –40°C to 125°C
Maximum Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

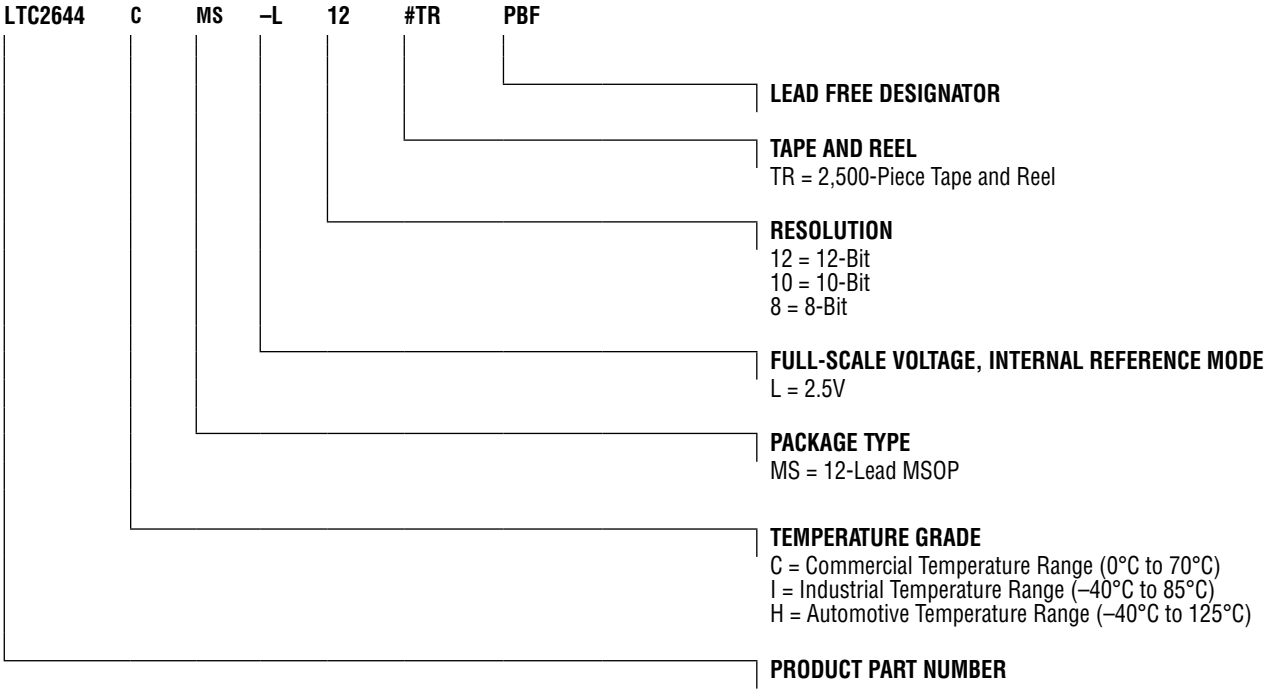
PIN CONFIGURATION



MS PACKAGE
12-LEAD PLASTIC MSOP

(4mm × 4.9mm)
T_{JMAX} = 150°C, θ_{JA} = 135°C/W

ORDER INFORMATION



Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

PRODUCT SELECTION GUIDE

PART NUMBER	PART MARKING*	RESOLUTION	CHANNELS	VFS WITH INTERNAL REFERENCE	MAXIMUM INL	PACKAGE DESCRIPTION
LTC2644-L12	644L12	12-Bit	2	2.5V	±2.5LSB	12-Lead Plastic MSOP
LTC2644-L10	644L10	10-Bit	2	2.5V	±1LSB	12-Lead Plastic MSOP
LTC2644-L8	2644L8	8-Bit	2	2.5V	±0.5LSB	12-Lead Plastic MSOP

*Temperature grades are identified by a label on the shipping container.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V to 5.5V, V_{OUT} unloaded unless otherwise specified.

LTC2644-L12/-L10/-L8 (V_{FS} = 2.5V)

SYMBOL	PARAMETER	CONDITIONS		LTC2644-L8 MIN	LTC2644-L8 TYP	LTC2644-L8 MAX	LTC2644-L10 MIN	LTC2644-L10 TYP	LTC2644-L10 MAX	LTC2644-L12 MIN	LTC2644-L12 TYP	LTC2644-L12 MAX	UNITS
DC Performance													
	Resolution		●	8			10			12			Bits
	Monotonicity	V_{CC} = 3V, Internal Ref. (Note 3)	●	8			10			12			Bits
DNL	Differential Nonlinearity	V_{CC} = 3V, Internal Ref. (Note 3)	●			±0.5			±0.5			±1	LSB
INL	Integral Nonlinearity	V_{CC} = 3V, Internal Ref. (Note 3)	●		±0.05	±0.5		±0.2	±1		±1	±2.5	LSB
ZSE	Zero-Scale Error	V_{CC} = 3V, Internal Ref., Code = 0	●		0.5	5		0.5	5		0.5	5	mV
V_{OS}	Offset Error	V_{CC} = 3V, Internal Ref. (Note 4)	●		±0.5	±5		±0.5	±5		±0.5	±5	mV
V_{OSTC}	V_{OS} Temperature Coefficient	V_{CC} = 3V, Internal Ref. (Note 9)			±10			±10			±10		µV/°C
GE	Gain Error	V_{CC} = 3V, Internal Ref.	●		±0.2	±0.8		±0.2	±0.8		±0.2	±0.8	%FSR
GE_{TC}	Gain Temperature Coefficient	V_{CC} = 3V, Internal Ref. (Note 9) C-grade I-grade H-grade			 10 10 10			 10 10 10			 10 10 10		 ppm/°C ppm/°C ppm/°C
	Load Regulation	Internal Ref., Mid-Scale, V_{CC} = 3V ±10%, –5mA ≤ I_{OUT} ≤ 5mA	●		0.009	0.016		0.035	0.064		0.14	0.256	LSB/mA
		V_{CC} = 5V ±10%, –10mA ≤ I_{OUT} ≤ 10mA	●		0.009	0.016		0.035	0.064		0.14	0.256	LSB/mA
R_{OUT}	DC Output Impedance	Internal Ref., Mid-Scale, V_{CC} = 3V ±10%, –5mA ≤ I_{OUT} ≤ 5mA	●		0.09	0.156		0.09	0.156		0.09	0.156	Ω
		V_{CC} = 5V ±10%, –10mA ≤ I_{OUT} ≤ 10mA	●		0.09	0.156		0.09	0.156		0.09	0.156	Ω

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OUT}	DAC Output Span	External Reference Internal Reference			0 to V_{REF} 0 to 2.5		V V
PSR	Power Supply Rejection	V_{CC} = 3V ±10% or 5V ±10%			–80		dB
I_{SC}	Short Circuit Output Current (Note 5) Sinking Sourcing	V_{FS} = V_{CC} = 5.5V Zero-Scale; V_{OUT} Shorted to V_{CC} Full-Scale; V_{OUT} Shorted to GND	 ● ●		 27 –28	 48 –48	 mA mA
Power Supply							
V_{CC}	Positive Supply Voltage	For Specified Performance	●	2.7		5.5	V
IOV_{CC}	Digital Input Supply Voltage	For Specified Performance	●	1.71		5.5	
I_{CC}	Supply Current (Note 6)	V_{CC} = 3V, Internal Reference V_{CC} = 5V, Internal Reference	● ●		2.7 4.6	4 6	mA mA
$I_{CC(IOVCC)}$	Supply Current, IOV_{CC} (Note 6)	IOV_{CC} = 5V	●		25	50	µA
I_{SD}	Supply Current in Power-Down Mode (Note 6)	V_{CC} = 5V, $\overline{PD}$ = 0V	●		0.5	5	µA
$I_{SD(IOVCC)}$	Supply Current in Power-Down Mode, IOV_{CC} (Note 6)	IOV_{CC} = 5V, $\overline{PD}$ = 0V	●		0.5	5	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V to 5.5V, V_{OUT} unloaded unless otherwise specified.

LTC2644-L12/-L10/-L8 (V_{FS} = 2.5V)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference Input							
V_{REF}	Input Voltage Range		●	1		V_{CC}	V
	Resistance		●	120	160	200	kΩ
	Capacitance				7.5		pF
I_{REF}	Reference Current, Power-Down Mode	DAC Powered Down	●		0.005	1.5	µA
Reference Output							
	Output Voltage		●	1.24	1.25	1.26	V
	Reference Temperature Coefficient	(Note 9)			±10		ppm/°C
	Output Impedance				0.5		kΩ
	Capacitive Load Driving				10		µF
	Short Circuit Current	V_{CC} = 5.5V, REF Shorted to GND			2.5		mA
Digital Inputs (IN_A, IN_B, $\overline{PD}$)							
V_{IH}	Digital Input High Voltage		●	0.8•IOV_{CC}			V
V_{IL}	Digital Input Low Voltage		●			0.5	V
I_{LK}	Digital Input Leakage	IN_A/IN_B = GND to IOV_{CC}	●			±1	µA
C_{IN}	Digital Input Capacitance	(Note 7)	●			5	pF
AC Performance							
t_s	Settling Time From IN_A/IN_B Rising Edge (Note 8)	±0.39% (±1LSB at 8 Bits) ±0.098% (±1LSB at 10 Bits) ±0.024% (±1LSB at 12 Bits)			7.0 7.4 7.8		µs µs µs
	Voltage Output Slew Rate				1.0		V/µs
	Capacitive Load Driving				500		pF
	Glitch Impulse	At Mid-Scale Transition			2.1		nV • s
	DAC-to-DAC Crosstalk	1 DAC Held at FS, 1 DAC Switched 0 to FS			0.9		nV • s
	Multiplying Bandwidth	External Reference			320		kHz
e_n	Output Voltage Noise Density	At f = 1kHz, External Reference At f = 10kHz, External Reference At f = 1kHz, Internal Reference At f = 10kHz, Internal Reference			180 160 200 180		nV/√Hz nV/√Hz nV/√Hz nV/√Hz
	Output Voltage Noise	0.1Hz to 10Hz, External Reference 0.1Hz to 10Hz, Internal Reference 0.1Hz to 200kHz, External Reference 0.1Hz to 200kHz, Internal Reference C_{REF} = 0.1µF			35 40 680 730		μV_{P-P} μV_{P-P} μV_{P-P} μV_{P-P}

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V to 5.5V, V_{OUT} unloaded unless otherwise specified.

LTC2644-L12/-L10/-L8 (V_{FS} = 2.5V)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{PWH}	IN_A/IN_B High Time		●	25			ns
t_{PWL}	IN_A/IN_B Low Time		●	25			ns
t_{PER}	IN_A/IN_B Rising Edge to Rising Edge Period	LTC2644-L12	●	0.160		33	ms
		LTC2644-L10	●	0.040		33	ms
		LTC2644-L8	●	0.010		33	ms
t_3	IN_A/IN_B Idle Mode Timeout		●	50		70	ms
t_4	IN_A/IN_B Rising Edge to DAC Update Delay				3.2		µs
f_{MAX}	IN_A/IN_B Frequency	LTC2644-L12	●	0.03		6.25	kHz
		LTC2644-L10	●	0.03		25	kHz
		LTC2644-L8	●	0.03		100	kHz

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltages with respect to GND.

Note 3: Linearity and monotonicity are defined from code 16 to code 4095 (LTC2644-12), code 4 to code 1023 (LTC2644-10) or code 1 to code 255 (LTC2644-8).

Note 4: Inferred from measurement at code 16 (LTC2644-12), code 4 (LTC2644-10) or code 1 (LTC2644-8), and at full-scale.

Note 5: This IC includes current limiting that is intended to protect the device during momentary overload conditions. Junction temperature can exceed the rated maximum during current limiting. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 6: INx at 0V or IOV_{CC}.

Note 7: Guaranteed by design and not production tested.

Note 8: Internal Reference mode. DAC is stepped ¼ scale to ¾ scale and ¾ scale to ¼ scale. Load is 2kΩ in parallel with 100pF to GND.

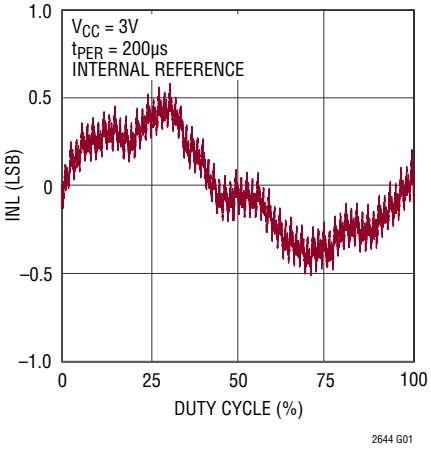
Note 9: Temperature coefficient is calculated by dividing the maximum change in output voltage by the specified temperature range.

TYPICAL PERFORMANCE CHARACTERISTICS

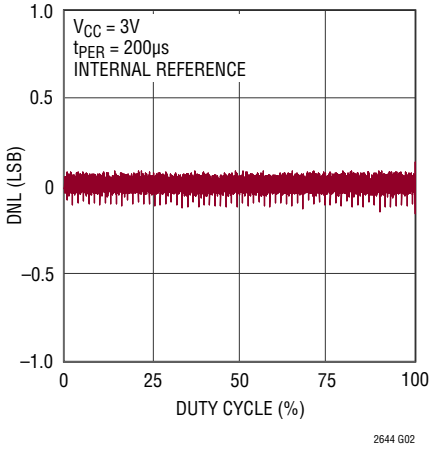
(T_A = 25°C, unless otherwise noted.)

LTC2644-12 (Internal Reference, V_{FS} = 2.5V)

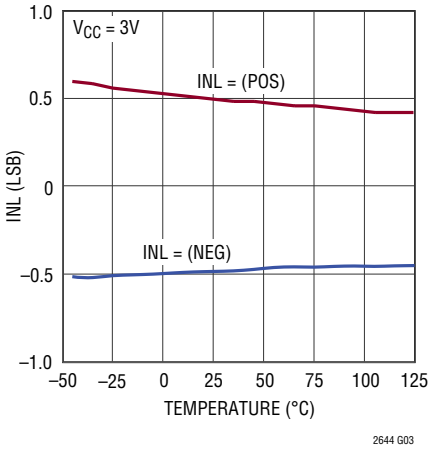
Integral Nonlinearity (INL)



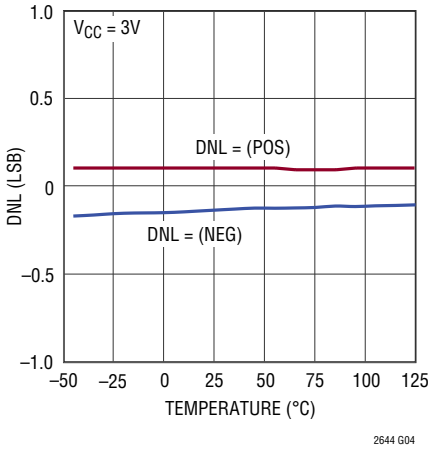
Differential Nonlinearity (DNL)



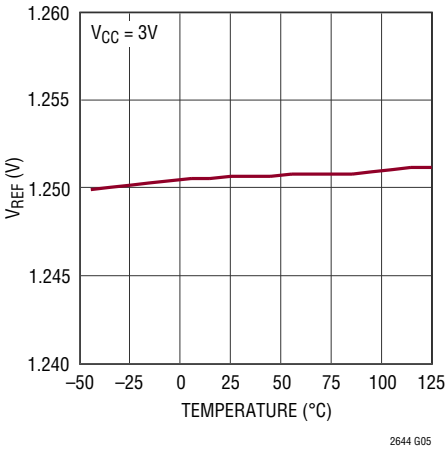
INL vs Temperature



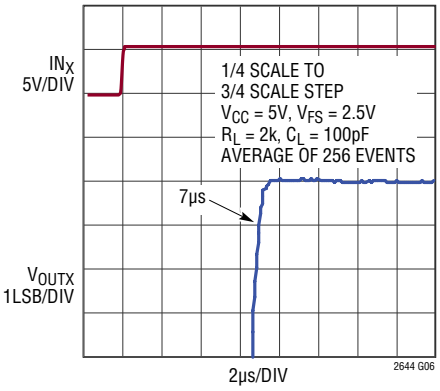
DNL vs Temperature



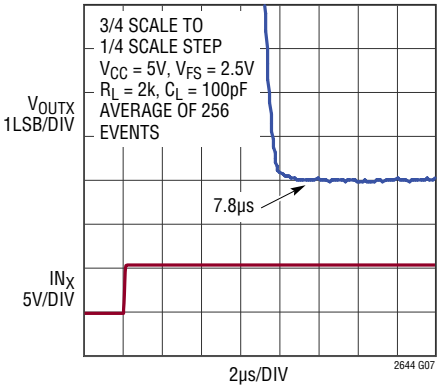
Reference Output Voltage vs Temperature



Settling to ±1LSB Rising



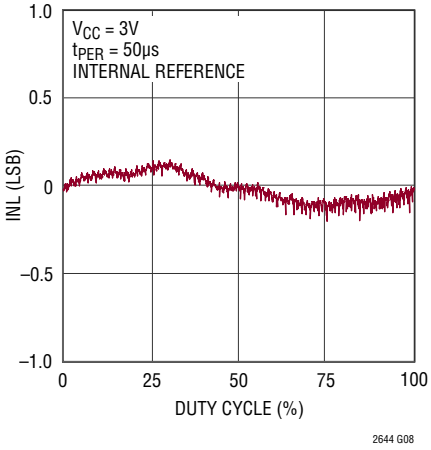
Settling to ±1LSB Falling



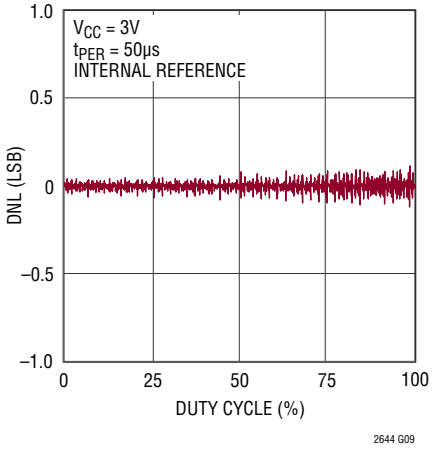
TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C, unless otherwise noted.)

LTC2644-10 (Internal Reference, V_{FS} = 2.5V)

Integral Nonlinearity (INL)

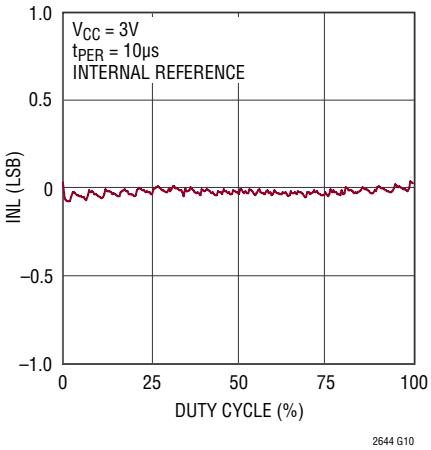


Differential Nonlinearity (DNL)

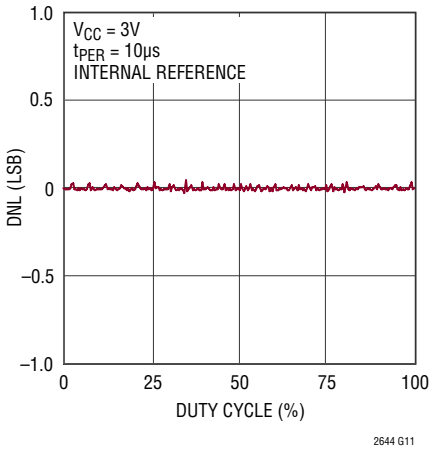


LTC2644-8 (Internal Reference, V_{FS} = 2.5V)

Integral Nonlinearity (INL)

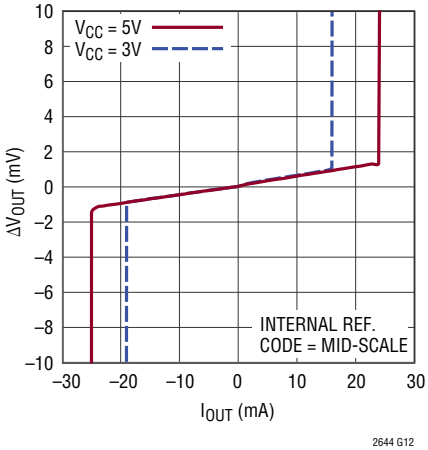


Differential Nonlinearity (DNL)

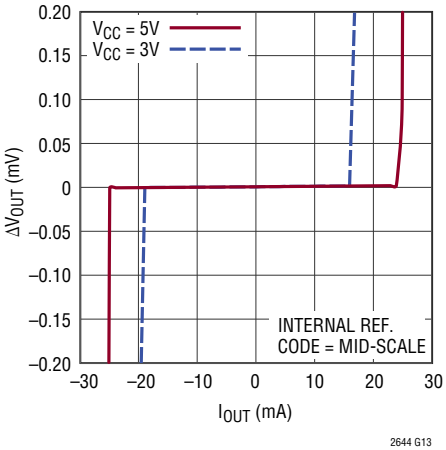


LTC2644

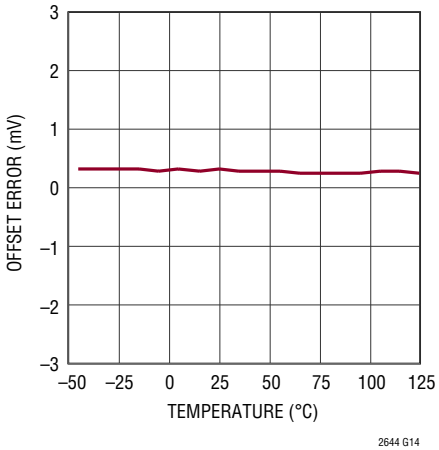
Load Regulation



Current Limiting



Offset Error vs Temperature

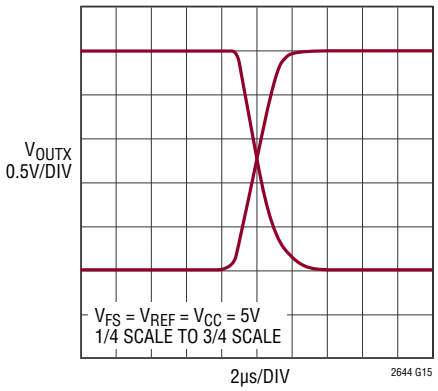


TYPICAL PERFORMANCE CHARACTERISTICS

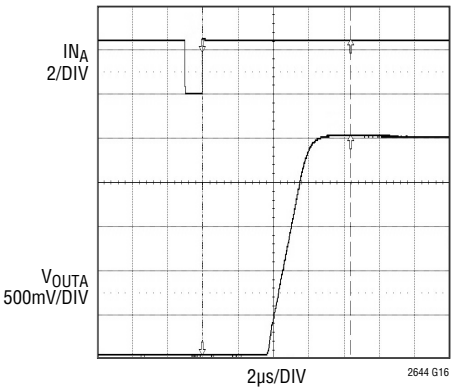
(T_A = 25°C, unless otherwise noted.)

(Internal Reference, V_{FS} = 2.5V)

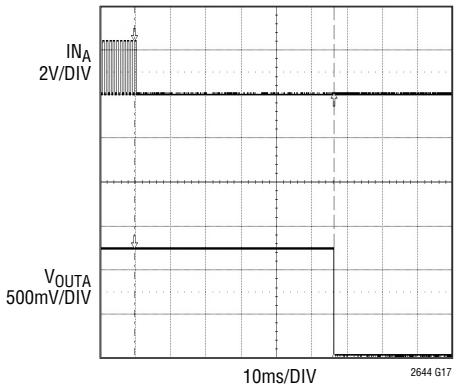
Large-Signal Response



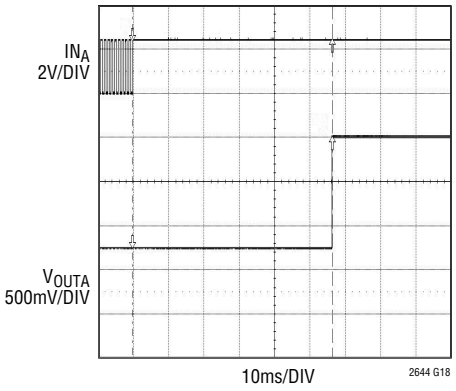
IN_X to V_{OUTX} Delay Full-Scale Transition



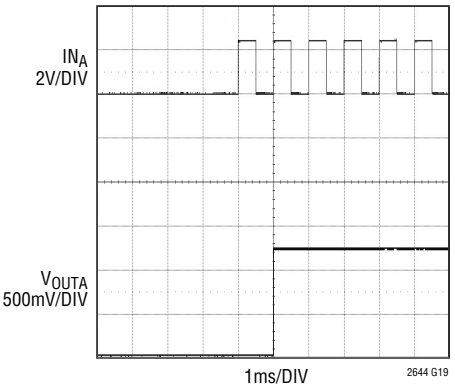
Entering Idle Mode Zero-Scale from Mid-Scale (IDLSEL = GND)



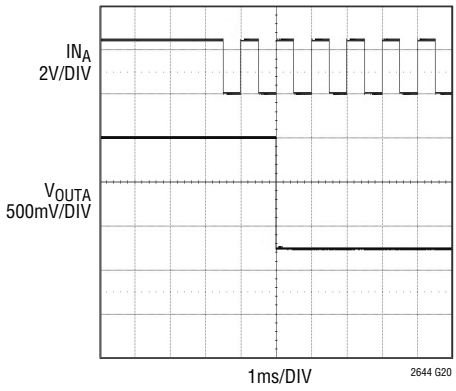
Entering Idle Mode Full-Scale from Mid-Scale (IDLSEL = GND)



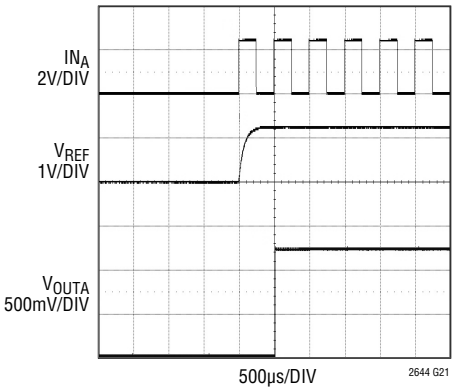
Exiting Idle Mode Zero-Scale to Mid-Scale (IDLSEL=GND)



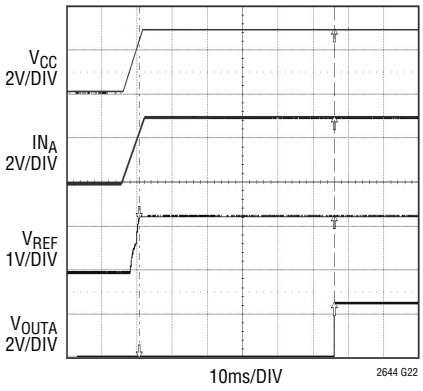
Exiting Idle Mode Full-Scale to Mid-Scale (IDLSEL = GND)



Exiting Idle Mode Power-Down (1 Channel) to Mid-Scale (IDLSEL = V_{CC})



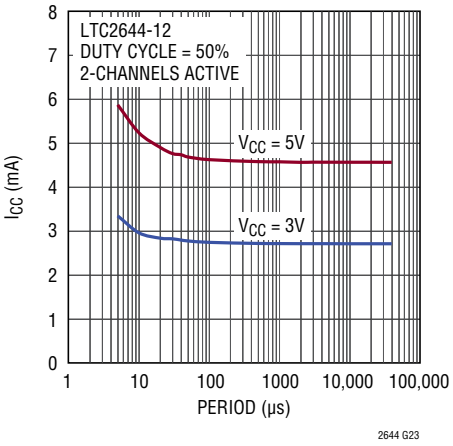
Power-On-Reset to Idle Mode Full-Scale (IDLSEL = GND)



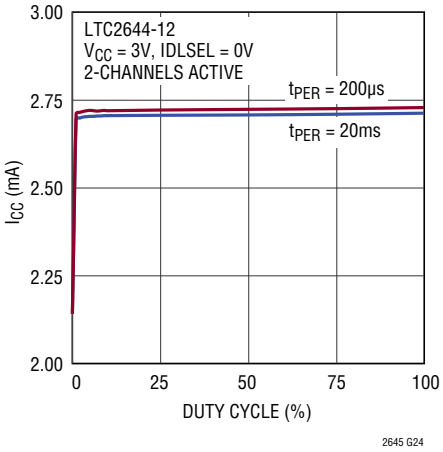
TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C, unless otherwise noted.)

(Internal Reference, V_{FS} = 2.5V)

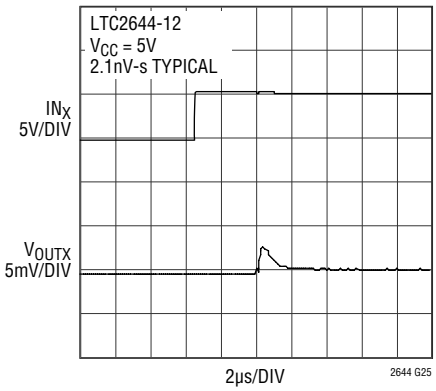
Supply Current vs Input Period (t_{PER})



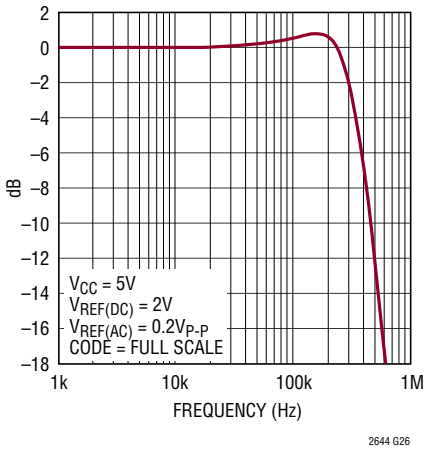
Supply Current vs Duty Cycle (t_{PW}/t_{PER})



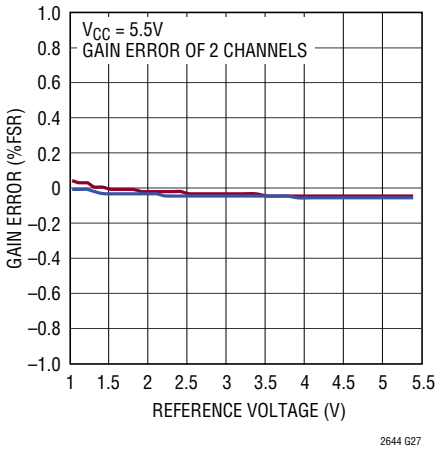
Mid-Scale Glitch Impulse



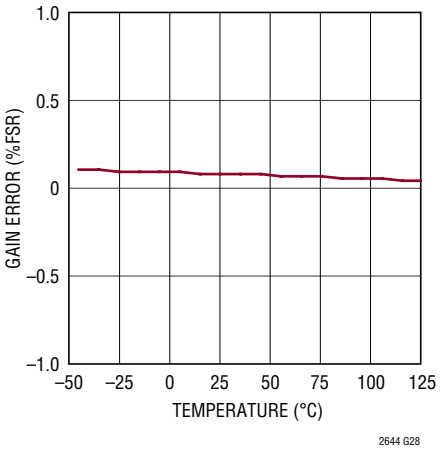
Multiplying Bandwidth



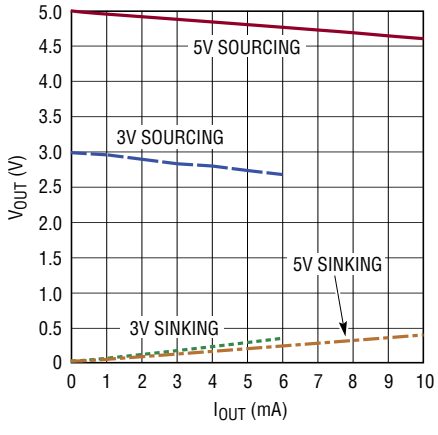
Gain Error vs Reference Input



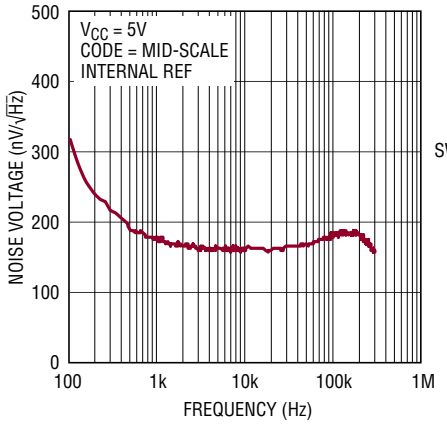
Gain Error vs Temperature



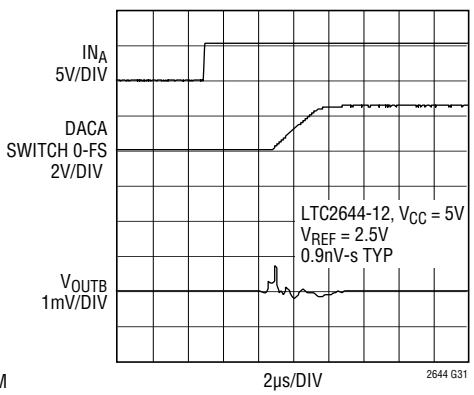
Headroom at Rails vs Output Current



Noise Voltage vs Frequency



DAC-to-DAC Crosstalk (Dynamic)



PIN FUNCTIONS

V_{CC} (Pin 1): Supply Voltage Input. 2.7V ≤ V_{CC} ≤ 5.5V. Bypass to GND with a 0.1µF capacitor.

V_{OUTA}, V_{OUTB} (Pins 2, 3): DAC Analog Voltage Outputs. The DAC output voltage can be calculated by the following equation:

$$V_{OUTX} = V_{REF} \bullet t_{PWHX}/t_{PERX}$$

where V_{REF} is 2.5V in internal reference mode or the REF pin voltage in external reference mode, t_{PWHX} is the pulse width of the preceding IN_X period and t_{PERX} is the time between the two most recent IN_X rising edges.

IDLSEL (Pin 4): Idle Mode Select Input. Connect IDLSEL to GND or V_{CC} to select the behavior of the DAC output when there has been no rising edge on the PWM input for more than the idle mode timeout delay t_3 (nominal delay is 60ms). Available idle mode states are power-down with high impedance output, hold previous state, zero-scale or full-scale. This pin also selects the initial state of the DAC outputs following a power-on reset.

IOV_{CC} (Pin 5): I/O Supply Voltage Input. 1.71V ≤ IOV_{CC} ≤ 5.5V. Bypass to GND with a 0.1µF capacitor.

GND (Pins 6, 12): Ground.

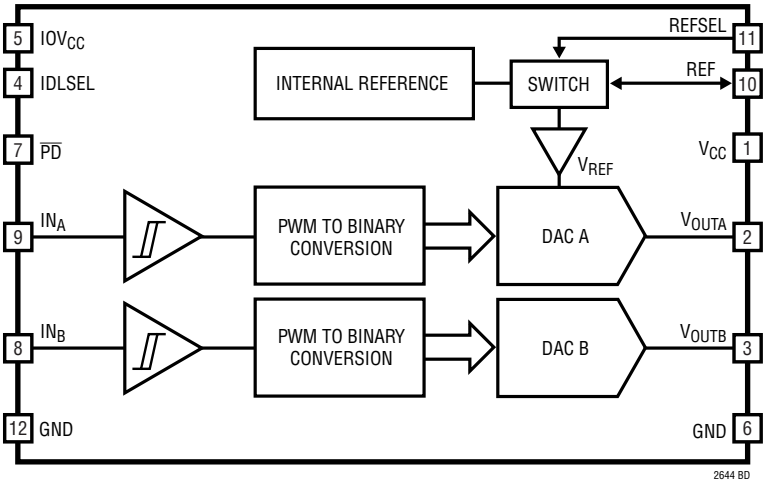
$\overline{PD}$ (Pin 7): Active-Low Power-Down Input. Connect $\overline{PD}$ to GND to place the part in power-down with a typical supply current of <1µA. Connect $\overline{PD}$ to IOV_{CC} for normal operation.

IN_A, IN_B (Pins 9, 8): PWM Inputs. Apply a pulse-width modulated input frequency between 30Hz and 6.25kHz (12-bit), 25kHz (10-bit) or 100kHz (8-bit). After each IN_X rising edge, the part calculates the duty cycle based upon the pulse width and period and updates DAC channel V_{OUTX}. Logic levels are referenced to IOV_{CC}.

REFSEL (Pin 11): Reference Select Input. Connect REFSEL to GND to select internal reference mode. Connect REFSEL to V_{CC} to select external reference mode.

REF (Pin 10): Reference Voltage Input or Output. When REFSEL is connected to V_{CC}, REF is an input (1V ≤ V_{REF} ≤ V_{CC}) where the voltage supplied sets the full-scale DAC output voltage. When REFSEL is connected to GND, the 10ppm/°C, 1.25V internal reference (half full-scale) is available at the pin. This output may be bypassed to GND with up to 10µF and must be buffered when driving external DC load current.

BLOCK DIAGRAM



TIMING DIAGRAMS

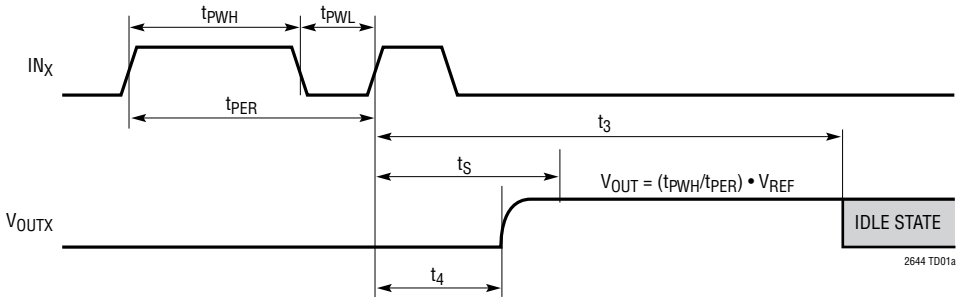


Figure 1a.

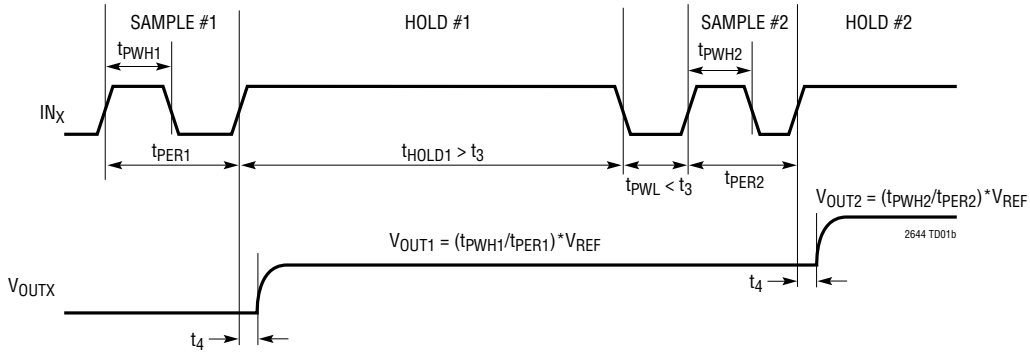


Figure 1b. Sample/Hold Operation (IDLSEL = V_{CC})

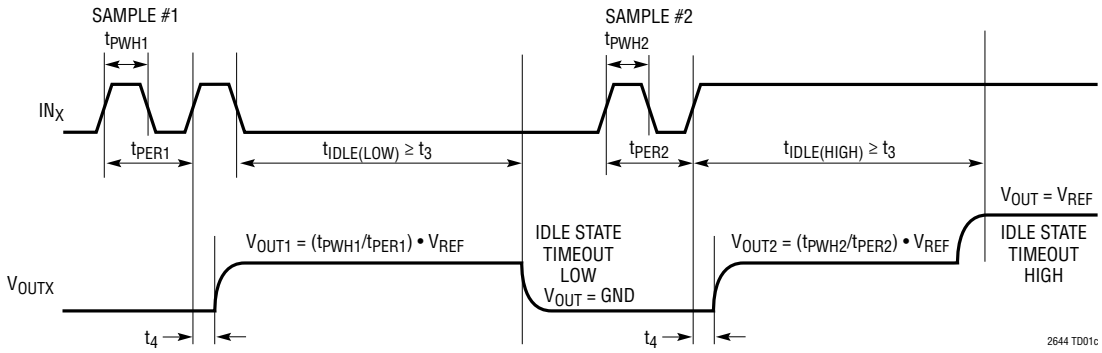


Figure 1c. Transparent Operation (IDLSEL = GND)

OPERATION

The LTC2644 is a family of dual PWM input, voltage output DACs in a 12-lead MSOP package. The part measures the pulse width and period of the PWM inputs and updates each DAC output after the corresponding PWM input rising edge. Each DAC can operate rail-to-rail using an external reference, or with a 2.5V full-scale voltage using an integrated reference. Three resolutions (12-, 10-, and 8-bit) are available.

PWM-to-Voltage Conversion

The LTC2644 converts a PWM input to an accurate, stable, buffered voltage without the latency, slow settling, and high-value passive components required for discrete solutions. The PWM input pins (IN_X) accept frequencies from 30Hz up to 6.25kHz (12-bit), 25kHz (10-bit), or 100kHz (8-bit).

The duty cycle is calculated after each PWM input rising edge based upon the previous high and low pulse width. The resulting digital DAC code k is calculated as:

$$k = 2^N \bullet t_{PWHX} / t_{PERX}$$

where t_{PWHX} is the pulse width of the preceding IN_X period and t_{PERX} is the time between the two most recent IN_X rising edges. The digital-to-analog transfer function is:

$$V_{OUT(IDEAL)} = \left(\frac{k}{2^N}\right) V_{REF}, \text{ for } k = 0 \text{ to } 2^N - 1$$

where N is the resolution, V_{REF} is 2.5V for internal reference mode or the REF pin voltage for external reference mode.

DAC Update Timing

The update for DAC output V_{OUTX} occurs following each rising edge input on IN_X (Figure 1a). Delay t_S is the delay from an IN_X rising edge to the V_{OUTX} settled output voltage corresponding to the previous period's duty cycle. Delay t_S is composed of the computational cycle delay (t_4) and the actual settling of the output DAC. The PWM-to-binary, internal computational cycle begins immediately following the IN_X rising edge. The computational cycle is completed after delay t_4 and the DAC output V_{OUTX} is updated. The DAC output typically settles to 12-bit accuracy within 8µs from the IN_X rising edge.

PWM Input Idle Mode Selection

When no PWM input rising edge is received for more than the idle mode timeout delay t_3 (nominal delay is 60ms), the DAC output enters an idle mode state which can be configured by connecting IDLSEL to GND or V_{CC} according to Table 1 below. Note that these pins also control the initial state of the DACs after power-on reset.

Table 1. Power-On Reset and Idle Mode States

IDLSEL	Power-On Reset	IN_X Idle Low	IN_X Idle Hi
GND	Zero-Scale	Zero-Scale	Full-Scale
V_{CC}	Power-Down Hi-Z	Power-Down Hi-Z	Hold

Transparent Operation

For applications in which the PWM input duty cycle may be 0% or 100%, connect IDLSEL to GND to select transparent operation, in which case an idle low input sets the DAC to zero-scale or an idle high input sets the DAC to full-scale. Figure 1c illustrates the timing for transparent operation. Any pair of PWM input rising edges separated by less than the idle mode timeout delay t_3 (50ms minimum) will cause the DAC code to be updated following the second rising edge. Note that an idle high input state may be followed by an idle low input state.

Sample/Hold Operation

The LTC2644 has the capability to *sample* the pulse-width/period and *hold* the corresponding voltage level indefinitely. Unlike analog filter implementations which require the PWM input to run continuously, the LTC2644 may operate with a discontinuous PWM input. Connect IDLSEL to V_{CC} to select sample/hold operation, in which a single pair of rising edges is sufficient to update the DAC, and the DAC code retains its previous value when the

OPERATION

PWM input idles high. Figure 1b illustrates correct timing for sample/hold operations. Any pair of rising edges separated by less than the idle timeout delay t_3 (50ms minimum) will cause the DAC code to be updated. Any pair of rising edges separated by more than t_3 (70ms maximum) will be ignored and the DAC code will retain its previous value. Note that after power-on-reset or when IN_X idles low, the DAC will power down with a high impedance output.

Short IN_X Period Operation

The accuracy of the PWM to voltage conversion is guaranteed for IN_X input frequencies up to 6.25 kHz (12-bit), 25kHz (10-bit) or 100kHz (8-bit). Faster IN_X input frequencies will proportionally decrease the resolution and accuracy of the analog output. For IN_X input periods of less than the computational delay t_4 (nominally 3.2µs), the DAC update will be skipped and the DAC code will retain its previous value.

Short IN_X Pulse-Width Operation

Provide IN_X input high and low pulse widths greater than t_{PWH} and t_{PWL} to ensure that the DAC output is updated after every IN_X rising edge. High going pulses narrower than t_{PWH} will cause the DAC code to be calculated as zero-scale, and low going pulses narrower than t_{PWL} will cause the DAC code to be calculated as full-scale. For much narrower pulse widths of only a few nanoseconds, the input edge may not be recognized, in which case the DAC update will be skipped entirely and the DAC code will retain its previous value.

Power-On Reset

The LTC2644 resets the output to a known state when power is first applied, making system initialization consistent and repeatable. Connect the IDLSEL pin to GND or V_{CC} according to Table 1 to cause the DACs to initialize to zero-scale or with the device powered down and the DAC outputs high impedance.

For some applications, downstream circuits are active during DAC power-up, and may be sensitive to nonzero outputs from the DAC during this time. The LTC2644 contains circuitry to reduce the power-on glitch when zero-scale reset is selected: the analog output typically rises less than 5mV above zero-scale during power on if the power supply is ramped to 5V in 1ms or more. In general, the glitch amplitude decreases as the power supply ramp time is increased.

Reference Modes

For applications where an accurate external reference is not available, nor desirable due to limited space, the LTC2644 has a user-selectable, integrated reference. Internal Reference mode can be selected by connecting the REFSEL pin to GND.

The 10ppm/°C, 1.25V internal reference is available at the REF pin. This voltage is internally amplified by 2x to provide a 2.5V full-scale DAC output voltage range. Adding bypass capacitance to the REF pin will improve noise performance; 0.1µF is recommended, and up to 10µF can be driven without oscillation. The REF output must be buffered when driving an external DC load current.

Alternatively, the DAC can operate in External Reference mode by connecting the REFSEL pin to V_{CC}. In this mode, an input voltage supplied externally to the REF pin provides the reference ($1V \le V_{REF} \le V_{CC}$) and the supply current is reduced. In this mode the full-scale DAC output voltage is equal to the voltage at the REF pin.

Power-Down Mode

For power constrained applications, power-down mode can be used to reduce the supply current whenever less than two DAC outputs are needed. When in power-down mode, the buffer amplifiers, bias circuits, and integrated reference circuits are disabled, and draw essentially zero current.

OPERATION

If IDLSEL is connected to V_{CC}, either or both channels can be powered down by keeping the PWM input(s) (IN_A/IN_B) low for the idle mode timeout delay t_3. The integrated reference is automatically powered down when external reference mode is selected or when both DAC channels are powered down. In addition, both DAC channels and the integrated reference can be powered down by pulling the $\overline{PD}$ pin low. When the integrated reference is powered down, the REF pin becomes high impedance (typically > 1GΩ).

Normal operating current resumes when $\overline{PD}$ returns high for transparent operation (IDLSEL = GND). For sample/hold operation (IDLSEL = V_{CC}), the LTC2644 remains in full power-down until the first rising edge is received on any PWM input. Any pair of PWM input rising edges separated by less than the idle mode timeout delay t_3 (50ms minimum) will cause the DAC code to be updated. The DAC output(s) will remain in Hi-Z until the channel is updated following the second rising PWM input edge.

Voltage Output

The LTC2644's integrated rail-to-rail amplifier has guaranteed load regulation when sourcing or sinking up to 10mA at 5V, and 5mA at 3V.

Load regulation is a measure of the amplifier's ability to maintain the rated voltage accuracy over a wide range of load current. The measured change in output voltage per change in forced load current is expressed in LSB/mA.

DC output impedance is equivalent to load regulation, and may be derived from it by simply calculating a change in units from LSB/mA to Ω. The amplifier's DC output impedance is 0.1Ω when driving a load well away from the rails.

When drawing a load current from either rail, the output voltage headroom with respect to that rail is limited by the 50Ω typical channel resistance of the output devices (e.g., when sinking 1mA, the minimum output voltage is 50Ω • 1mA, or 50mV). See the graph Headroom at Rails vs Output Current in the Typical Performance Characteristics section.

The amplifier is stable driving capacitive loads of up to 500pF.

Rail-to-Rail Output Considerations

In any rail-to-rail voltage output device, the output is limited to voltages within the supply range.

Since the analog output of the DAC cannot go below ground, it may limit the lowest codes reachable as shown in Figure 2b. Similarly, limiting can occur near full-scale when the REF pin is tied to V_{CC}. If $V_{REF} = V_{CC}$ and the DAC full-scale error (FSE) is positive, the output for the highest codes limits at V_{CC}, as shown in Figure 2c. No full-scale limiting will occur if V_{REF} is less than V_{CC}–FSE.

Offset and linearity are defined and tested over the region of the DAC transfer function where no output limiting can occur.

Board Layout

The PC board should have separate areas for the analog and digital sections of the circuit. A single, solid ground plane should be used, with analog and digital signals carefully routed over separate areas of the plane. This keeps digital signals away from sensitive analog signals and minimizes the interaction between digital ground currents and the analog section of the ground plane. The resistance from the LTC2644 GND pin to the ground plane should be as low as possible. Resistance here will add directly to the effective DC output impedance of the device (typically 0.1Ω). Note that the LTC2644 is no more susceptible to this effect than any other parts of this type; on the contrary, it allows layout-based performance improvements to shine rather than limiting attainable performance with excessive internal resistance.

OPERATION

Another technique for minimizing errors is to use a separate power ground return trace on another board layer. The trace should run between the point where the power supply is connected to the board and the DAC ground pin. Thus the DAC ground pin becomes the common point for analog ground, digital ground, and power ground. When the LTC2644 is sinking large currents, this current flows out of the ground pin and directly into the power ground trace without affecting the analog ground plane voltage.

It is sometimes necessary to interrupt the ground plane to confine digital ground currents to the digital portion of the plane. When doing this, make the gap in the plane only as long as it needs to be to serve its purpose and ensure that no traces cross over the gap.

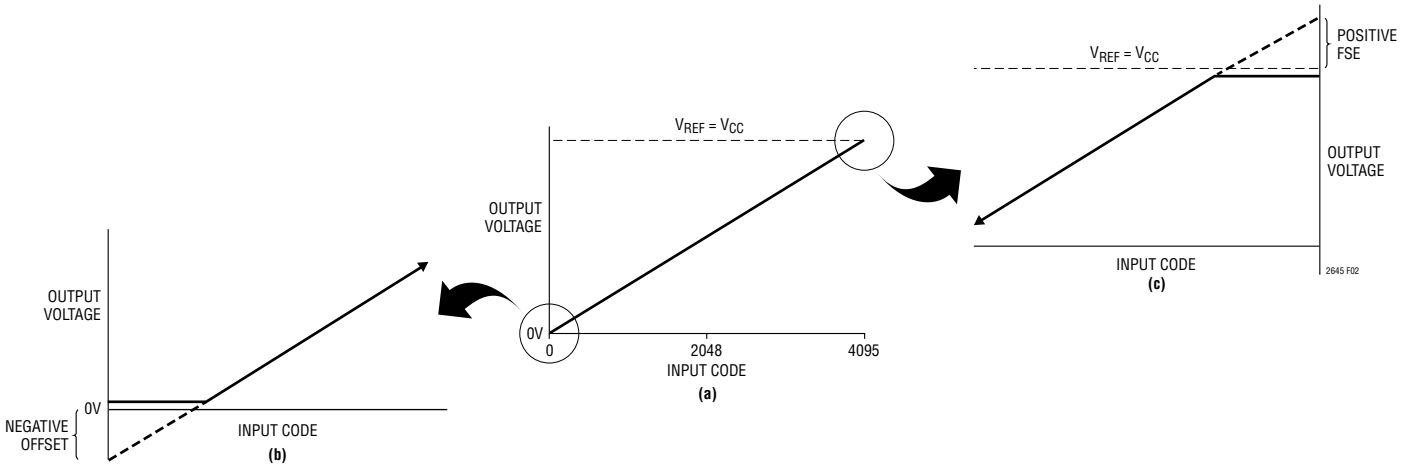


Figure 2. Effects of Rail-to-Rail Operation on a DAC Transfer Curve (Shown for 12 Bits).
(a) Overall Transfer Function
(b) Effect of Negative Offset for Codes Near Zero
(c) Effect of Positive Full-Scale Error for Codes Near Full-Scale

TYPICAL APPLICATIONS

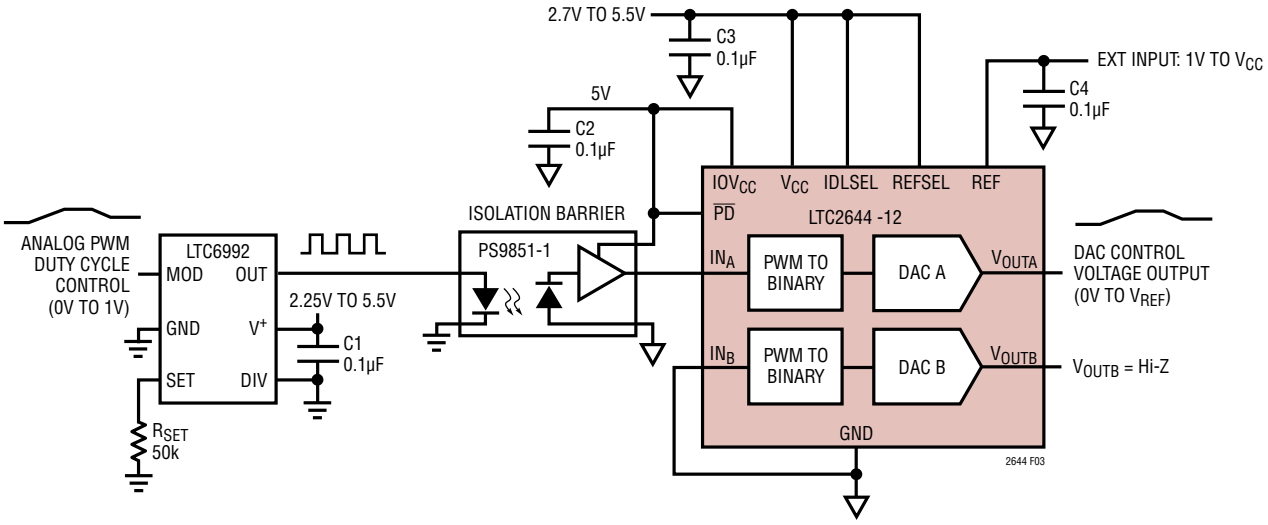
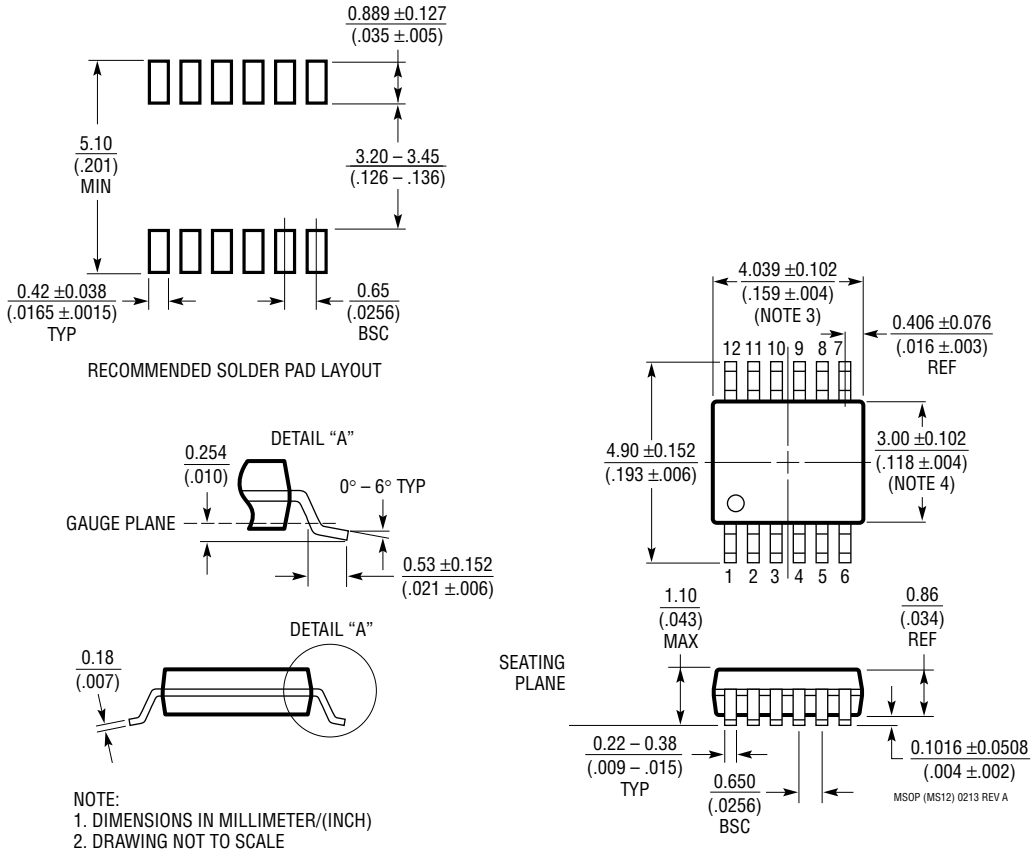


Figure 3. Analog Control Voltage with PWM Transmission to DAC Control Voltage Output

PACKAGE DESCRIPTION

MS Package
12-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1668 Rev A)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	02/17	Corrected $V_{OUT(IDEAL)}$ equation	13
B	11/18	Corrected units of Output Voltage Noise	5

TYPICAL APPLICATION

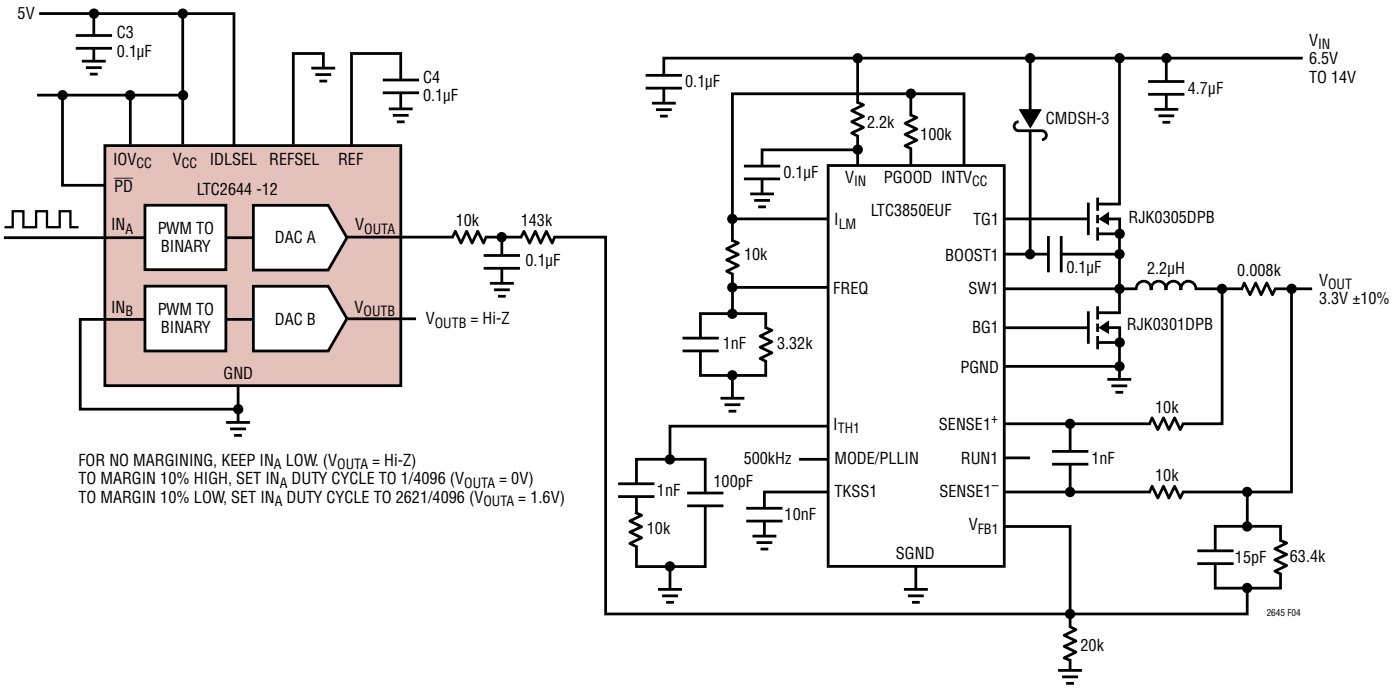


Figure 4. Voltage Margining Application with LTC3850 (3.3V ±10%)

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC2645	Quad 12-/10-/8-Bit PWM to V_{OUT} DACs with 10ppm/°C Reference	Zero Latency Bus Update, 100kHz to 30Hz Input Frequency, ±2.5LSB INL, 2.7V to 5.5V Supply Range, 16-Lead MSOP Package
LT®1991	Precision, 100µA Gain Selectable Amplifier	Gain Accuracy of 0.04%, Gains from –13 to 14, 100µA Precision Op Amp
LT1469-2	Dual 200MHz, 30V/µs 16-Bit Accurate Op Amp	200MHz Gain Bandwidth, 125µV Offset, 30V/µs Slew Rate Precision Op Amp
LTC2055	Dual Micropower Zero-Drift Op Amp	2.7V Minimum Supply Voltage, 150µA Supply Current per Amplifier, Zero-Drift Op Amp
LTC6992	Timer Blox: Voltage-Controlled Pulse Width Modulator (PWM)	3.8Hz to 1MHz Output Frequency Range, 0V to 1V Analog Input, < 1.7% Maximum Frequency Error
LTC2632/LTC2633	Dual 12-/10-/8-Bit SPI/I^2C V_{OUT} DACs with 10ppm/°C Reference	±2.5LSB INL, 2.7V to 5.5V Supply Range, 10ppm/°C Reference, External REF Mode, 8-Lead ThinSOT™ Package