MMBT6589T1

High Current Surface Mount PNP Silicon Switching Transistor for Load Management in Portable Applications

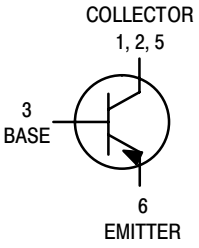
ON Semiconductor®

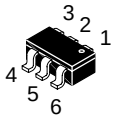
http://onsemi.com

30 VOLTS, 2.0 AMPS PNP TRANSISTOR

Features

- Pb−Free Package is Available





TSOP−6
CASE 318G
STYLE 7

MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Max	Unit
Collector-Emitter Voltage	V_{CEO}	−30	Vdc
Collector-Base Voltage	V_{CBO}	−50	Vdc
Emitter-Base Voltage	V_{EBO}	−5.0	Vdc
Collector Current − Continuous	I_C	−1.0	Adc
Collector Current − Peak	I_{CM}	−2.0	A
Electrostatic Discharge	ESD	HBM Class 3 MM Class C	

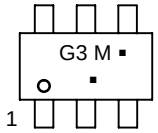
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D (Note 1)	540 4.4	mW mW/°C
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$ (Note 1)	230	°C/W
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D (Note 2)	925 7.4	mW mW/°C
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$ (Note 2)	135	°C/W
Total Device Dissipation (Single Pulse < 10 s)	$P_{Dsingle}$ (Note 2) (Note 3)	1.3	W
Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. FR−4 @ Minimum Pad
2. FR−4 @ 1.0 X 1.0 inch Pad
3. ref: Figure 8

MARKING DIAGRAM



G3 = Specific Device Code
M = Date Code*
▪ = Pb−Free Package
(Note: Microdot may be in either location)
*Date Code orientation may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
MMBT6589T1	TSOP−6	3000/Tape & Reel
MMBT6589T1G	TSOP−6 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Breakdown Voltage (I_C = −10 mAdc, I_B = 0)	$V_{(BR)CEO}$	−30	−	Vdc
Collector−Base Breakdown Voltage (I_C = −0.1 mAdc, I_E = 0)	$V_{(BR)CBO}$	−50	−	Vdc
Emitter−Base Breakdown Voltage (I_E = −0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	−5.0	−	Vdc
Collector Cutoff Current (V_{CB} = −30 Vdc, I_E = 0)	I_{CBO}	−	−0.1	μAdc
Collector−Emitter Cutoff Current (V_{CES} = −30 Vdc)	I_{CES}	−	−0.1	μAdc
Emitter Cutoff Current (V_{EB} = −4.0 Vdc)	I_{EBO}	−	−0.1	μAdc
ON CHARACTERISTICS				
DC Current Gain (Note 4) (Figure 1) (I_C = −1.0 mA, V_{CE} = −2.0 V) (I_C = −500 mA, V_{CE} = −2.0 V) (I_C = −1.0 A, V_{CE} = −2.0 V) (I_C = 2.0 A, V_{CE} = −2.0 V)	h_{FE}	 100 100 80 40	 − 300 − −	
Collector−Emitter Saturation Voltage (Note 4) (Figure 3) (I_C = −0.5 A, I_B = −0.05 A) (I_C = −1.0 A, I_B = 0.1 A) (I_C = −2.0 A, I_B = −0.2 A)	$V_{CE(sat)}$	 − − −	 −0.25 −0.30 −0.65	V
Base−Emitter Saturation Voltage (Note 4) (Figure 2) (I_C = −1.0 A, I_B = −0.1 A)	$V_{BE(sat)}$	−	−1.2	V
Base−Emitter Turn−on Voltage (Note 4) (I_C = −1.0 A, V_{CE} = −2.0 V)	$V_{BE(on)}$	−	−1.1	V
Cutoff Frequency (I_C = −100 mA, V_{CE} = −5.0 V, f = 100 MHz)	f_T	100	−	MHz
Output Capacitance (V_{CB} = −5.0 V, f = 1.0 MHz)	Cobo	−	20	pF

4. Pulsed Condition: Pulse Width = 300 μsec, Duty Cycle ≤ 2%

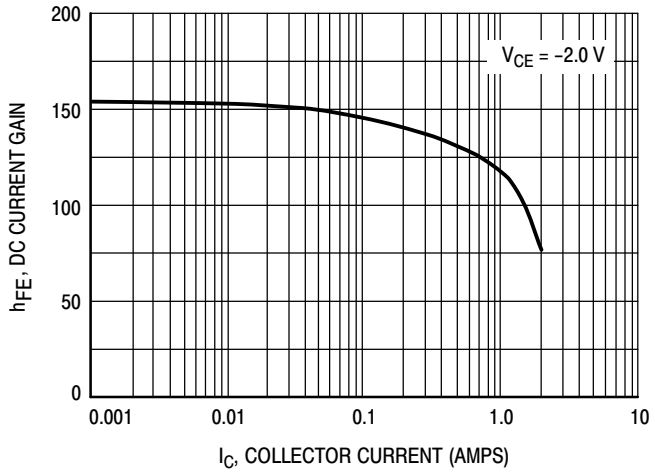


Figure 1. DC Current Gain versus Collector Current

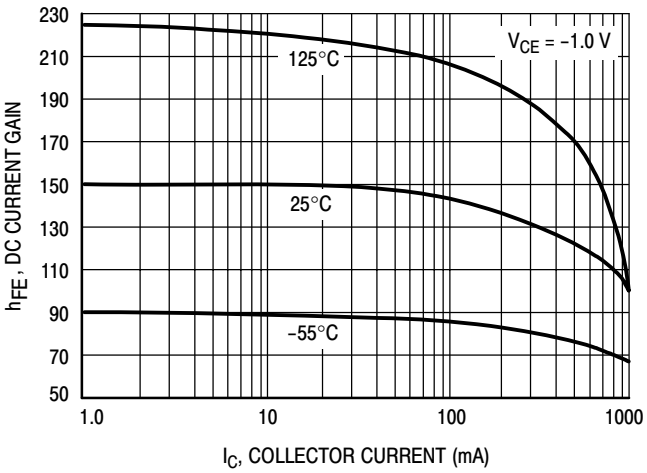


Figure 2. DC Current Gain versus Collector Current

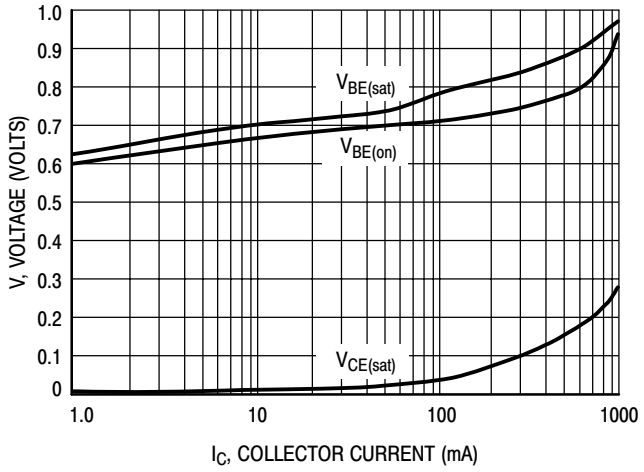


Figure 3. “On” Voltages

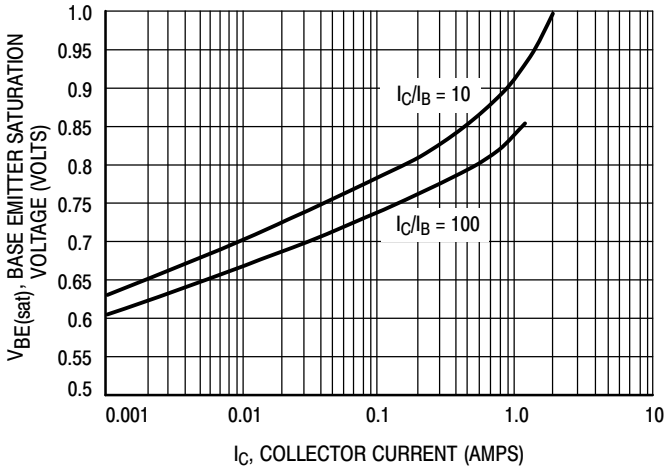


Figure 4. Base Emitter Saturation Voltage versus Collector Current

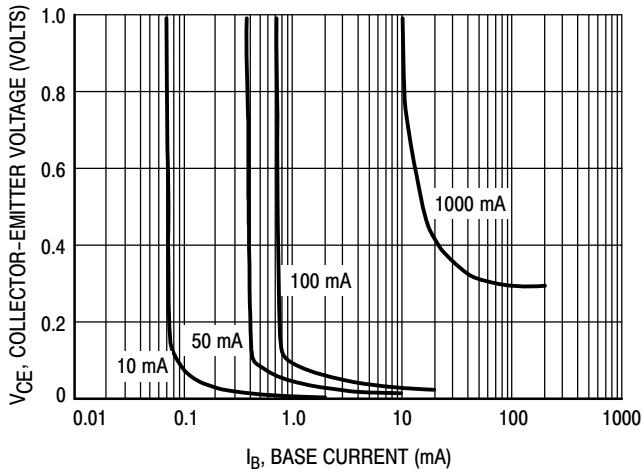


Figure 5. Collector Emitter Saturation Voltage versus Collector Current

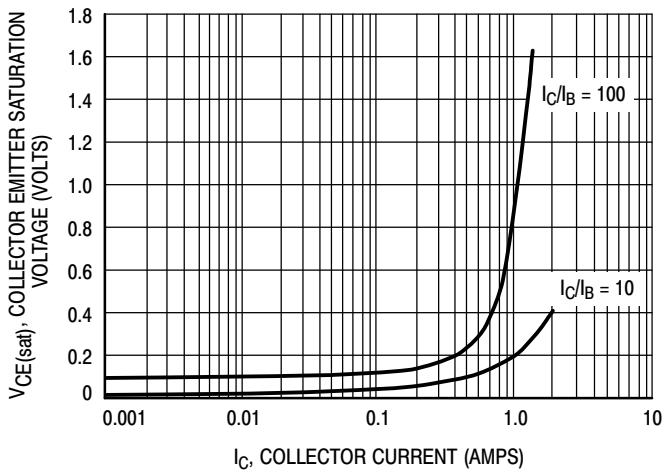


Figure 6. Collector Emitter Saturation Voltage versus Collector Current

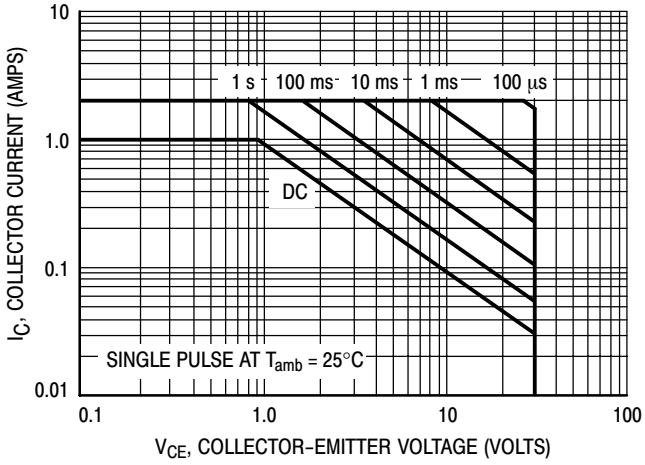


Figure 7. Safe Operating Area

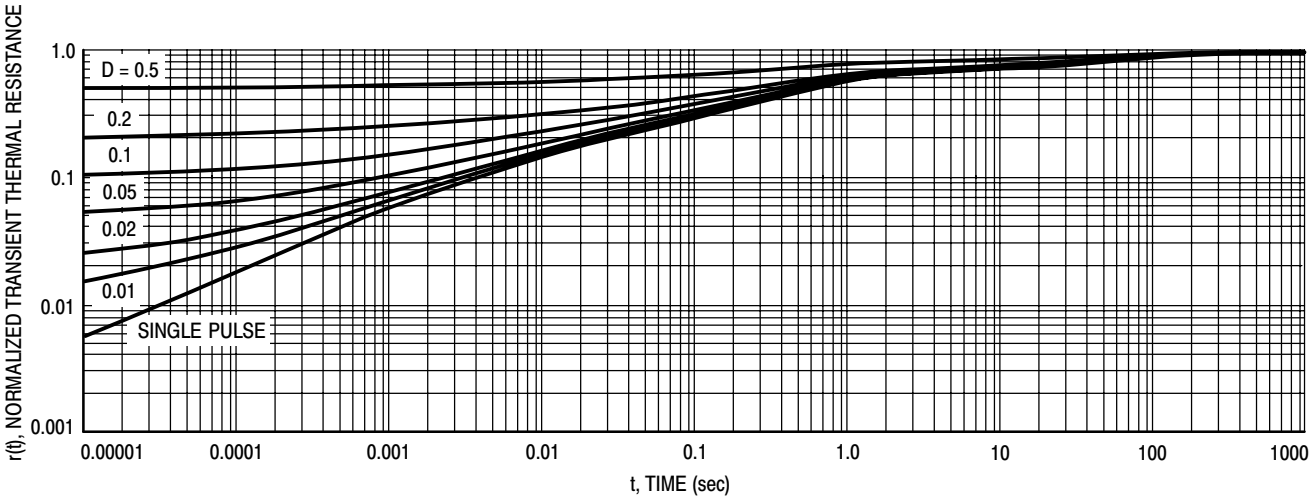


Figure 8. Normalized Thermal Response

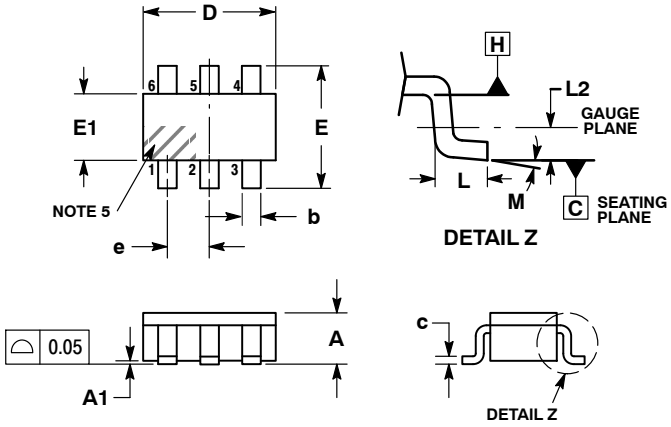
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

1

SCALE 2:1

TSOP−6
CASE 318G−02
ISSUE V

DATE 12 JUN 2012



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

	MILLIMETERS		
DIM	**MIN**	**NOM**	**MAX**
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	–	10°

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 2:
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2

STYLE 3:
PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out

STYLE 4:
PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD

STYLE 5:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 6:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 7:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER

STYLE 8:
PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND

STYLE 9:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE

STYLE 10:
PIN 1. D(OUT)+
2. GND
3. D(OUT)−
4. D(IN)−
5. VBUS
6. D(IN)+

STYLE 11:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2

STYLE 12:
PIN 1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O

STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1

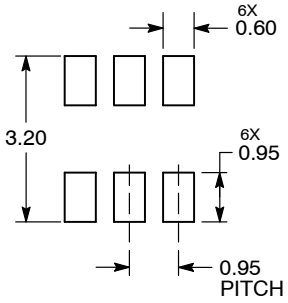
STYLE 14:
PIN 1. ANODE
2. SOURCE
3. GATE
4. CATHODE/DRAIN
5. CATHODE/DRAIN
6. CATHODE/DRAIN

STYLE 15:
PIN 1. ANODE
2. SOURCE
3. GATE
4. DRAIN
5. N/C
6. CATHODE

STYLE 16:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE

STYLE 17:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR

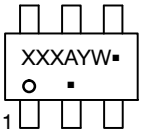
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

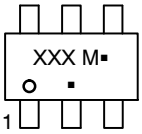
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package



STANDARD

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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