

NB3N51034

3.3V, Crystal to 100MHz/ 200MHz Quad HCSL/LVDS Clock Generator

The NB3N51034 is a high precision, low phase noise clock generator that supports spread spectrum designed for PCI Express applications. This device takes a 25 MHz fundamental mode parallel resonant crystal and generates 4 differential HCSL/LVDS outputs at 100 MHz or 200 MHz (See Figure 8 for LVDS interface). The NB3N51034 provides selectable spread options of -0.5%, -1.0%, -1.5%, for applications demanding low Electromagnetic Interference (EMI) as well as optimum performance with no spread option.

Features

- Uses 25 MHz Fundamental Mode Parallel Resonant Crystal
- Power Down Mode
- 4 Low Skew HCSL or LVDS Outputs
- OE Tri-States Outputs
- Spread of -0.5%, -1.0%, -1.5% and No Spread
- PCIe Gen 1, Gen 2, Gen 3, Gen 4 Compliant
- Phase Noise (SS OFF) @ 100 MHz:

| Offset | Noise Power |
|---------|-------------|
| 100 Hz | -110 dBc/Hz |
| 1 kHz | -123 dBc/Hz |
| 10 kHz | -134 dBc/Hz |
| 100 kHz | -137 dBc/Hz |
| 1 MHz | -138 dBc/Hz |
| 10 MHz | -154 dBc/Hz |

- Operating Supply Voltage Range 3.3 V \pm 5%
- Industrial Temperature Range -40°C to +85°C
- Functionally Compatible with IDT557-05, IDT5V41066, IDT5V41236 with enhanced performance
- These are Pb-Free Devices

Applications

- Networking
- Consumer

- Computing and Peripherals
- Industrial Equipment
- PCIe Clock Generation Gen 1, Gen 2, Gen 3 and Gen 4

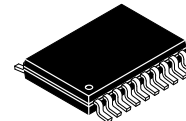
End Products

- Switch and Router
- Set Top Box, LCD TV
- Servers, Desktop Computers
- Automated Test Equipment



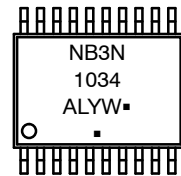
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TSSOP-20
DT SUFFIX
CASE 948E

MARKING DIAGRAM



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 10 of this data sheet.

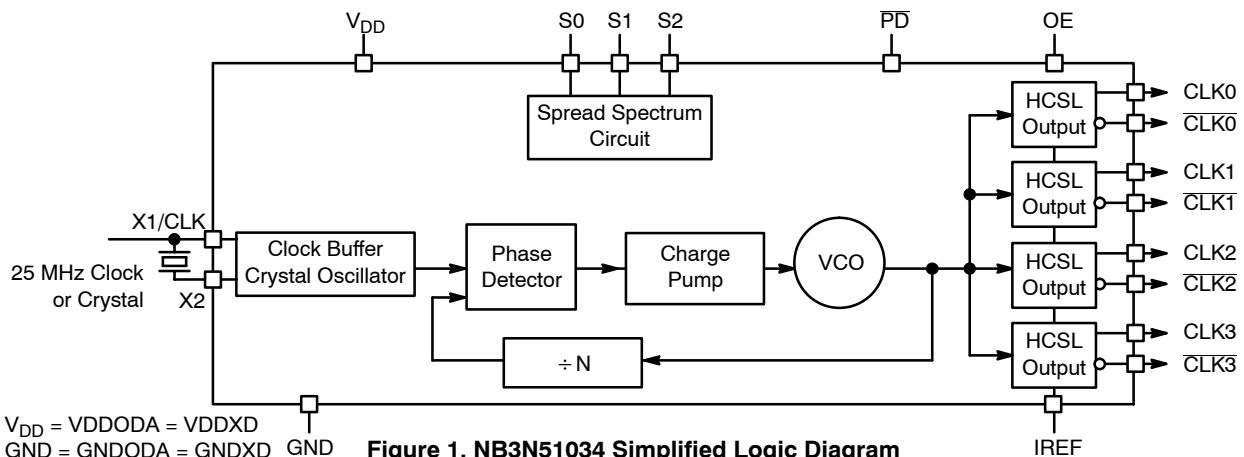


Figure 1. NB3N51034 Simplified Logic Diagram

NB3N51034

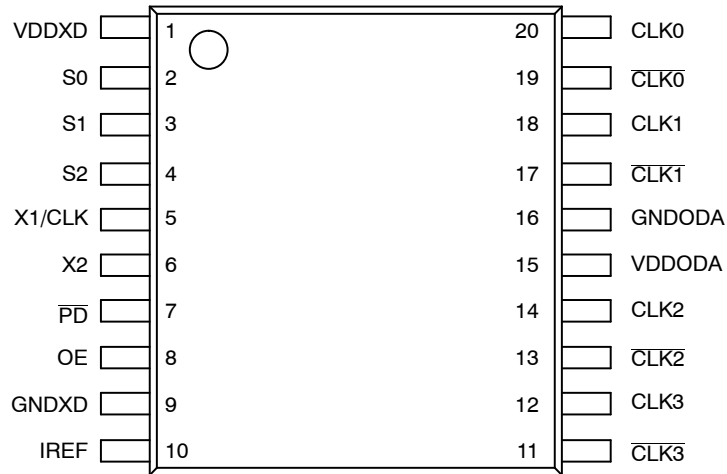


Figure 2. Pin Configuration (Top View)

Table 1. PIN DESCRIPTION

| Pin | Symbol | I/O | Description |
|-----|--------|---------------------|--|
| 1 | VDDXD | Power | Connect to a +3.3 V source. |
| 2 | S0 | Input | LVTTL/LVCMOS frequency select input 0. Internal pullup resistor to VDDXD. See output select table 2 for details. |
| 3 | S1 | Input | LVTTL/LVCMOS frequency select input 1. Internal pullup resistor to VDDXD. See output select Table 2 for details. |
| 4 | S2 | Input | LVTTL/LVCMOS frequency select input 2. Internal pullup resistor to VDDXD. See output select Table 2 for details. |
| 5 | X1/CLK | Input | Crystal interface or single-ended reference clock input. |
| 6 | X2 | Output | Crystal interface. Float this pin for reference clock input CLK. |
| 7 | PD | Input | LVTTL/LVCMOS power down input. Assert this pin LOW to enter power down mode. Internal pull-up resistor to VDDXD. |
| 8 | OE | Input | Output enable. Tri-state output (High=enable outputs, Low=disable outputs). Internal pull-up resistor. |
| 9 | GNDXD | Power | Connect to digital circuit ground. |
| 10 | IREF | Output | Precision resistor attached to this pin is connected to the internal current reference. |
| 11 | CLK3 | HCSL or LVDS Output | Inverted clock output. (For LVDS levels see Figure 8) |
| 12 | CLK3 | HCSL or LVDS Output | Noninverted clock output. (For LVDS levels see Figure 8) |
| 13 | CLK2 | HCSL or LVDS Output | Inverted clock output. (For LVDS levels see Figure 8) |
| 14 | CLK2 | HCSL or LVDS Output | Noninverted clock output. (For LVDS levels see Figure 8) |
| 15 | VDDODA | Power | Connect to a +3.3 V analog source. |
| 16 | GNDODA | Power | Output and analog circuit ground. |
| 17 | CLK1 | HCSL or LVDS Output | Inverted clock output. (For LVDS levels see Figure 8) |
| 18 | CLK1 | HCSL or LVDS Output | Noninverted clock output. (For LVDS levels see Figure 8) |
| 19 | CLK0 | HCSL or LVDS Output | Inverted clock output. (For LVDS levels see Figure 8) |
| 20 | CLK0 | HCSL or LVDS Output | Noninverted clock output. (For LVDS levels see Figure 8) |

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Table 2. OUTPUT FREQUENCY AND SPREAD SPECTRUM SELECT TABLE

| S2* | S1* | S0* | Spread% | Spread Type | Output Frequency |
|-----|-----|-----|-----------|-------------|------------------|
| 0 | 0 | 0 | -0.5 | Down | 100 |
| 0 | 0 | 1 | -1.0 | Down | 100 |
| 0 | 1 | 0 | -1.5 | Down | 100 |
| 0 | 1 | 1 | No Spread | N/A | 100 |
| 1 | 0 | 0 | -0.5 | Down | 200 |
| 1 | 0 | 1 | -1.0 | Down | 200 |
| 1 | 1 | 0 | -1.5 | Down | 200 |
| 1 | 1 | 1 | No Spread | N/A | 200 |

*Pins S2, S1 and S0 default high when left open.

Recommended Crystal Parameters

| | |
|------------------------------|--------------------|
| Crystal | Fundamental AT-Cut |
| Frequency | 25 MHz |
| Load Capacitance | 16–20 pF |
| Shunt Capacitance, C0 | 7 pF Max |
| Equivalent Series Resistance | 50 Ω Max |
| Initial Accuracy at 25 °C | ±20 ppm |
| Temperature Stability | ±30 ppm |
| Aging | ±20 ppm |

Table 3. ATTRIBUTES

| Characteristic | Value |
|---|----------------------|
| Internal Input Default State Resistor (OE, Sx, PD) | 110 kΩ |
| ESD Protection Human Body Model | 2 kV |
| Moisture Sensitivity, Indefinite Time Out of Dray Pack (Note 1) | Level 1 |
| Flammability Rating Oxygen Index: 28 to 34 | UL 94 V-0 @ 0.125 in |
| Transistor Count | 132,000 |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | |

1. For additional information, see Application Note AND8003/D.

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Table 4. MAXIMUM RATINGS (Note 2)

| Symbol | Parameter | Rating | Units |
|------------------|--|----------------------------------|--------------|
| V _{DD} | Positive Power Supply with respect to GND (VDDXD and VDDODA) | 4.6 | V |
| V _I | Input Voltage with respect to GND (V _{IN}) | -0.5 V to V _{DD} +0.5 V | V |
| T _A | Operating Temperature Range | -40 to +85 | °C |
| T _{stg} | Storage Temperature Range | -65 to +150 | °C |
| θ _{JA} | Thermal Resistance (Junction-to-Ambient) (Note 3) | 0 lfpm 500 lfpm | °C/W °C/W |
| θ _{JC} | Thermal Resistance (Junction-to-Case) | 50 | °C/W |
| T _{sol} | Wave Solder | 265 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and not valid simultaneously. If stress limits are exceeded device functional operation is not implied, damage may occur and reliability may be affected.
- JEDEC standard multilayer board – 2S2P (2 signal, 2 power).

Table 5. DC CHARACTERISTICS (V_{DD} = 3.3 V ±5%, GND = 0 V, T_A = -40°C to +85°C, Note 4)

| Symbol | Characteristic | Min | Typ | Max | Unit |
|---------------------|--|-----------|-----|-----------------------|------|
| V _{DD} | Power Supply Voltage (VDDXD and VDDODA) | 3.135 | 3.3 | 3.465 | V |
| GND | Power Supply Ground (GNDXD and GNDODA) | | 0 | | V |
| I _{DD} | Power Supply Current, 200 MHz output, -1.5% spread | | 135 | | mA |
| I _{DDOE} | Power Supply Current when OE is Set Low | | 60 | | mA |
| I _{DDPD} | Power Supply Current (PD = Low, no load) | | 1.5 | | mA |
| V _{IH} | Input HIGH Voltage (X1/CLK, S0, S1, S2 and OE) | 2000 | | V _{DD} + 300 | mV |
| V _{IL} | Input LOW Voltage (X1/CLK, S0, S1, S2 and OE) | GND - 300 | | 800 | mV |
| V _{max} | Absolute Maximum Output Voltage (Notes 5, 6) | | | 1150 | mV |
| V _{min} | Absolute Minimum Output Voltage (Notes 5, 7) | -300 | | | mV |
| V _{rb} | Ringback Voltage (Notes 8, 9) | -100 | | 100 | mV |
| V _{OH} | Output High Voltage (Note 5) | 660 | | 850 | mV |
| V _{OL} | Output Low Voltage (Note 5) | -150 | | 27 | mV |
| V _{CROSS} | Absolute Crossing Voltage (Notes 5, 9, 10) | 250 | | 550 | mV |
| ΔV _{CROSS} | Total Variation of V _{CROSS} (Notes 5, 9, 11) | | | 140 | mV |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

- VDDXD and VDDODA power pins must be shorted to power supply voltage V_{DD} and GNDXD and GNDODA ground pins must be shorted to power supply ground GND. Measurement taken with outputs terminated with R_S = 33.2 Ω, R_L = 50 Ω, with test load capacitance of 2 pF and current biasing resistor set at 475 Ω. See Figure 7. Guaranteed by characterization.
- Measurement taken from single-ended waveform
- Defined as the maximum instantaneous voltage value including positive overshoot
- Defined as the maximum instantaneous voltage value including negative overshoot
- Measurement taken from differential waveform
- Measured at crossing point where the instantaneous voltage value of the rising edge of CLKx+ equals the falling edge of CLKx-.
- Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
- Defined as the total variation of all crossing voltage of rising CLKx+ and falling CLKx-. This is maximum allowed variance in the V_{CROSS} for any particular system.

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Table 6. AC CHARACTERISTICS ($V_{DD} = 3.3\text{ V} \pm 5\%$, $GND = 0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$; Note 12)

| Symbol | Characteristic | Min | Typ | Max | Unit |
|--------------------|--|-----|--|-------|---------------|
| f_{CLKIN} | Clock/Crystal Input Frequency | | 25 | | MHz |
| f_{CLKOUT} | Output Clock Frequency | | 100/200 | | MHz |
| Φ_{NOISE} | Phase-Noise Performance SS OFF $f_{CLKOUT} = 100\text{ MHz}$ @ 100 Hz offset from carrier @ 1 kHz offset from carrier @ 10 kHz offset from carrier @ 100 kHz offset from carrier @ 1 MHz offset from carrier @ 10 MHz offset from carrier | | -110 -123 -134 -137 -138 -154 | | dBc/Hz |
| $t_{JIT(\Phi)}$ | Phase RMS Jitter, Integration Range 12 kHz to 20 MHz | | 0.4 | | ps |
| f_{MOD} | Spread Spectrum Modulation Frequency | 30 | 31.5 | 33.33 | kHz |
| SS _{RED} | Spectral Reduction, f_{CLKOUT} of 100 MHz with -0.5% spread, 3 rd Harmonic (Note 13) | | -10 | | dB |
| t_{SKEW} | Within Device Output to Output Skew | | | 40 | ps |
| E _{ppm} | Frequency Synthesis Error, All Outputs | | 0 | | ppm |
| t_{SPREAD} | Spread Spectruction Transition Time (Stabilization Time After Spread Spectrum Changes) | 7 | | 30 | ms |
| t_{OE} | Output Enable/Disable Time (All outputs) (Note 14) | | | 10 | μs |
| t_{DUTY_CYCLE} | Output Clock Duty Cycle (Measured at cross point) | 45 | 50 | 55 | % |
| t_R | Output Risetime (Measured from 175 mV to 525 mV, Figure 9) | 175 | 340 | 700 | ps |
| t_F | Output Falltime (Measured from 525 mV to 175 mV, Figure 9) | 175 | 400 | 700 | ps |
| Δt_R | Output Risetime Variation (Single-Ended) | | | 125 | ps |
| Δt_F | Output Falltime Variation (Single-Ended) | | | 125 | ps |
| Stabilization Time | Stabilization Time From Powerup $V_{DD} = 3.3\text{ V}$ | | 3.0 | | ms |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

12. VDDXD and VDDODA power pins must be shorted to power supply voltage V_{DD} and GNDXD and GNDODA ground pins must be shorted to power supply ground GND. Measurement taken from differential output on single-ended channel terminated with $R_S = 33.2\ \Omega$, $R_L = 50\ \Omega$, with test load capacitance of 2 pF and current biasing resistor set at 475 Ω . See Figure 7. Guaranteed by characterization.

13. Spread spectrum clocking enabled.

14. Output pins are tri-stated when OE is asserted LOW. Output pins are driven differentially when OE is HIGH unless device is in power down mode, $\overline{PD} = \text{Low}$.

Table 7. AC ELECTRICAL CHARACTERISTICS – PCI EXPRESS JITTER SPECIFICATIONS,

$V_{DD} = 3.3\text{ V} \pm 5\%$, $T_A = -40^\circ\text{C}$ to 85°C

| Symbol | Parameter | Test Conditions | | Min | Typ | Max | PCIe Industry Spec | Unit |
|-----------------------------|---|---|--------------|-----|------|------|--------------------|------|
| tj (PCIe Gen 1) | Phase Jitter Peak-to-Peak (Notes 16 and 19) | f = 100 MHz, 25 MHz Crystal Input Evaluation Band: 0 Hz – Nyquist (clock frequency/2) | SSOFF | | 10 | 20 | 86 | ps |
| | | | SSON (-0.5%) | | 19 | 28 | | |
| tREFCLK_HF_RMS (PCIe Gen 2) | Phase Jitter RMS (Notes 17 and 19) | f = 100 MHz, 25 MHz Crystal Input High Band: 1.5 MHz – Nyquist (clock frequency/2) | SSOFF | | 1.0 | 1.8 | 3.1 | ps |
| | | | SSON (-0.5%) | | 1.1 | 1.9 | | |
| tREFCLK_LF_RMS (PCIe Gen 2) | Phase Jitter RMS (Notes 17 and 19) | f = 100 MHz, 25 MHz Crystal Input Low Band: 10 kHz – 1.5 MHz | SSOFF | | 0.1 | 0.15 | 3.0 | ps |
| | | | SSON (-0.5%) | | 0.8 | 1.1 | | |
| tREFCLK_RMS (PCIe Gen 3) | Phase Jitter RMS (Notes 18 and 19) | f = 100 MHz, 25 MHz Crystal Input Evaluation Band: 0 Hz – Nyquist (clock frequency/2) | SSOFF | | 0.35 | 0.7 | 1.0 | ps |
| | | | SSON (-0.5%) | | 0.55 | 0.8 | | |
| tREFCLK_RMS (PCIe Gen 4) | Phase Jitter RMS (Notes 18 and 19) | f = 100 MHz, 25 MHz Crystal Input Evaluation Band: 0 Hz – Nyquist (clock frequency/2) | SSOFF | | 0.35 | 0.5 | 0.5 | ps |

15. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
16. Peak-to-Peak jitter after applying system transfer function for the Common Clock Architecture. Maximum limit for PCI Express Gen 1 is 86 ps peak-to-peak for a sample size of 10^6 clock periods.
17. RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1 ps RMS for tREFCLK_HF_RMS (High Band) and 3.0ps RMS for tREFCLK_LF_RMS (Low Band).
18. RMS jitter after applying system transfer function for the common clock architecture.
19. VDDXD and VDDODA power pins must be shorted to power supply voltage V_{DD} and GNDXD and GNDODA ground pins must be shorted to power supply ground GND. Measurement taken from differential output on single-ended channel terminated with $R_S = 33.2\ \Omega$, $R_L = 50\ \Omega$, with test load capacitance of 2 pF and current biasing resistor set at 475 Ω . See Figure 7. This parameter is guaranteed by characterization. Not tested in production.

PHASE NOISE

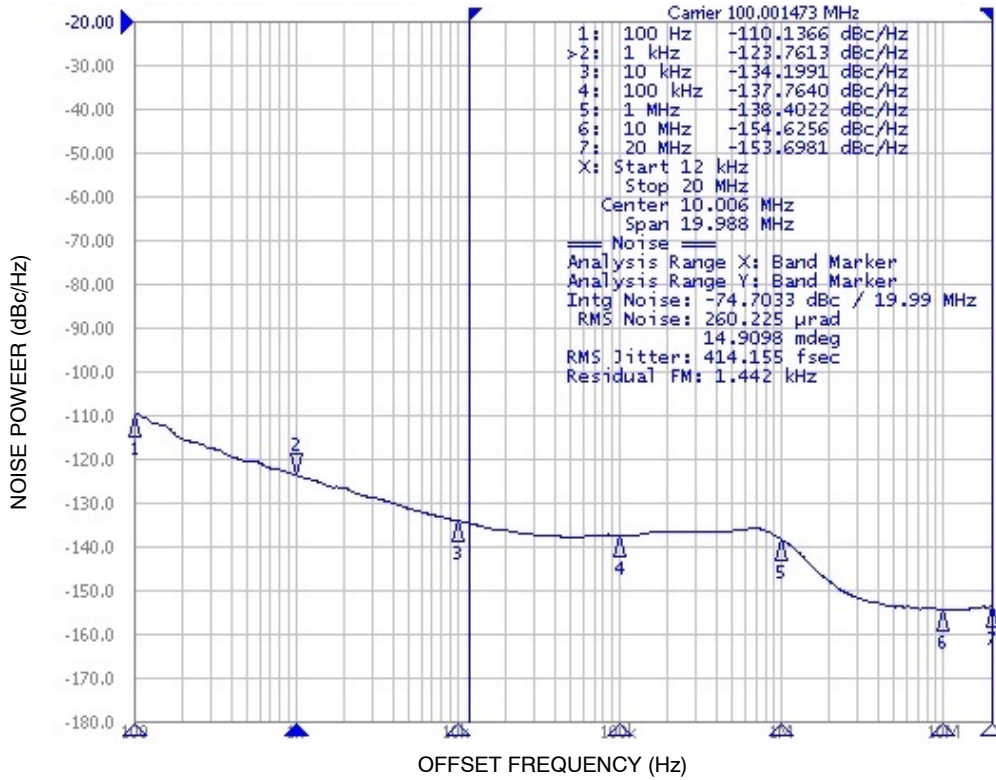


Figure 3. Typical Phase Noise Plot at 100 MHz; (f_{CLKIN} = 25 MHz Crystal , f_{CLKOUT} = 100 MHz SS OFF, RMS Phase Jitter for Integration Range 12 kHz to 20 MHz = 414 fs, Output Termination = HCSL type)

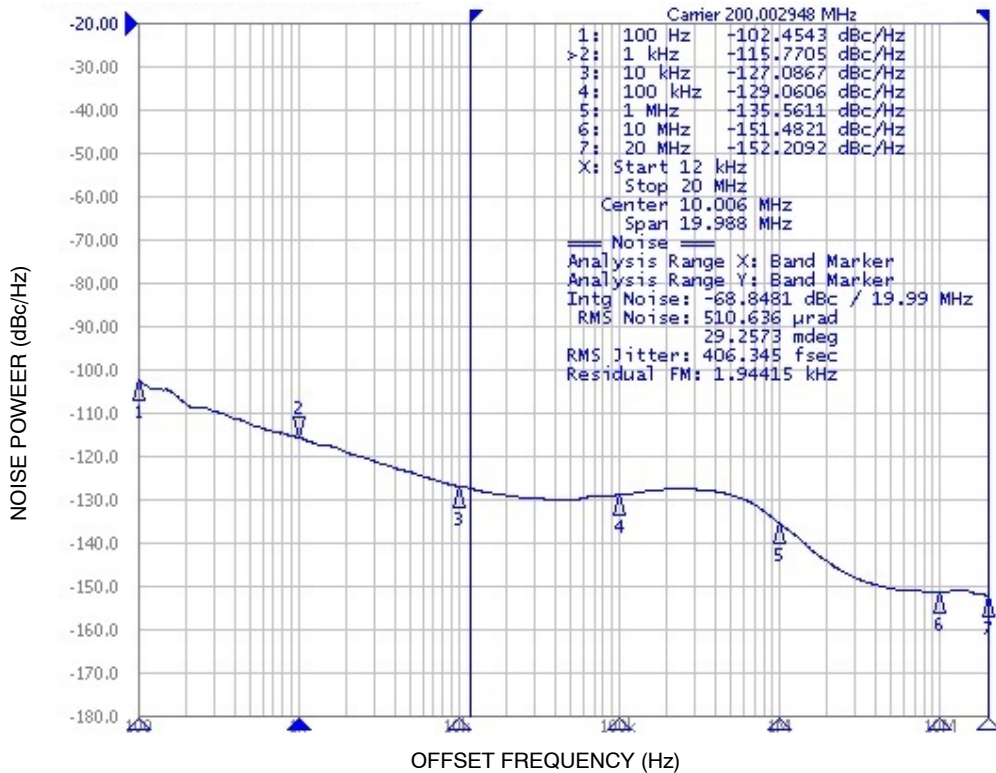


Figure 4. Typical Phase Noise Plot at 200 MHz; (f_{CLKIN} = 25 MHz Crystal , f_{CLKOUT} = 200 MHz SS OFF, RMS Phase Jitter for Integration Range 12 kHz to 20 MHz = 406 fs, Output Termination = HCSL type)

APPLICATION INFORMATION

Crystal Input Interface

Figure 5 shows the NB3N51034 device crystal oscillator interface using a typical parallel resonant crystal. The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground. These capacitors, C_1 and C_2 , need to consider the stray capacitances of the board and are used to match the nominally required crystal load capacitance C_L . A parallel crystal with loading capacitance $C_L = 18 \text{ pF}$ would use $C_1 = 26 \text{ pF}$ and $C_2 = 26 \text{ pF}$

as nominal values, assuming approximately 2 pF of stray capacitance per trace and approximately 8 pF of internal capacitance.

$$C_L = (C_1 + C_{\text{stray}} + C_{\text{in}}) / 2; C_1 = C_2$$

The frequency accuracy and duty cycle skew can be fine-tuned by adjusting the C_1 and C_2 values. For example, increasing the C_1 and C_2 values will reduce the operational frequency.

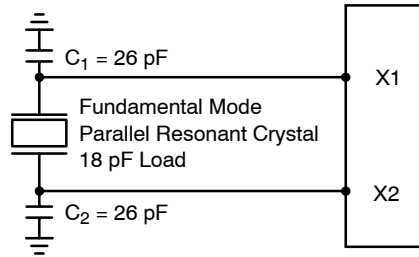


Figure 5. Crystal Interface Loading

Power Supply Filter

In order to isolate the NB3N51034 from system power supply, noise decoupling is required. The 10 μF and a 0.1 μF cap from supply pins to GND decoupling capacitor has to be connected between V_{DD} (pins 1 and 15) and GND (pins 9

and 6). It is recommended to place decoupling capacitors as close as possible to the device to minimize lead inductance.

Termination

The output buffer structure is shown in the Figure 6.

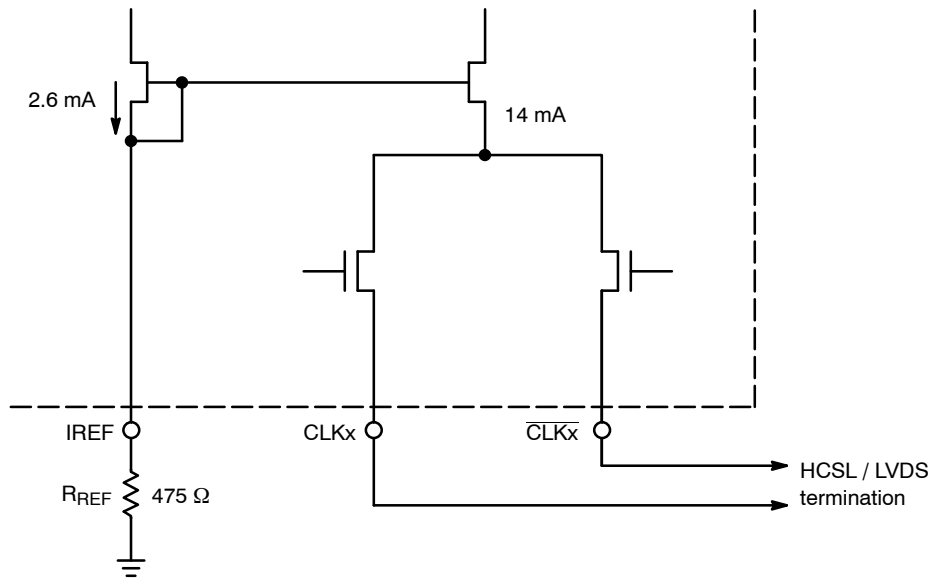


Figure 6. Simplified Output Structure

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The outputs can be terminated to drive HCSL receiver (see Figure 7) or LVDS receiver (see Figure 8). HCSL output interface requires 49.9 Ω termination resistors to GND for generating the output levels. LVDS output interface may not

require the 100 Ω near the LVDS receiver if the receiver has internal 100 Ω termination. An optional series resistor R_L may be connected to reduce the overshoots in case of impedance mismatch.

HCSL INTERFACE

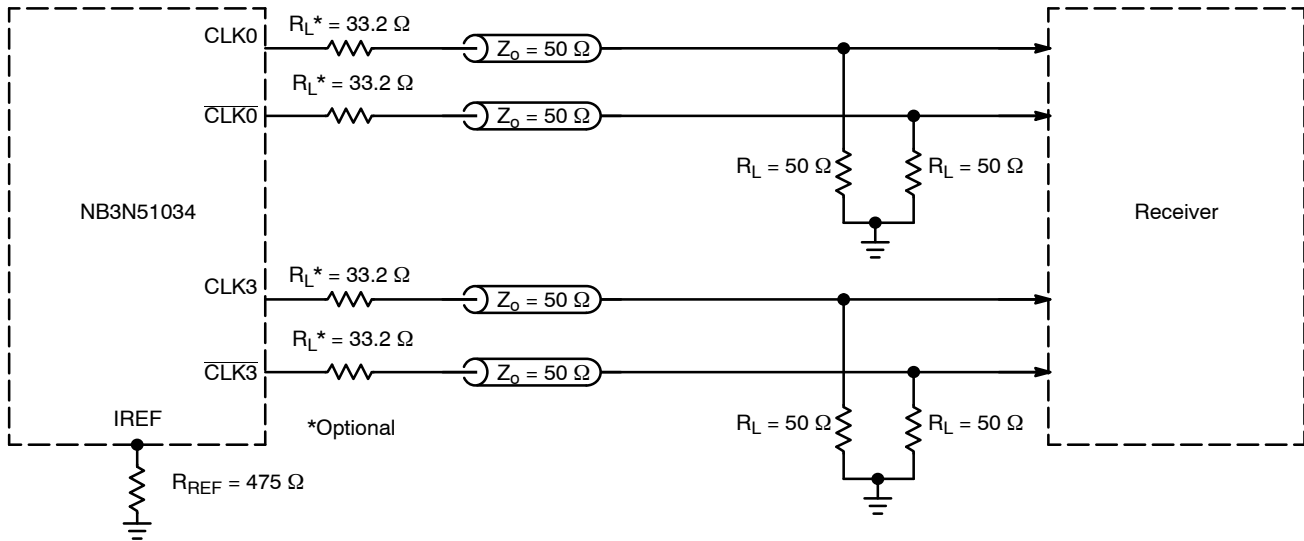


Figure 7. Typical Termination for HCSL Output Driver and Device Evaluation

LVDS COMPATIBLE INTERFACE

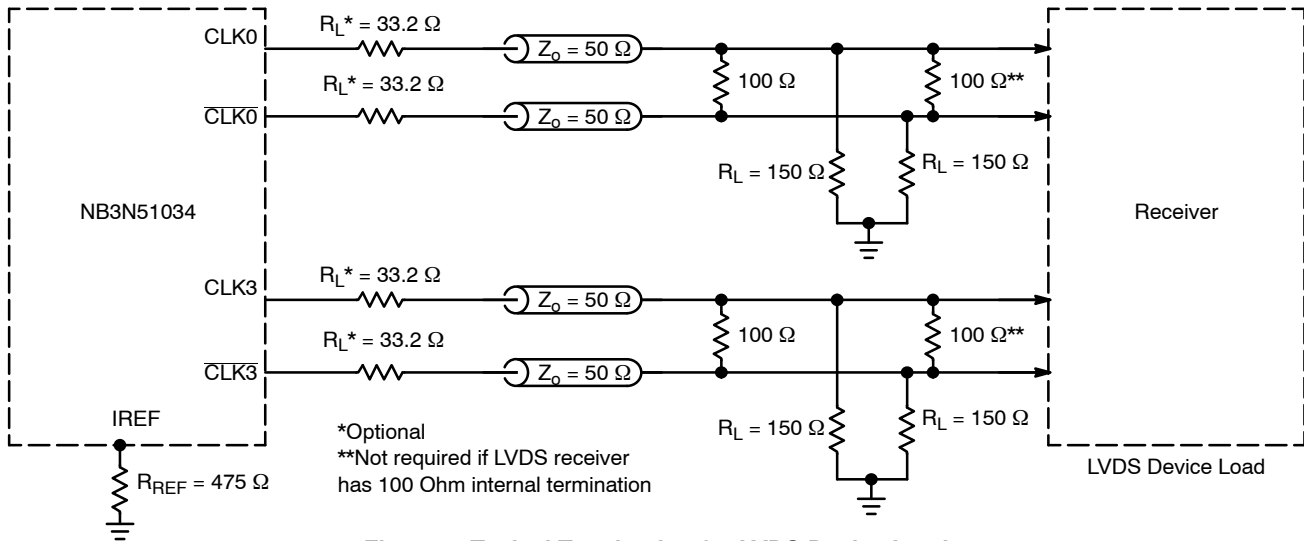


Figure 8. Typical Termination for LVDS Device Load

NB3N51034

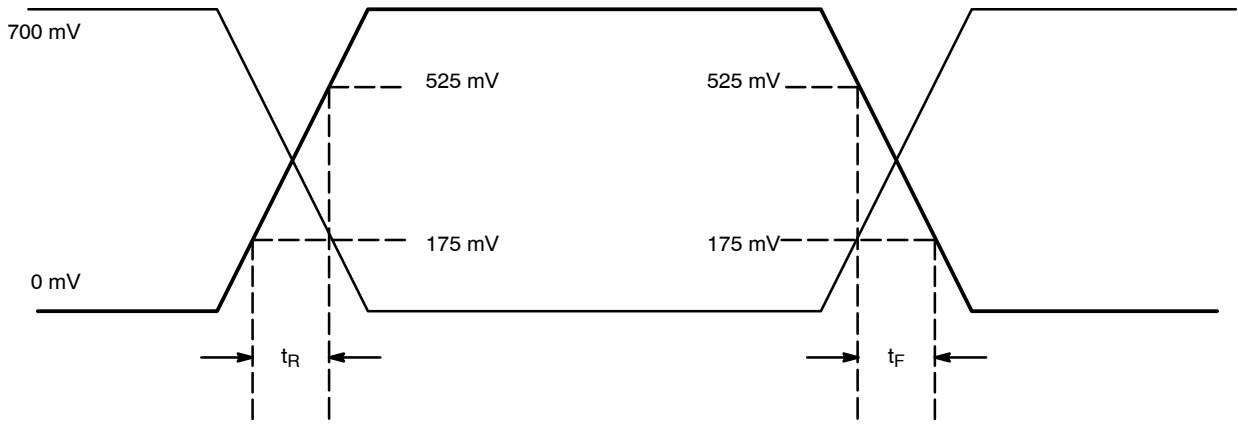


Figure 9. HCSL Output Parameter Characteristics

ORDERING INFORMATION

| Device | Package | Shipping† |
|----------------|-----------------------|--------------------|
| NB3N51034DTG | TSSOP-20 (Pb-Free) | 75 Units / Rail |
| NB3N51034DTR2G | TSSOP-20 (Pb-Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



TSSOP-20 WB
CASE 948E
ISSUE D

DATE 17 FEB 2016

SCALE 2:1



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 6.40 | 6.60 | 0.252 | 0.260 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.27 | 0.37 | 0.011 | 0.015 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |



SOLDERING FOOTPRINT



GENERIC MARKING DIAGRAM*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

| | | |
|------------------|-------------|--|
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