PE42020

Product Specification

UltraCMOS® True DC RF Switch, 0 Hz–8000 MHz

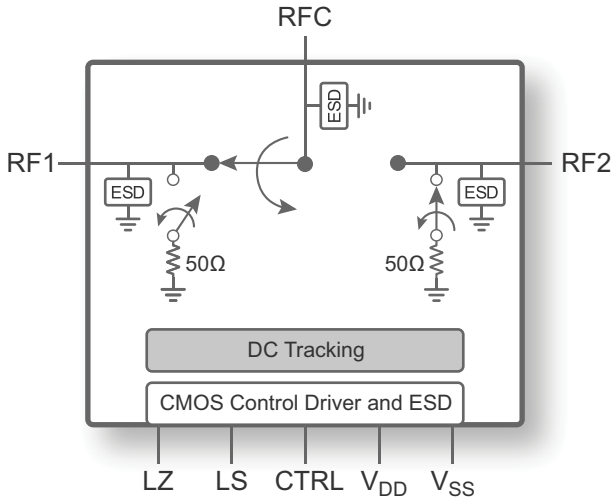
Features

- High power handling
  - 30 dBm @ DC
  - 36 dBm @ 8 GHz
- Maximum voltage (DC or AC peak): ±10V on the RF ports
- Total harmonic distortion (THD): –84 dBc
- Configurable 50Ω absorptive or open reflective switch via a single pin (LZ)
- Packaging – 20-lead 4 × 4 mm QFN

Applications

- Test and measurement
  - Signal sources
  - Communication testers
  - Spectrum analyzers
  - Network analyzers
- Automated test equipment
  - Complex combination of DC + RF/analog and digital signals

Figure 1 • *PE42020 Functional Diagram*



Product Description

The PE42020 is a HaRP™ technology-enhanced SPDT True DC RF switch that operates from zero Hertz up to 8 GHz with integrated RF, analog and digital functions. The PE42020 can accommodate up to ±10V input DC voltage on the RF ports. It can be configured as a 50Ω absorptive or an open reflective True DC switch via the single LZ pin. The PE42020 True DC RF switch delivers excellent RF performance and high power handling down to zero Hertz, making this device ideal for handling the complex combination of DC, RF/analog and digital signals in test and measurement (T&M) and automated test equipment (ATE) applications.

The PE42020 is manufactured on Peregrine's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate.

Peregrine's HaRP™ technology enhancements deliver high linearity and excellent harmonics performance. It is an innovative feature of the UltraCMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Absolute Maximum Ratings

Exceeding absolute maximum ratings listed in **Table 1** may cause permanent damage. Operation should be restricted to the limits in **Table 2**. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

ESD Precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in **Table 1**.

Latch-up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1 • *Absolute Maximum Ratings for PE42020*

Parameter/Condition	Min	Max	Unit
Positive supply voltage, V_{DD}	10	17	V
Negative supply voltage, V_{SS}	–17	–10	V
Digital input voltage (CTRL, LS, LZ)	–0.3	3.6	V
RF input power (RFC–RFX), 50Ω 0–40 MHz ≥40–8000 MHz		 **Fig. 2–Fig. 5** 38	 dBm dBm
Storage temperature range	–65	+150	°C
ESD voltage HBM, all pins(1)		1000	V
ESD voltage MM, all pins(2)		150	V
ESD voltage CDM, all pins(3)		1000	V

Notes:
1) Human body model (MIL-STD 883 Method 3015).
2) Machine model (JEDEC JESD22-A115).
3) Charged device model (JEDEC JESD22-C101).

Recommended Operating Conditions

Table 2 list the recommending operating condition for PE42020. Devices should not be operated outside the recommended operating conditions listed below.

Table 2 • *Recommended Operating Conditions for PE42020*

Parameter	Min	Typ	Max	Unit
Positive supply voltage, V_{DD} (1)	11		15	V
Negative supply voltage, V_{SS} (1)	–15		–11	V
Positive supply current, I_{DD}			3.9	mA
Negative supply current, I_{SS}	–3.8			mA
Digital input high (CTRL, LS, LZ)	1.17		3.6	V
Digital input low (CTRL, LS, LZ)	–0.3		0.6	V
RF input power, CW (RFC–RFX) (2)			Fig. 2–Fig. 5	dBm
RF input power, pulsed (RFC–RFX) (3)			Fig. 2–Fig. 5	dBm
RF input power into terminated ports, CW (RFX) (2)			Fig. 6	dBm
Max DC bias voltage at RF ports V_{DD} = +11V, V_{SS} = –11V, ≥ 0 °C V_{DD} = +15V, V_{SS} = –15V, ≥ 0 °C	 –7 –10		 +7 +10	 V V
Max voltage 0–2 MHz (V_{DD} = +11V, V_{SS} = –11V, ≥ 0 °C) 0–2 MHz (V_{DD} = +15V, V_{SS} = –15V, ≥ 0 °C) 2–8000 MHz	 –7 –10 Fig. 2–Fig. 5		 +7 +10 Fig. 2–Fig. 5	 V V V
DC current through RF active ports			80	mA
Operating temperature range	–40	+25	+85	°C

Notes:

1) To maintain proper operation of the PE42020, a mismatch between V_{DD} and V_{SS} should not exceed a maximum of 8%. A large mismatch will result in distortion appearing at the RF output at low frequencies. For example, V_{DD} = +13.85V, V_{SS} = –15V represents an 8% mismatch. |13.85-15| / (13.85+15) / 2*100 = 8%.
2) 100% duty cycle, all bands 50Ω.
3) Pulsed, 5% duty cycle of 4620 µs period, 50Ω.

Electrical Specifications

Table 3 provides the PE42020 key electrical specifications @ 25 °C, V_{DD} = +15V, V_{SS} = –15V, LZ = 0 (absorptive), 0 VDC at RF ports (Z_S = Z_L = 50Ω), unless otherwise specified.

Table 3 • *PE42020 Electrical Specifications*[1]

Parameter	Path	Condition	Min	Typ	Max	Unit
Operating frequency			0 Hz		8 GHz	As shown
Insertion loss	RFC–RFX	0 Hz 0–3 GHz 3–6 GHz 6–8 GHz		0.60 0.85 1.00 1.10	0.70 1.00 1.30 1.35	dB dB dB dB
Isolation	RFX–RFX	0–3 GHz 3–6 GHz 6–8 GHz	52 38 30	56 42 34		dB dB dB
	RFC–RFX	0–3 GHz 3–6 GHz 6–8 GHz	46 35 31	48 37 34		dB dB dB
Return loss (active and RFC ports)	RFC–RFX	0–3 GHz 3–6 GHz 6–8 GHz		20 18 15		dB dB dB
Return loss (terminated port)	RFX	0–3 GHz 3–6 GHz 6–8 GHz		23 17 16		dB dB dB
Total harmonic distortion		1 kHz (2.5 V_{PP} into 300Ω load)		–84		dBc
Input 0.1dB compression point[2]	RFC–RFX	40 MHz–8 GHz		38		dBm
Input IP2	RFC–RFX	836 MHz, 1900 MHz 2.7 GHz 4.8 GHz		115 105 90		dBm dBm dBm
Input IP3	RFC–RFX	836 MHz, 1900 MHz 2.7 GHz 4.8 GHz		62 61 55		dBm dBm dBm
Settling time		50% CTRL to 0.05 dB finallue		35	45	µs
Switching time		50% CTRL to 90% or 10% RF		10	14	µs

Notes:
1) Device is linear down to 0 Hz.
2) The input 0.1dB compression point is a linearity figure of merit. Refer to Table 2 for the RF input power (50Ω).

Table 4 provides the PE42020 key electrical specifications @ 25 °C, V_{DD} = +15V, V_{SS} = –15V, LZ = 1 (open reflective), 0 VDC at RF ports (Z_S = Z_L = 50Ω), unless otherwise specified.

Table 4 • *PE42020 Electrical Specifications*[1]

Parameter	Path	Condition	Min	Typ	Max	Unit
Operating frequency			0 Hz		8 GHz	As shown
Insertion loss	RFC–RFX	0 Hz 0–3 GHz 3–6 GHz 6–8 GHz		0.60 0.85 1.00 1.10	0.75 1.00 1.25 1.35	dB dB dB dB
Isolation	RFX–RFX	0–3 GHz 3–6 GHz 6–8 GHz	35 29 25	37 31 27		dB dB dB
	RFC–RFX	0–3 GHz 3–6 GHz 6–8 GHz	34 27 21	36 29 24		dB dB dB
Return loss (active and RFC ports)	RFC–RFX	0–3 GHz 3–6 GHz 6–8 GHz		20 19 15		dB dB dB
Total harmonic distortion		1 kHz (2.5 V_{PP} into 300Ω load)		–84		dBc
Input 0.1dB compression point[2]	RFC–RFX	40 MHz–8 GHz		38		dBm
Input IP2	RFC–RFX	836 MHz, 1900 MHz 2.7 MHz 4.8 MHz		115 105 90		dBm dBm dBm
Input IP3	RFC–RFX	836 MHz, 1900 MHz 2.7 MHz 4.8 MHz		62 61 55		dBm dBm dBm
Settling time		50% CTRL to 0.05 dB final value		35	45	µs
Switching time		50% CTRL to 90% or 10% RF		10	14	µs

Notes:
1) Device is linear down to 0 Hz.
2) The input 0.1dB compression point is a linearity figure of merit. Refer to Table 2 for the RF input power (50Ω).

Power-up/Power-down Sequence

The following power-up/power-down sequence must be followed. Failure to follow this sequence will cause permanent damage to the device.

- During the power-up sequence, V_{SS} must be turned on before V_{DD}.
- During the power-down sequence, V_{DD} must be turned off before V_{SS}.

It is recommended to turn on V_{DD} within 1 second of turning on V_{SS} during the power-up sequence and turn off V_{SS} within 1 second of turning off V_{DD} during the power-down sequence. The device is not sensitive to the timing and level of the control voltages.

Hot-switching Capability

The maximum hot switching capability of the PE42020 is 27 dBm at V_{DD} = +15V and V_{SS} = –15V; 24 dBm at V_{DD} = +11V and V_{SS} = –11V. Hot switching occurs when RF power is applied while switching between RF ports.

Control Logic

Table 5 provides the control logic truth table for the PE42020.

Table 5 • *Control Logic Truth Table for PE42020*

LS	CTRL	LZ(*)	RFC–RF1	RFC–RF2	Off Port Terminated
0	0	0	OFF	ON	Yes
0	0	1	OFF	ON	No (High–Z)
0	1	0	ON	OFF	Yes
0	1	1	ON	OFF	No (High–Z)
1	0	0	ON	OFF	Yes
1	0	1	ON	OFF	No (High–Z)
1	1	0	OFF	ON	Yes
1	1	1	OFF	ON	No (High–Z)

Note: * If LZ is pulled high, the part is configured as an open reflective switch.

Figure 2 • *Power De-rating Curve for 0 Hz–8 GHz, V_{DD} = +15V, V_{SS} = –15V, 0 VDC,–40 to 0 °C, 50Ω*

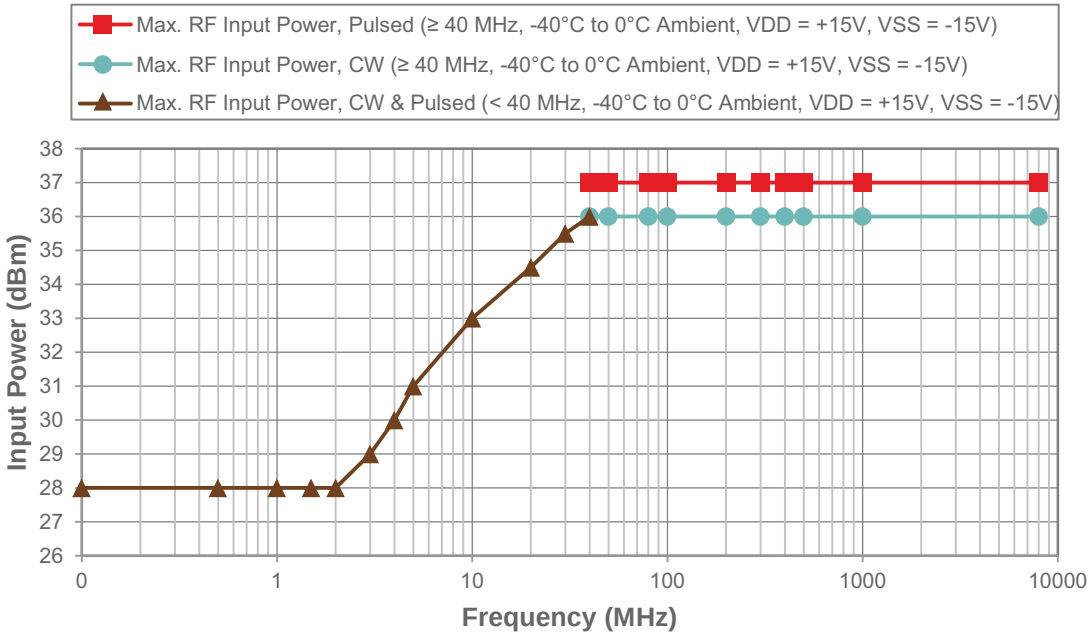


Figure 3 • *Power De-rating Curve for 0 Hz–8 GHz, V_{DD} = +15V, V_{SS} = –15V, 0 VDC, 0–85 °C, 50Ω*

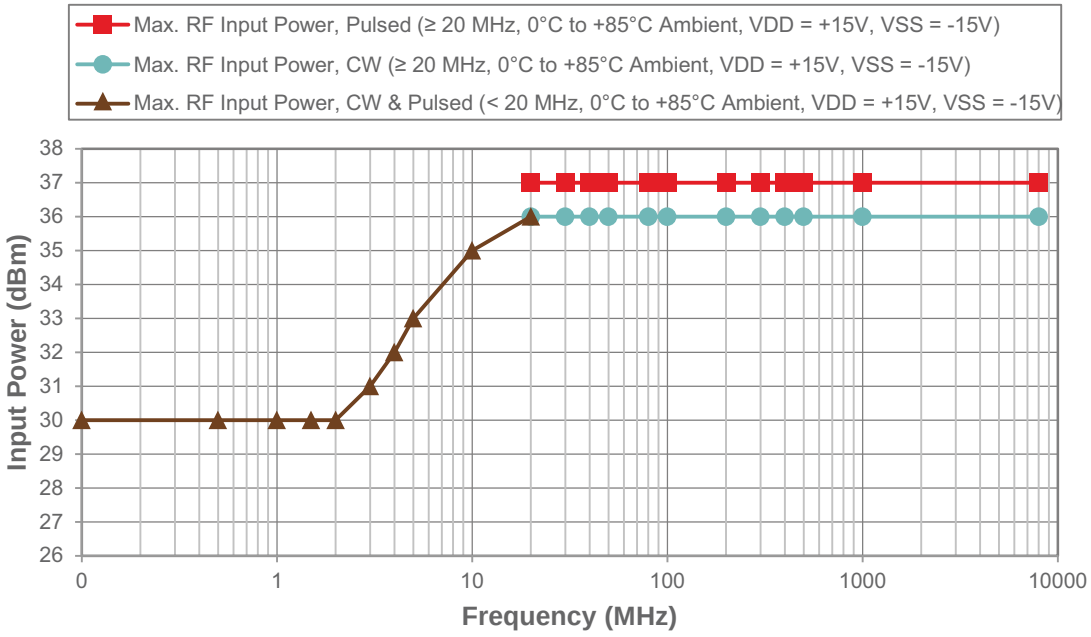


Figure 4 • *Power De-rating Curve for 0 Hz–8 GHz, V_{DD} = +11V, V_{SS} = –11V, 0 VDC, –40 to 0 °C, 50Ω*

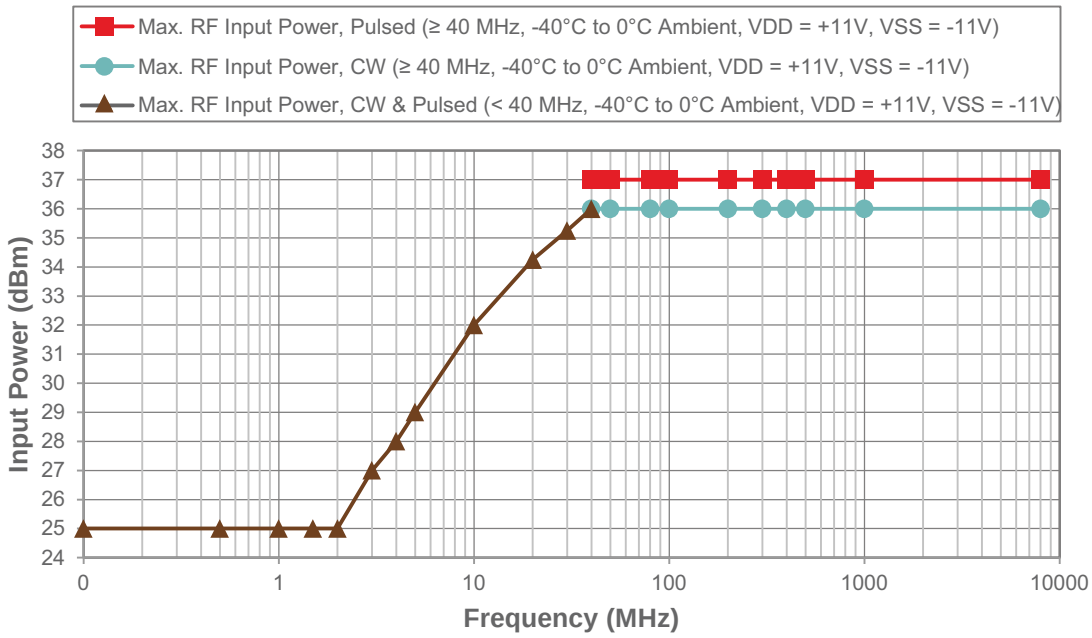


Figure 5 • *Power De-rating Curve for 0 Hz–8 GHz, V_{DD} = +11V, V_{SS} = –11V, 0 VDC, 0–85 °C, 50Ω*

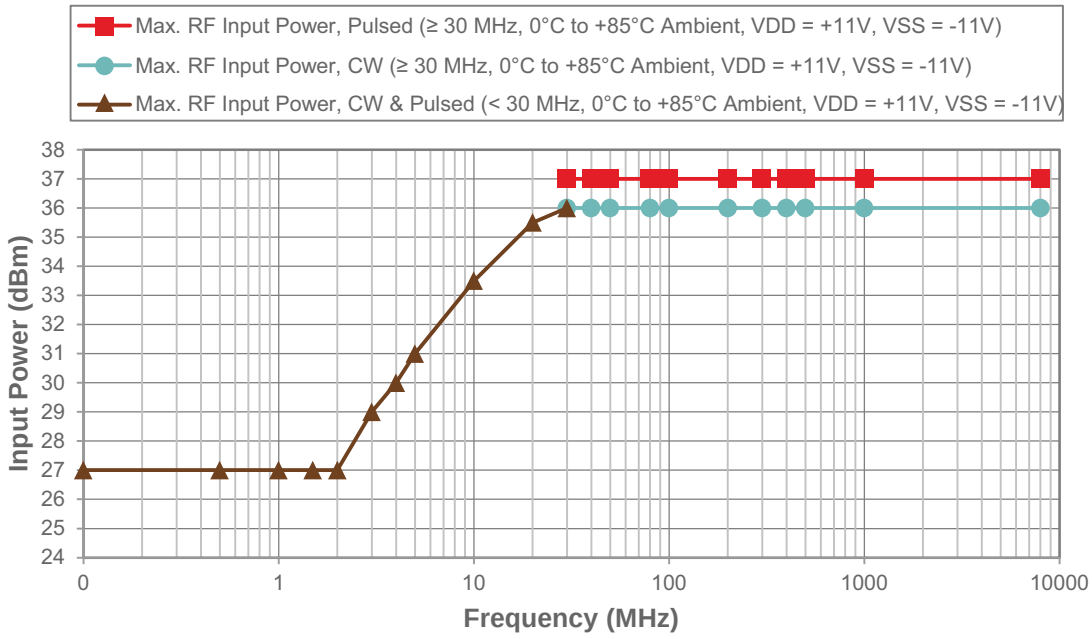
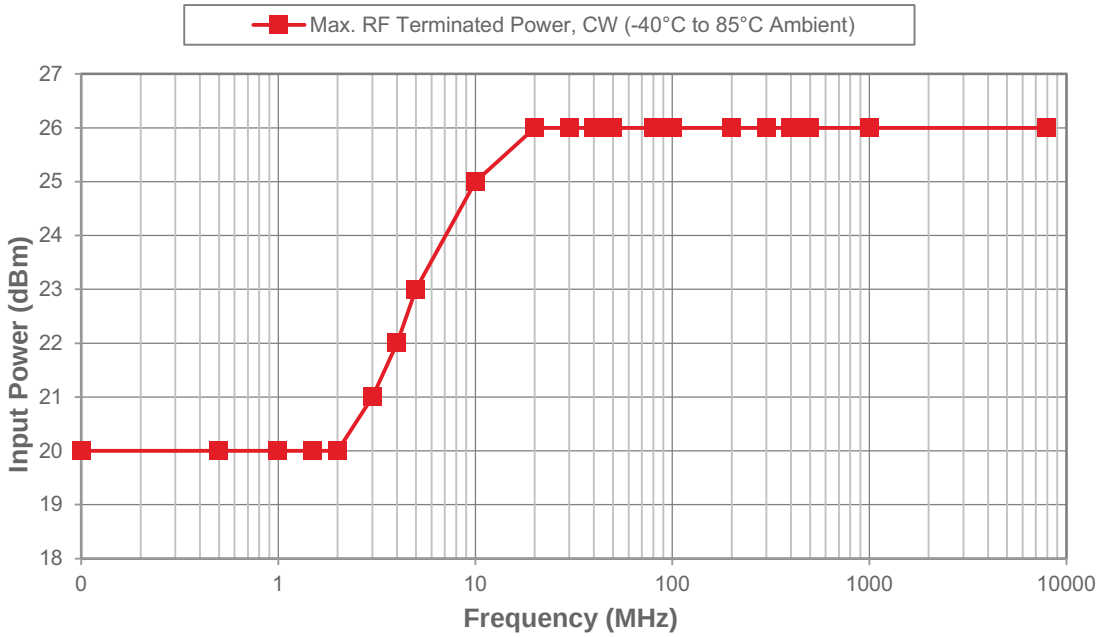


Figure 6 • *Power De-rating Curve for 0 Hz–8 GHz, Terminated Power, 0 VDC, –40 to 85 °C, 50Ω*



Performance Data

Figure 7–Figure 28 show the performance data at 25 °C, V_{DD} = +15V, V_{SS} = –15V, 0 VDC, (Z_S = Z_L = 50Ω), unless otherwise specified.

Figure 7 • *Insertion Loss vs Temperature (RFC–RFX), LZ = 0*

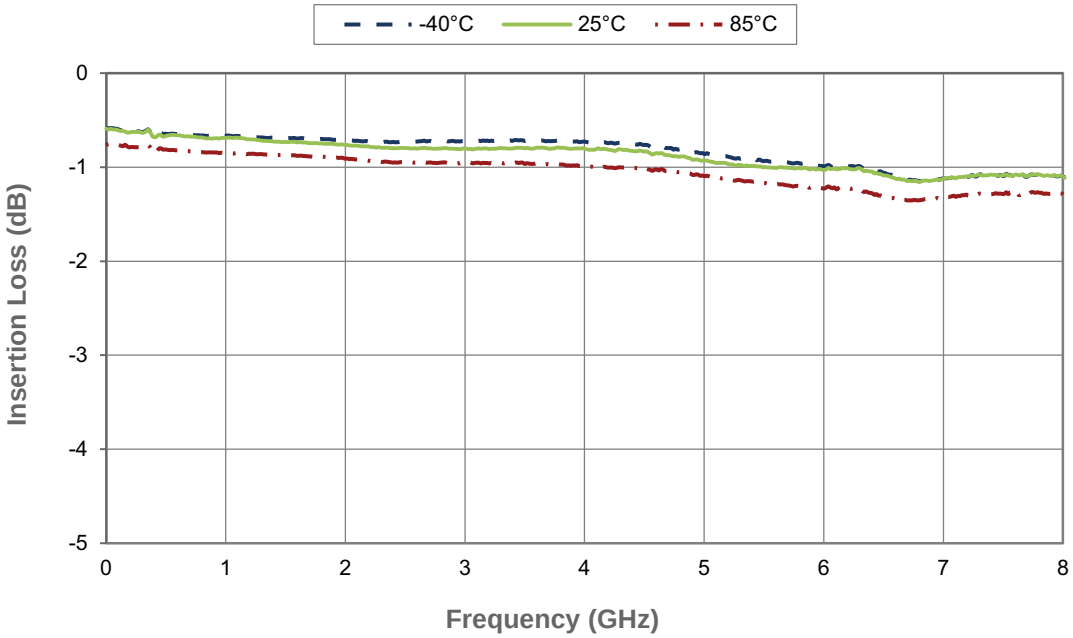


Figure 8 • *Insertion Loss vs Temperature (RFC–RFX), LZ = 1*

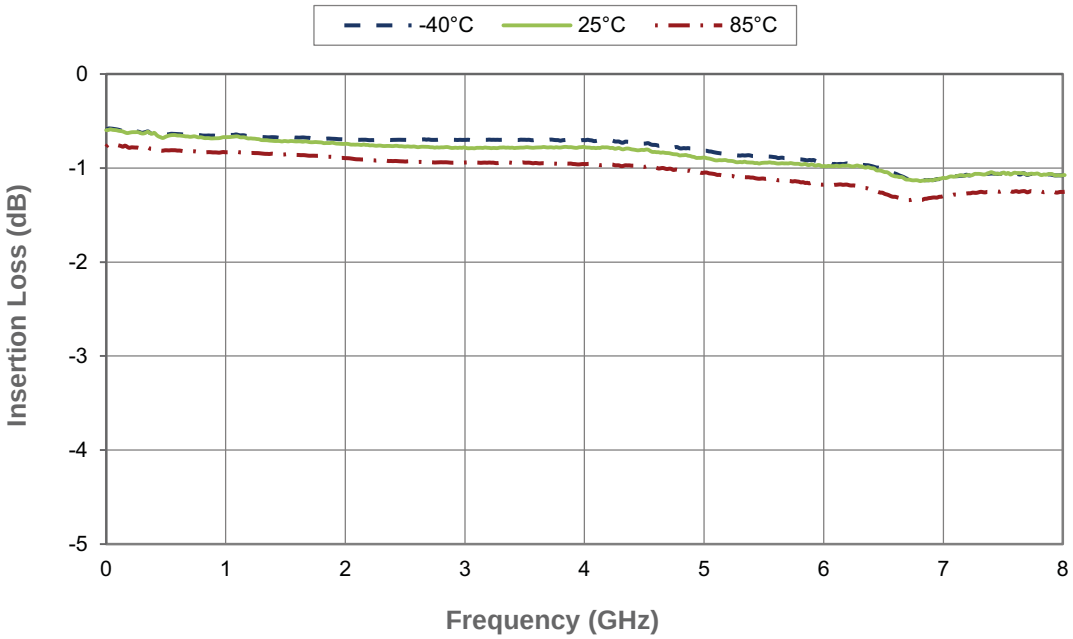


Figure 9 • *Insertion Loss vs V_{DD}/V_{SS} (RFC–RFX), LZ = 0*

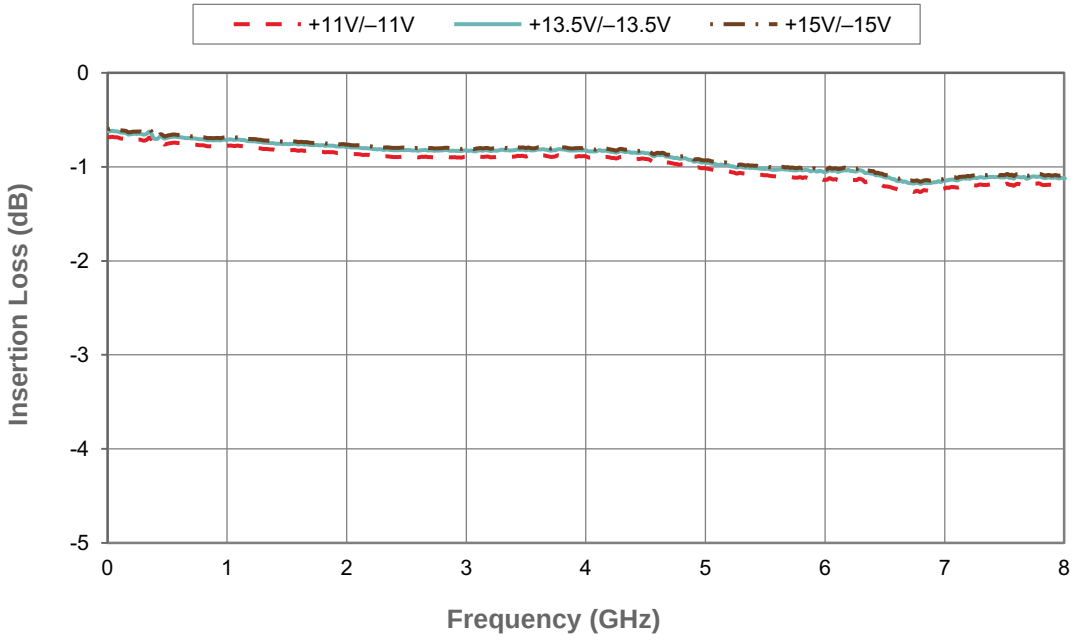


Figure 10 • *Insertion Loss vs V_{DD}/V_{SS} (RFC–RFX), LZ = 1*

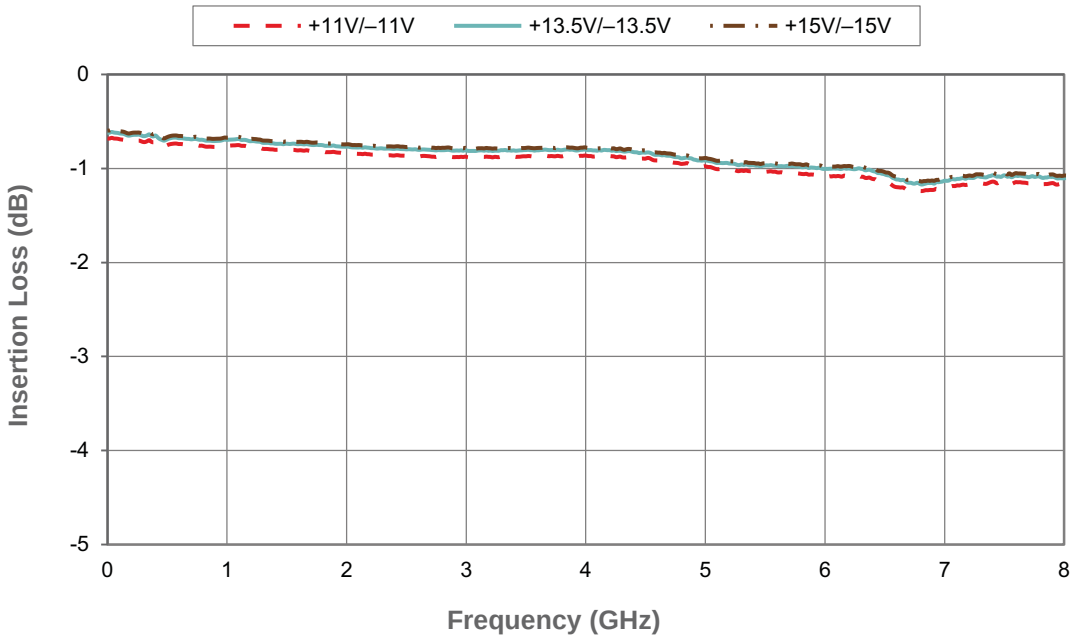


Figure 11 • *RFC Port Return Loss vs Temperature, LZ = 0*

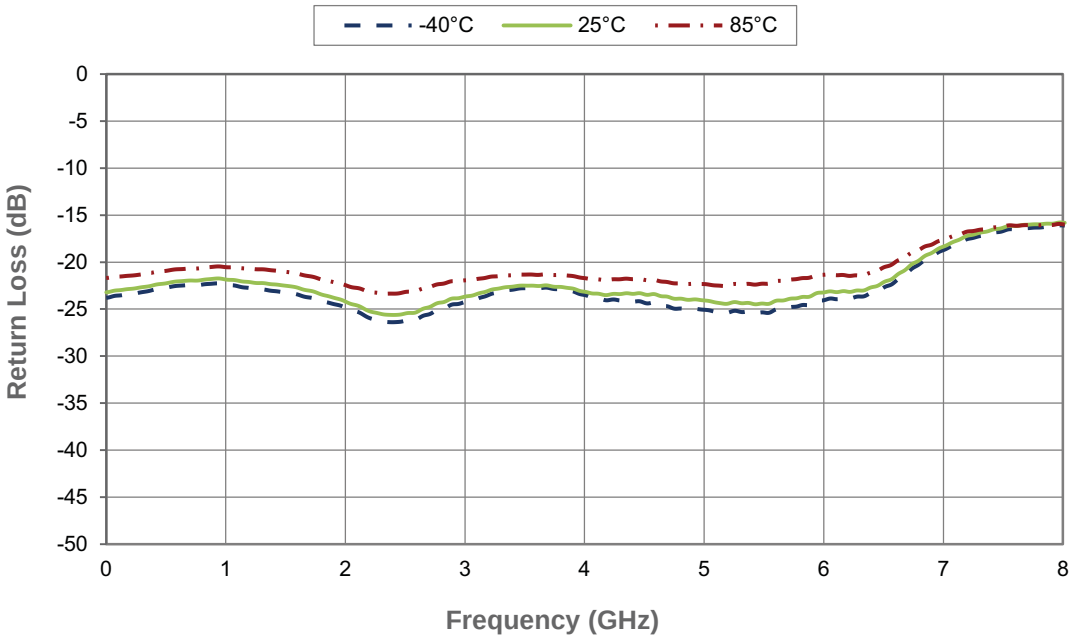


Figure 12 • *RFC Port Return Loss vs Temperature, LZ = 1*

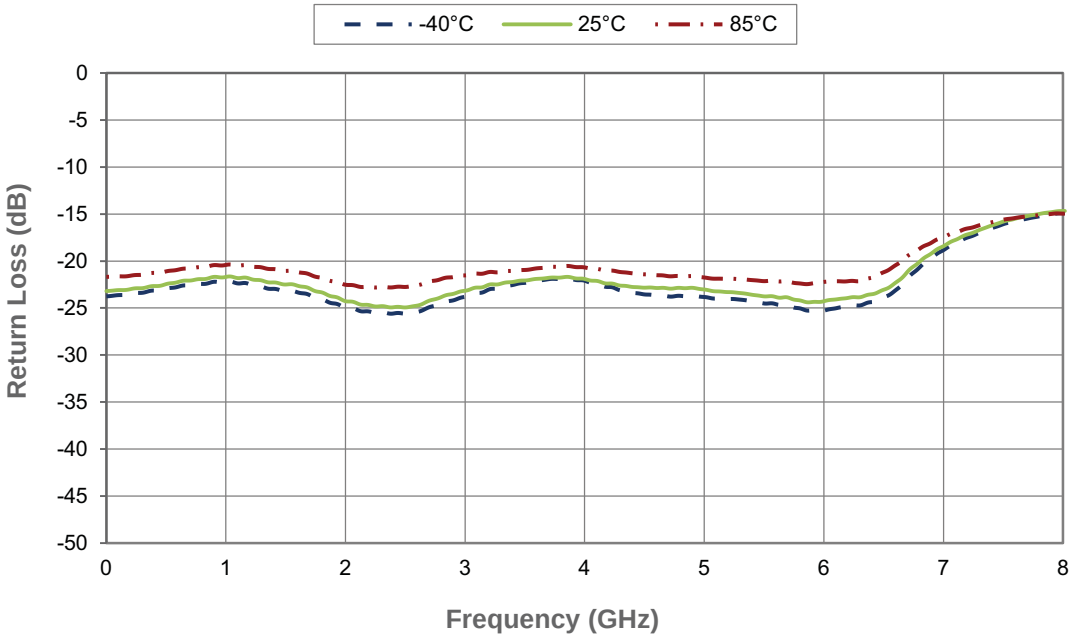


Figure 13 • *RFC Port Return Loss vs V_{DD}/V_{SS}, LZ = 0*

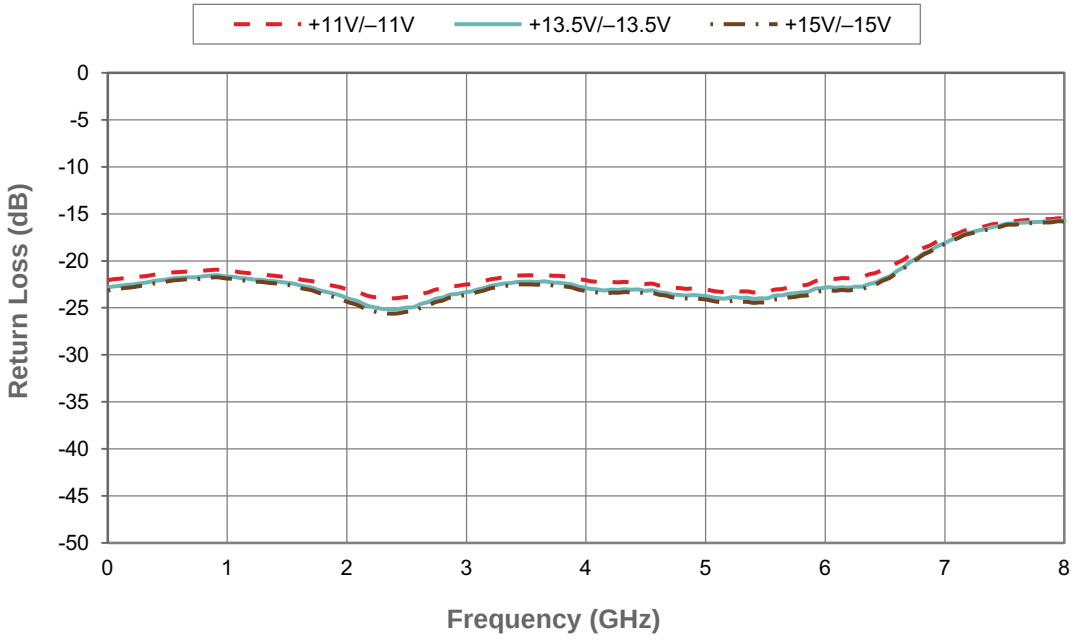


Figure 14 • *RFC Port Return Loss vs V_{DD}/V_{SS}, LZ = 1*

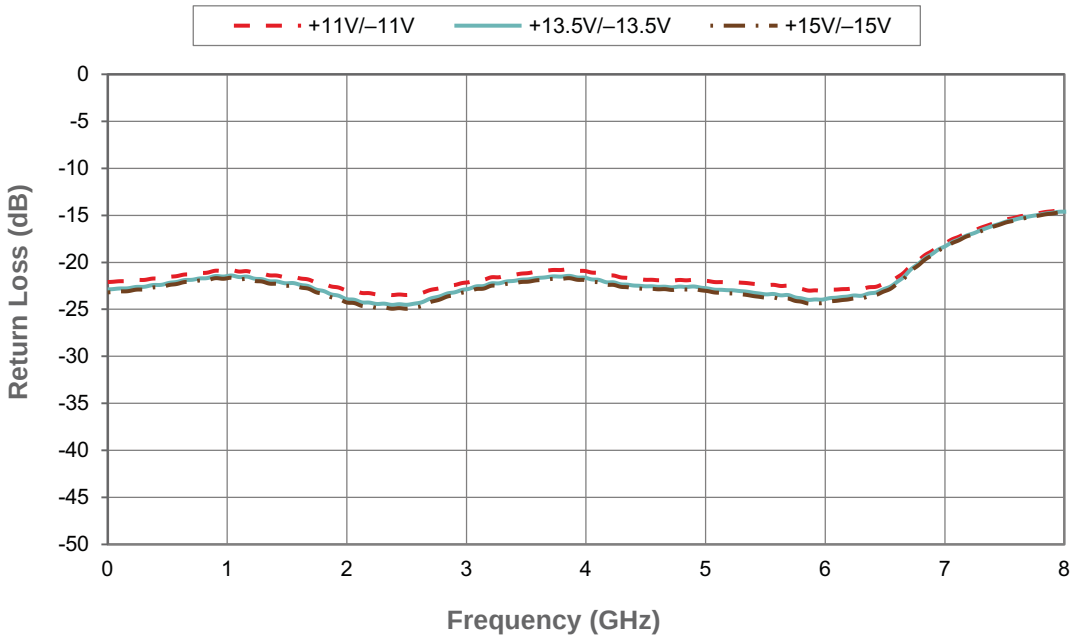


Figure 15 • *Active Port Return Loss vs Temperature, LZ = 0*

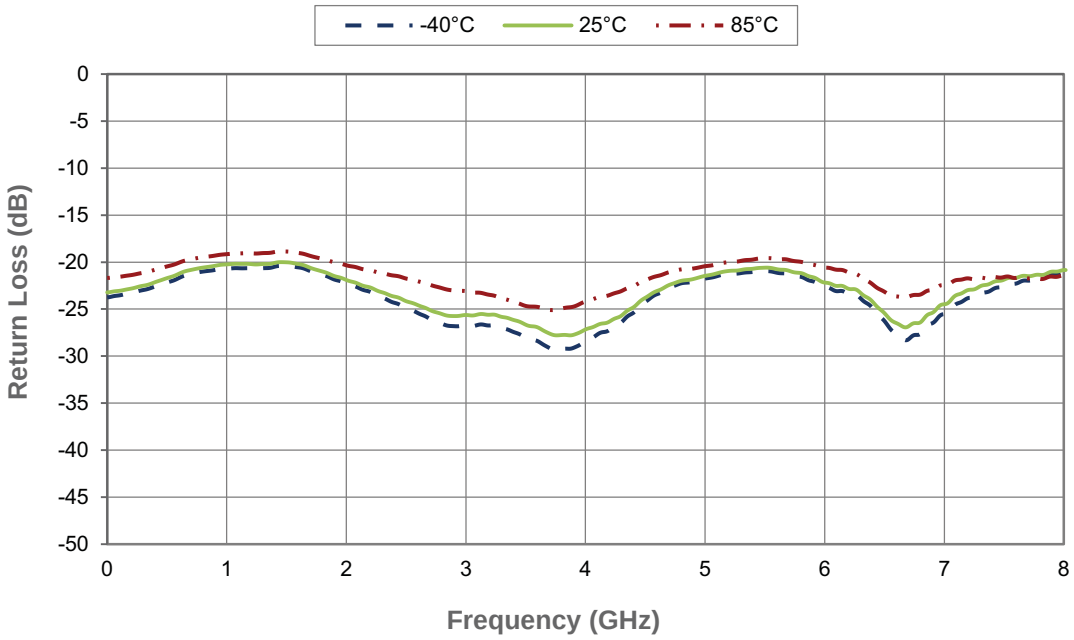


Figure 16 • *Active Port Return Loss vs Temperature, LZ = 1*

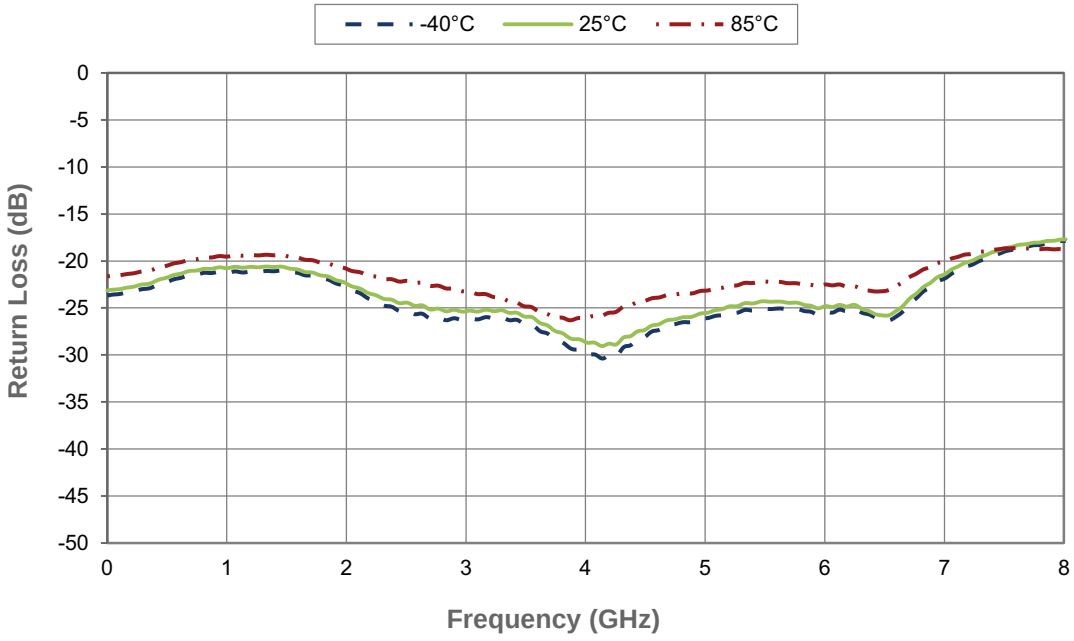


Figure 17 • *Active Port Return Loss vs V_{DD}/V_{SS}, LZ = 0*

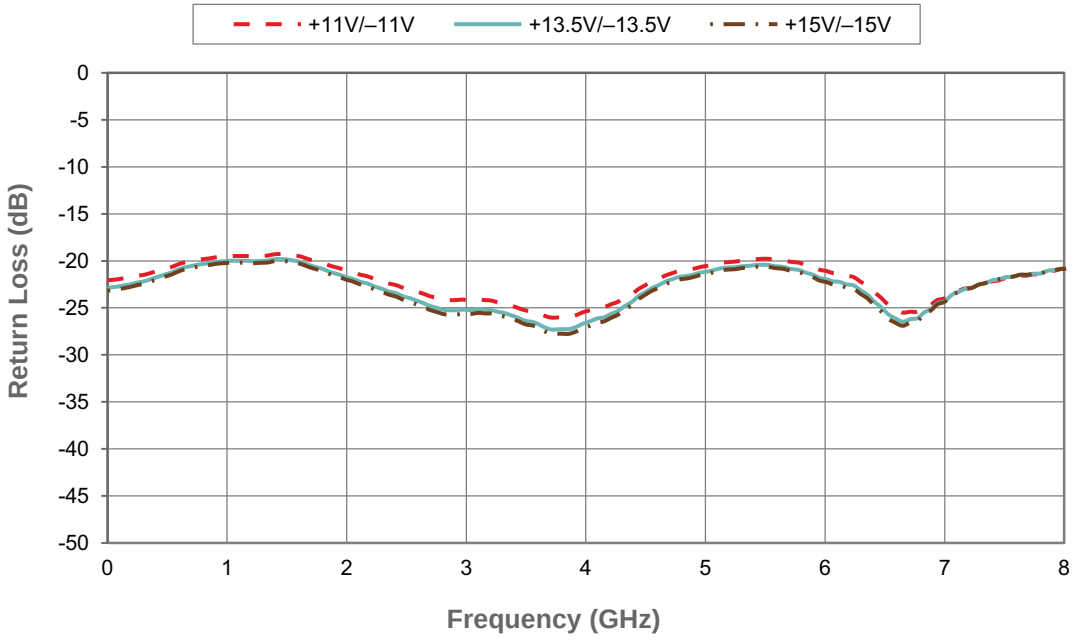


Figure 18 • *Active Port Return Loss vs V_{DD}/V_{SS}, LZ = 1*

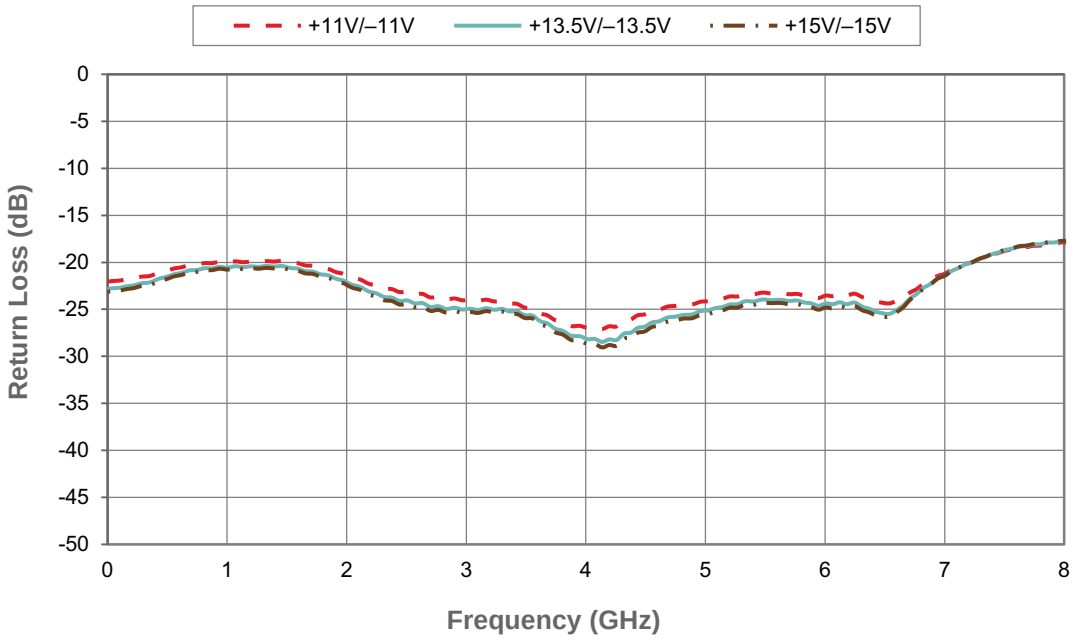


Figure 19 • *Terminated Port Return Loss vs Temperature, LZ = 0*

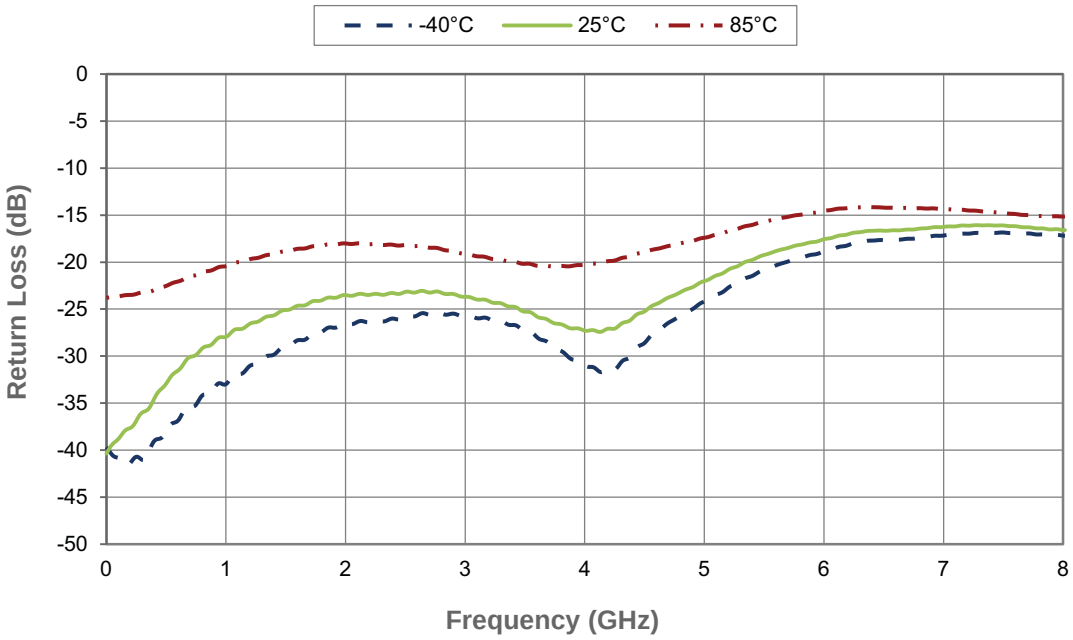


Figure 20 • *Terminated Port Return Loss vs V_{DD}/V_{SS}, LZ = 0*

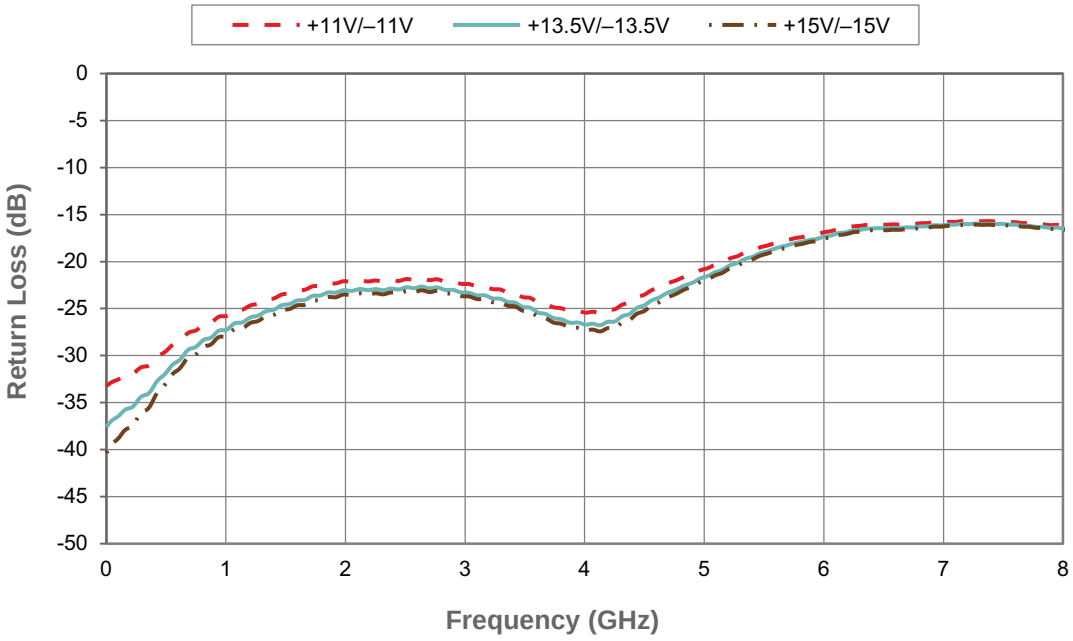


Figure 21 • *Isolation vs Temperature (RFX–RFX), LZ = 0*

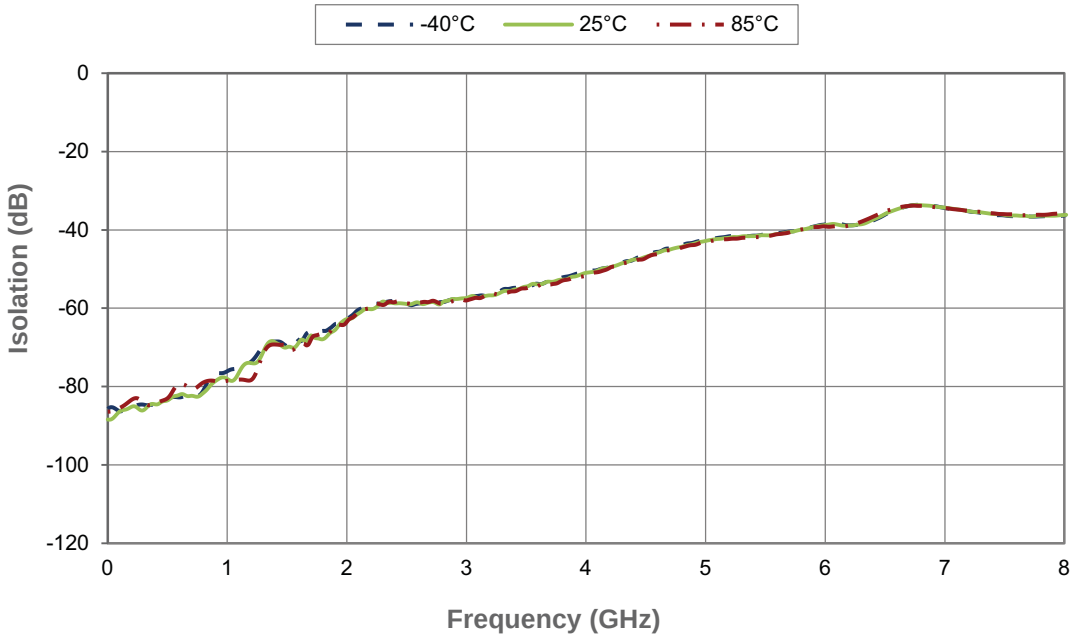


Figure 22 • *Isolation vs Temperature (RFX–RFX), LZ = 1*

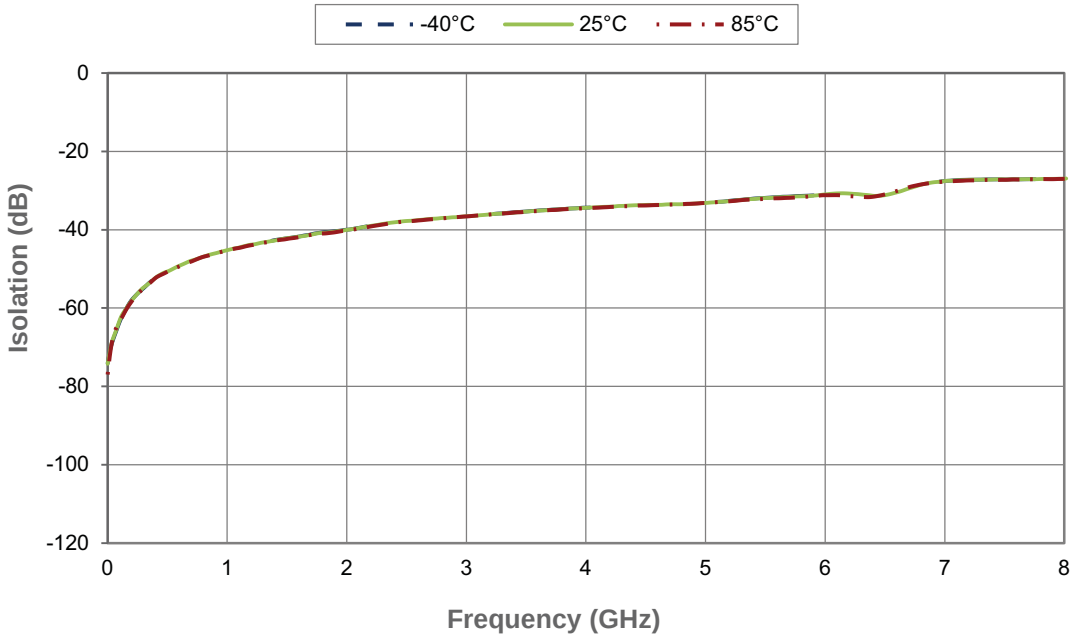


Figure 23 • *Isolation vs V_{DD}/V_{SS} (RFX–RFX), LZ = 0*

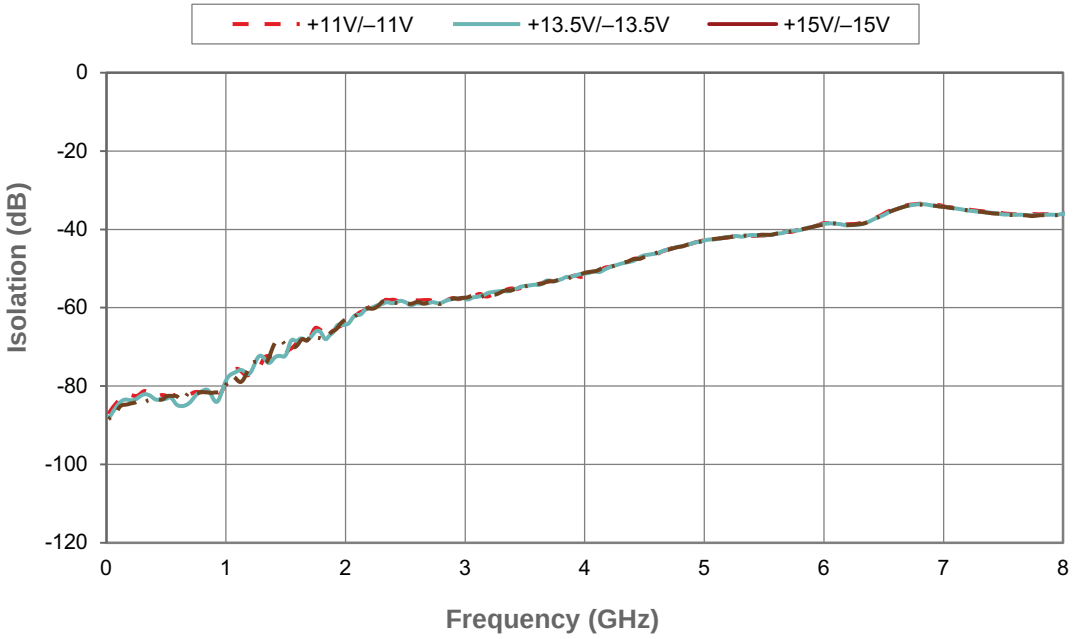


Figure 24 • *Isolation vs V_{DD}/V_{SS} (RFX–RFX), LZ = 1*

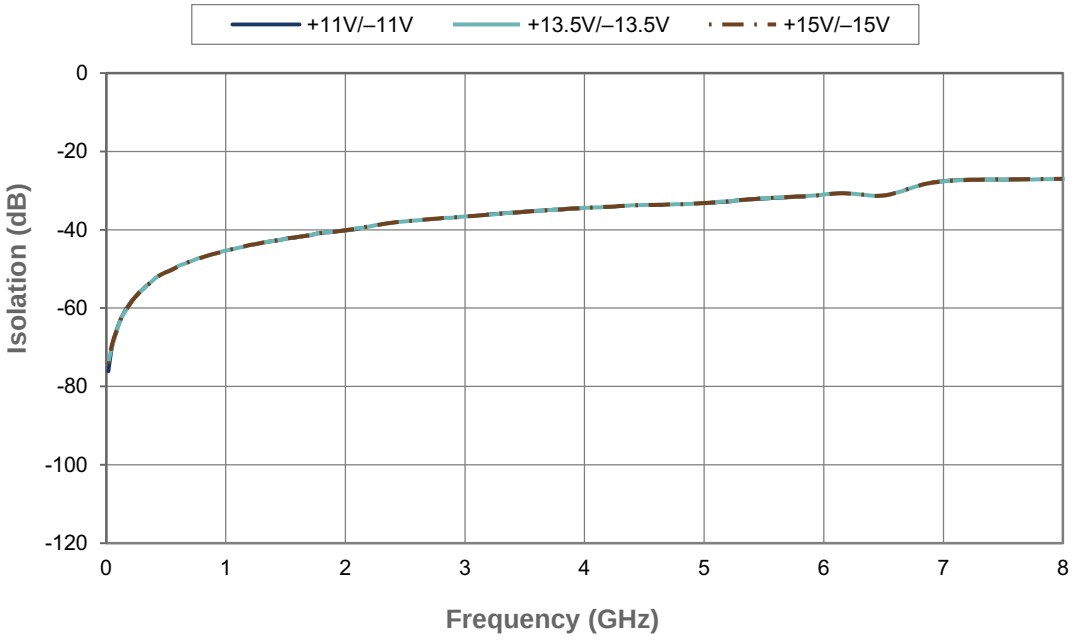


Figure 25 • *Isolation vs Temperature (RFC–RFX), LZ = 0*

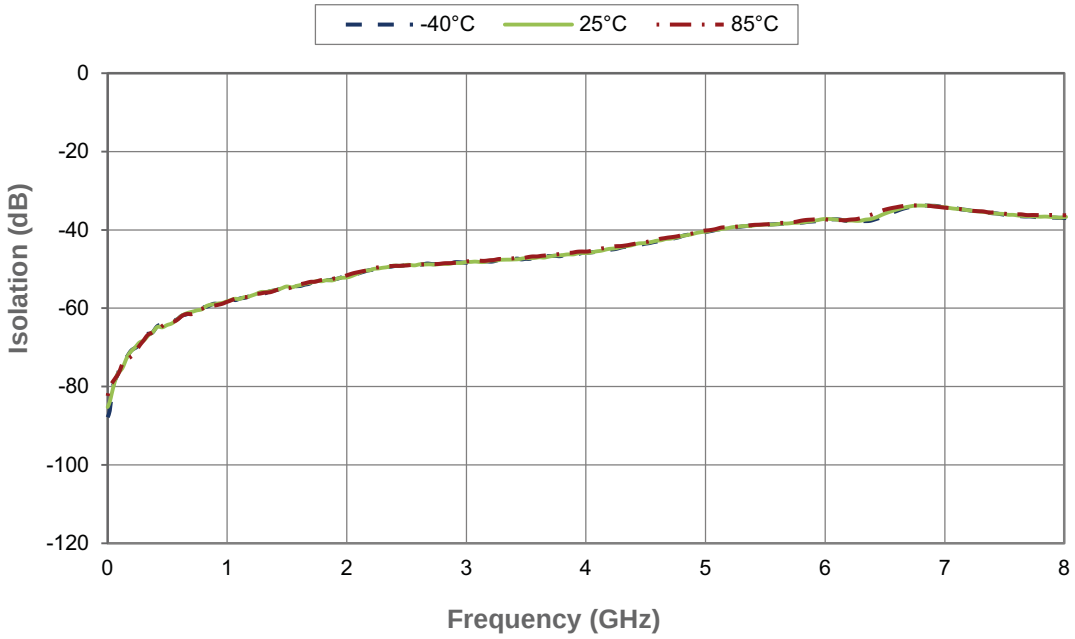


Figure 26 • *Isolation vs Temperature (RFC–RFX), LZ = 1*

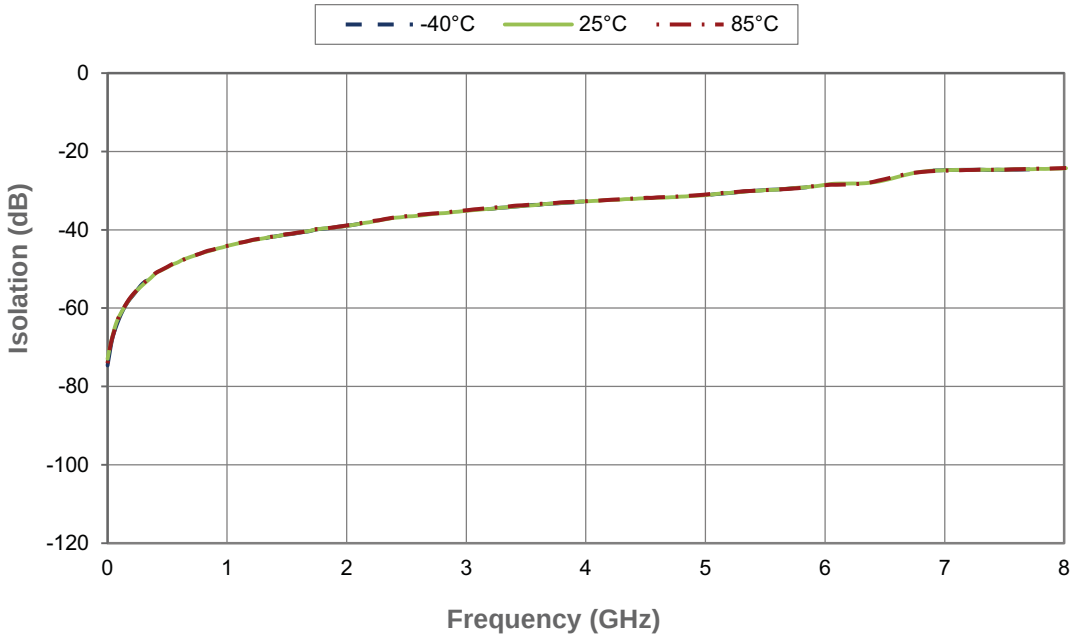


Figure 27 • *Isolation vs V_{DD}/V_{SS} (RFC–RFX), LZ = 0*

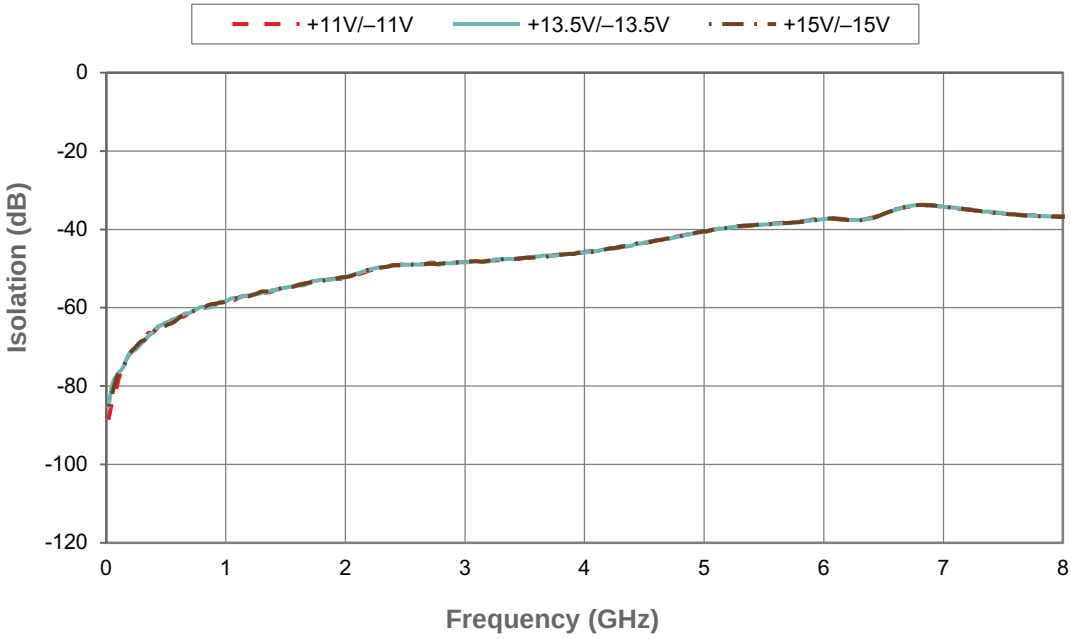
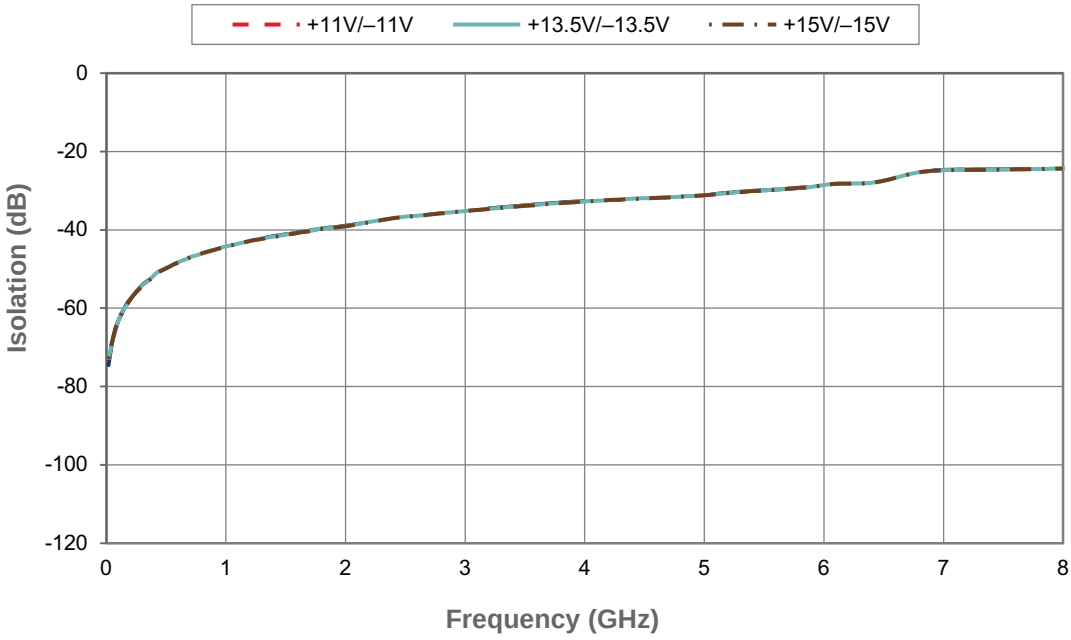


Figure 28 • *Isolation vs V_{DD}/V_{SS} (RFC–RFX), LZ = 1*



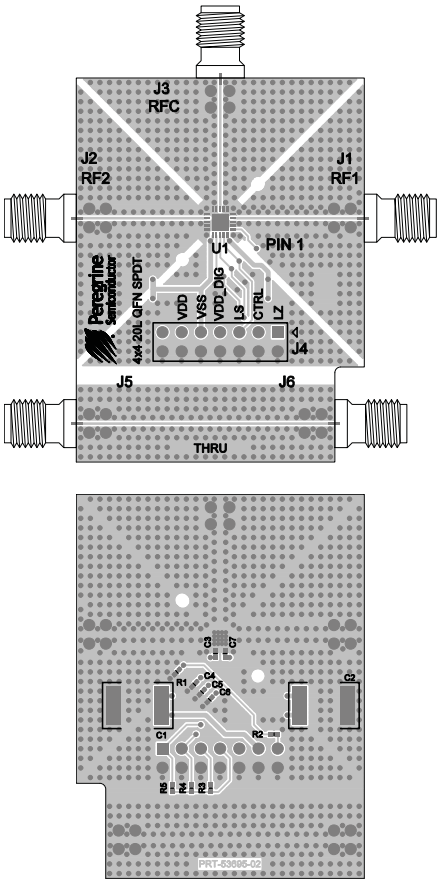
Evaluation Kit

The SPDT switch evaluation board was designed to ease customer evaluation of Peregrine's PE42020. The RF common port is connected through a 50Ω transmission line via the SMA connector, J3. RF1 and RF2 ports are connected through 50Ω transmission lines via SMA connectors J1 and J2 respectively. A 50Ω through transmission line is available via SMA connectors J5 and J6, which can be used to de-embed the loss of the PCB. J4 provides DC and digital inputs to the device.

The board is constructed of a four metal layer material with a total thickness of 62 mils. The top RF layer is Rogers 4350B material with a thickness of 6.6 mils and the ε_r = 3.66. The middle layers provide ground for the transmission lines. The transmission lines were designed using a coplanar waveguide with ground plane model using a trace width of 13 mils, trace gaps of 10.5 mils and metal thickness of 3.4 mils.

For the true performance of the PE42020 to be realized, the PCB must be designed in such a way that RF transmission lines and sensitive DC I/O traces are well isolated from one another.

Figure 29 • *Evaluation Kit Layout for PE42020*



Pin Information

This section provides pinout information for the PE42020. **Figure 30** shows the pin map of this device for the available package. **Table 6** provides a description for each pin.

Figure 30 • *Pin Configuration (Top View)*

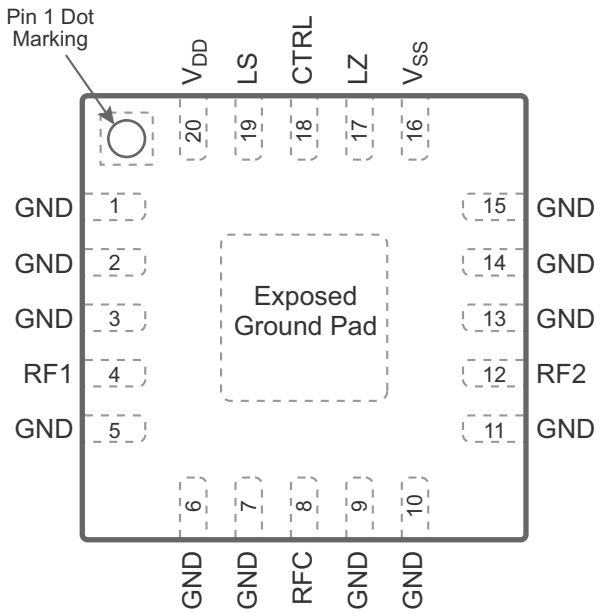


Table 6 • *Pin Descriptions for PE42020*

Pin No.	Pin Name	Description
1–3, 5–7, 9–11, 13–15	GND(*)	Ground.
4	RF1	RF port 1.
8	RFC	RF common.
12	RF2	RF port 2.
16	V_{SS}	Negative supply voltage.
17	LZ	High impedence mode.
18	CTRL	Digital control logic input for selecting ON path (see **Table 5**).
19	LS	Logic Select–used to determine the definition for the CTRL pin (see **Table 5**).
20	V_{DD}	Positive supply voltage.
Pad	GND	Exposed pad: ground for proper operation.

Note: * Ground connection. traces should be physically short and connected to the ground plane. This pin is connected to the exposed solder pad that also must be soldered to the ground plane for best performance.

Packaging Information

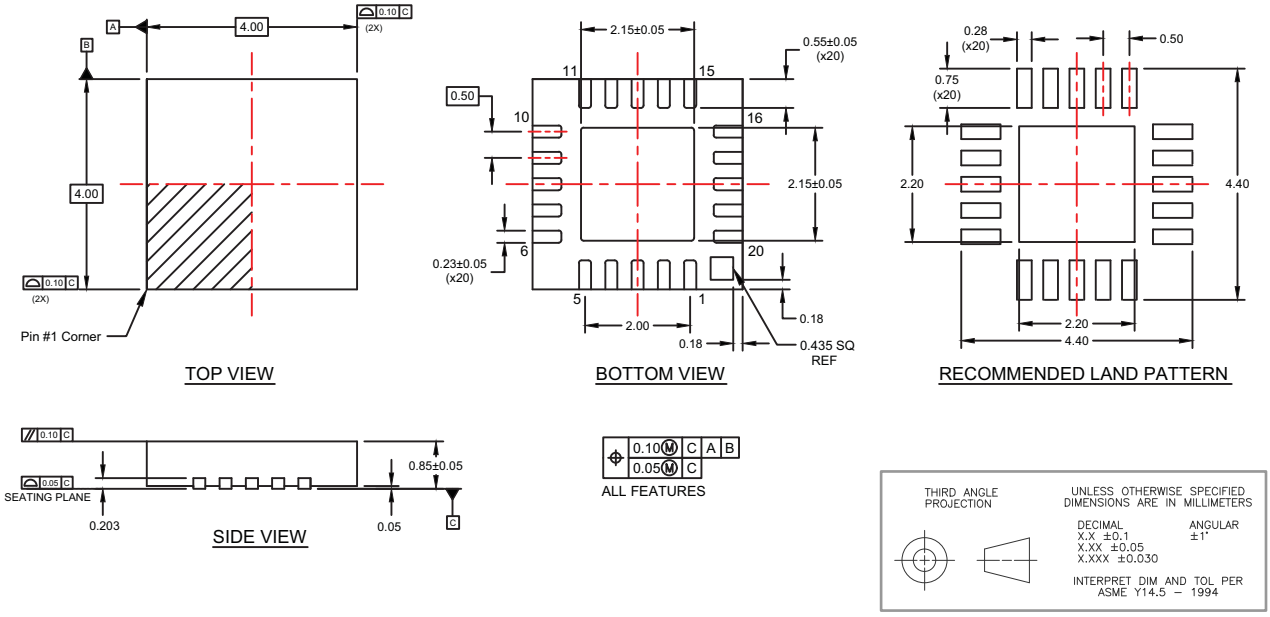
This section provides packaging data including the moisture sensitivity level, package drawing, package marking and tape-and-reel information.

Moisture Sensitivity Level

The moisture sensitivity level rating for the PE42020 in the 20-lead 4 × 4 mm QFN package is MSL3.

Package Drawing

Figure 31 • ***Package Mechanical Drawing for 20-lead 4 × 4 × 0.85 mm QFN***



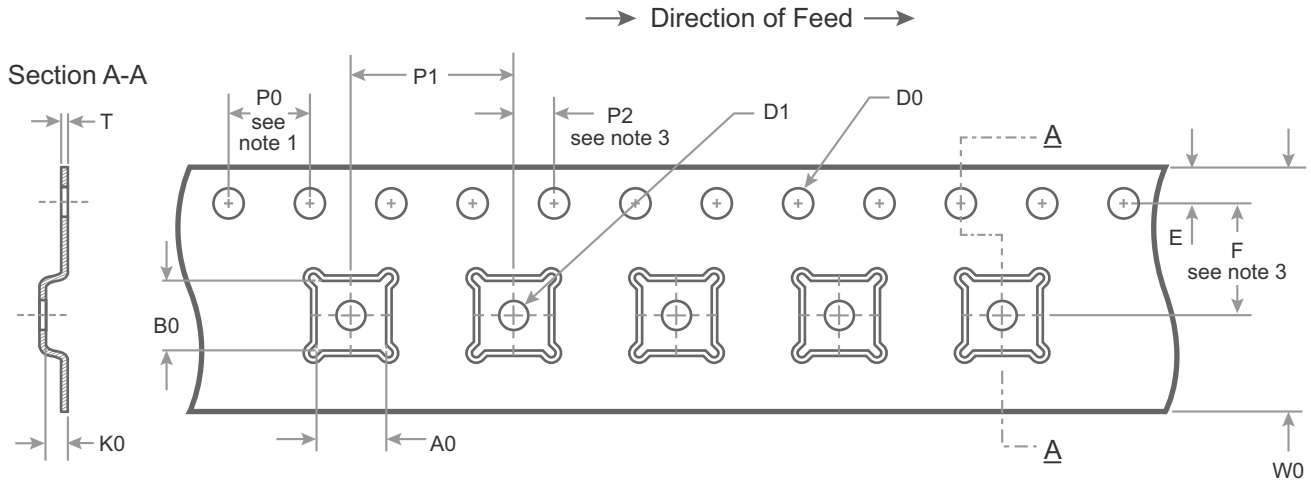
Top-Marking Specification

Figure 32 • ***Package Marking Specifications for PE42020***

● = Pin 1 indicator
YY = Last two digits of assembly year
WW = Assembly work week
ZZZZZZ = Assembly lot code (maximum six characters)

Tape and Reel Specification

Figure 33 • *Tape and Reel Specifications for 20-lead 4 × 4 × 0.85 mm QFN*

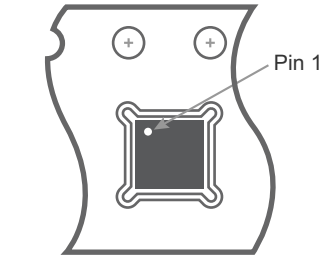


A0	4.35
B0	4.35
K0	1.10
D0	1.50 + 0.10/ -0.00
D1	1.50 min
E	1.75 ± 0.10
F	5.50 ± 0.05
P0	4.00
P1	8.00
P2	2.00 ± 0.05
T	0.30 ± 0.05
W0	12.00 ± 0.30

Notes:

1. 10 Sprocket hole pitch cumulative tolerance ±0.2
2. Camber in compliance with EIA 481
3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole

Dimensions are in millimeters unless otherwise specified



Device Orientation in Tape

Ordering Information

Table 7 lists the available ordering codes for the PE42020 as well as the available shipping methods.

Table 7 • *Order Codes for PE42020*

Order Codes	Description	Packaging	Shipping Method
PE42020A-X	PE42020 SPDT True DC RF Switch	Green 20-lead 4 × 4 mm QFN	500 units / T&R
EK42020-02	PE42020 Evaluation kit	Evaluation kit	1 / Box

Document Categories

Advance Information

The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The datasheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The datasheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

Sales Contact

For additional information, contact Sales at sales@psemi.com.

Disclaimers

The information in this document is believed to be reliable. However, Peregrine assumes no liability for the use of this information. Use shall be entirely at the user's own risk. No patent rights or licenses to any circuits described in this document are implied or granted to any third party. Peregrine's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the Peregrine product could create a situation in which personal injury or death might occur. Peregrine assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.

Patent Statement

Peregrine products are protected under one or more of the following U.S. patents: patents.psemi.com

Copyright and Trademark