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September 2014

# FCP170N60

## N-Channel SuperFET<sup>®</sup> II MOSFET

600 V, 22 A, 170 mΩ

### Features

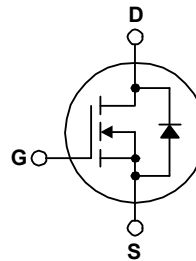
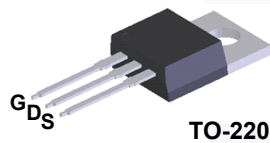
- 650 V @T<sub>J</sub> = 150°C
- Typ. R<sub>DS(on)</sub> = 150 mΩ
- Ultra Low Gate Charge (Typ. Q<sub>g</sub> = 42 nC)
- Low Effective Output Capacitance (Typ. C<sub>oss(eff.)</sub> = 190 pF)
- 100% Avalanche Tested
- RoHS Compliant

### Applications

- Telecom / Server Power Supplies
- Industrial Power Supplies
- AC-DC Power Supply

### Description

SuperFET<sup>®</sup> II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate and higher avalanche energy. Consequently, SuperFET II MOSFET is suitable for various AC/DC power conversion for system miniaturization and higher efficiency.



### Absolute Maximum Ratings

T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter	FCP170N60	Unit
V <sub>DSS</sub>	Drain to Source Voltage	600	V
V <sub>GSS</sub>	Gate to Source Voltage	- DC	±20
		- AC	±30
I <sub>D</sub>	Drain Current	- Continuous (T <sub>C</sub> = 25°C)	22
		- Continuous (T <sub>C</sub> = 100°C)	14
I <sub>DM</sub>	Drain Current	- Pulsed (Note 1)	66
E <sub>AS</sub>	Single Pulsed Avalanche Energy	(Note 2)	525
I <sub>AR</sub>	Avalanche Current	(Note 1)	5
E <sub>AR</sub>	Repetitive Avalanche Energy	(Note 1)	2.27
dv/dt	MOSFET dv/dt	(Note 3)	100
	Peak Diode Recovery dv/dt		20
P <sub>D</sub>	Power Dissipation	(T <sub>C</sub> = 25°C)	227
		- Derate above 25°C	1.82
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range	-55 to +150	°C
T <sub>L</sub>	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	°C

### Thermal Characteristics

Symbol	Parameter	FCP170N60	Unit
R <sub>θJC</sub>	Thermal Resistance, Junction to Case, Max.	0.55	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction to Ambient, Max.	40	

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCP170N60	FCP170N60	TO-220	Tube	N/A	N/A	50 units

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 10\text{ mA}, V_{GS} = 0\text{ V}, T_J = 25^\circ\text{C}$	600	-	-	V
		$I_D = 10\text{ mA}, V_{GS} = 0\text{ V}, T_J = 150^\circ\text{C}$	650	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 10\text{ mA}$ , Referenced to $25^\circ\text{C}$	-	0.67	-	$\text{V}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, T_C = 125^\circ\text{C}$	-	1.2	-	
$I_{GSS}$	Gate to Body Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	-	-	$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	2.5	-	3.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 11\text{ A}$	-	150	170	$\text{m}\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 20\text{ V}, I_D = 11\text{ A}$	-	17	-	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 380\text{ V}, V_{GS} = 0\text{ V}$ $f = 1\text{ MHz}$	-	2150	2860	pF	
$C_{oss}$	Output Capacitance		-	60	80	pF	
$C_{rss}$	Reverse Transfer Capacitance		-	2.65	-	pF	
$C_{oss (eff.)}$	Effective Output Capacitance	$V_{DS} = 0\text{ V to } 480\text{ V}, V_{GS} = 0\text{ V}$	-	190	-	pF	
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 380\text{ V}, I_D = 11\text{ A},$ $V_{GS} = 10\text{ V}$	-	42	55	nC	
$Q_{gs}$	Gate to Source Gate Charge		-	9	-	nC	
$Q_{gd}$	Gate to Drain "Miller" Charge		(Note 4)	-	11	-	nC
ESR	Equivalent Series Resistance		$f = 1\text{ MHz}$	-	0.95	-	$\Omega$

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 380\text{ V}, I_D = 11\text{ A},$ $V_{GS} = 10\text{ V}, R_g = 4.7\text{ }\Omega$	-	21	50	ns
$t_r$	Turn-On Rise Time		-	12	35	ns
$t_{d(off)}$	Turn-Off Delay Time		-	55	120	ns
$t_f$	Turn-Off Fall Time		(Note 4)	-	3.8	18

### Drain-Source Diode Characteristics

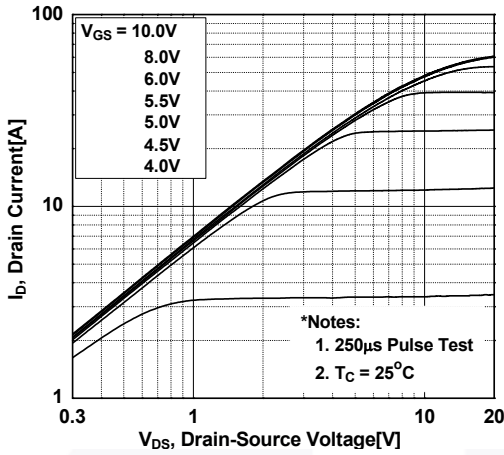
$I_S$	Maximum Continuous Drain to Source Diode Forward Current	-	-	22	A	
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current	-	-	66	A	
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_{SD} = 11\text{ A}$	-	-	1.2	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_{SD} = 11\text{ A},$	-	346	-	ns
$Q_{rr}$	Reverse Recovery Charge	$di_F/dt = 100\text{ A}/\mu\text{s}$	-	6.2	-	$\mu\text{C}$

#### Notes:

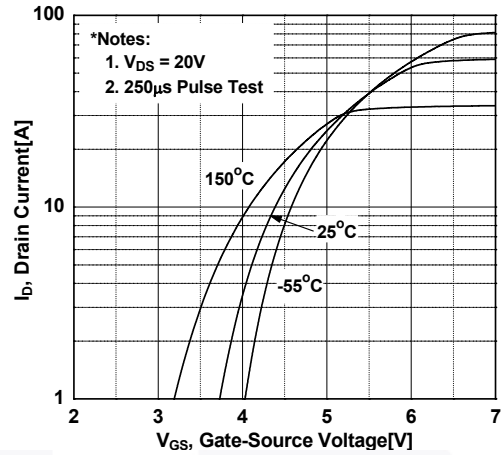
1. Repetitive rating: pulse width limited by maximum junction temperature
2.  $I_{AS} = 5\text{ A}, R_G = 25\text{ }\Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq 11\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq 380\text{ V}$ , Starting  $T_J = 25^\circ\text{C}$
4. Essentially independent of operating temperature typical characteristics

## Typical Performance Characteristics

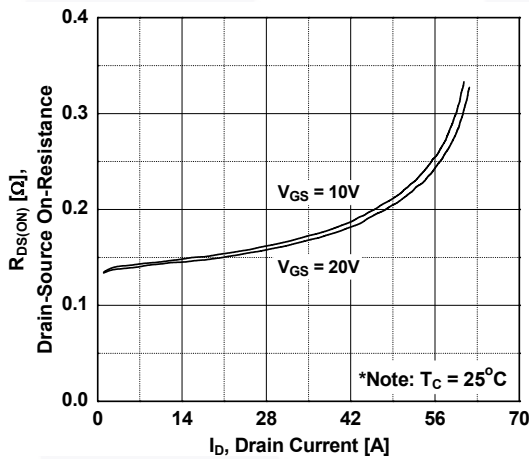
**Figure 1. On-Region Characteristics**



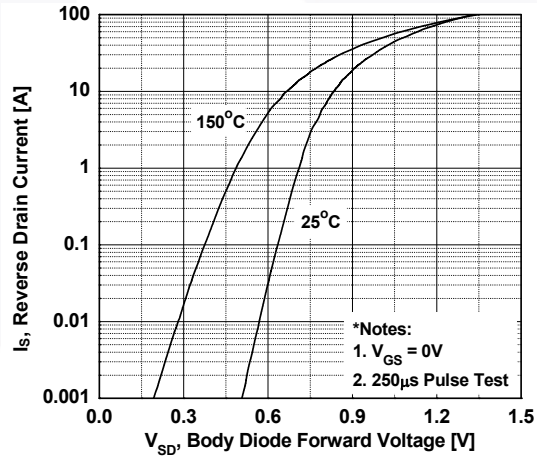
**Figure 2. Transfer Characteristics**



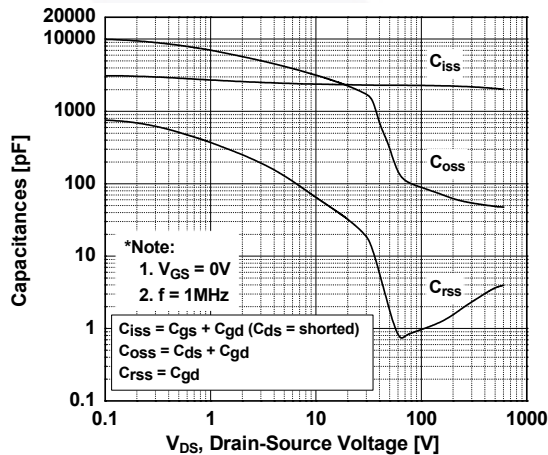
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



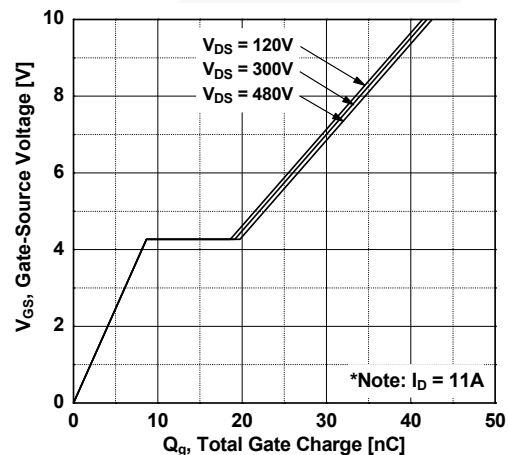
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**



**Figure 6. Gate Charge Characteristics**



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

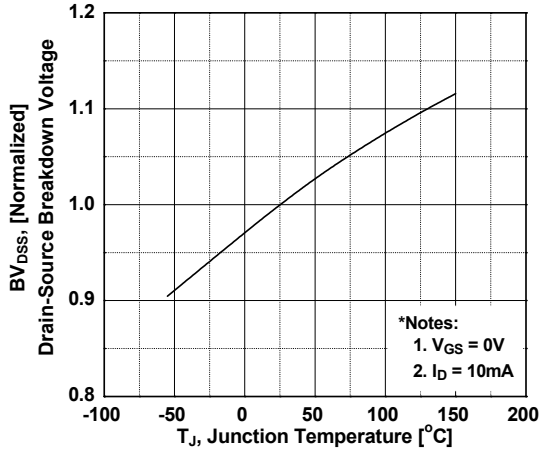


Figure 8. On-Resistance Variation vs. Temperature

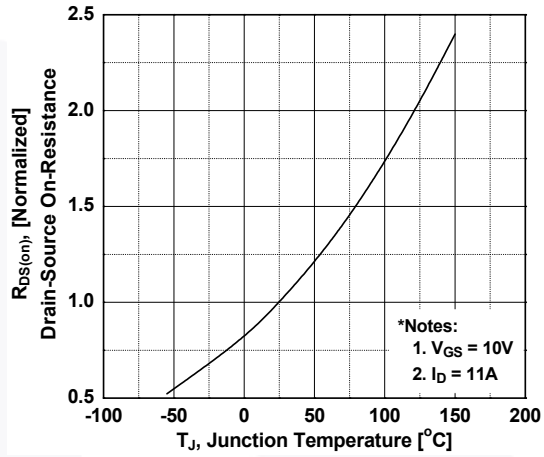


Figure 9. Maximum Safe Operating Area

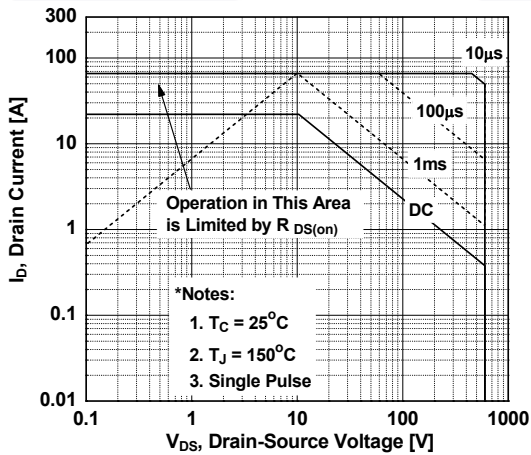


Figure 10. Maximum Drain Current vs. Case Temperature

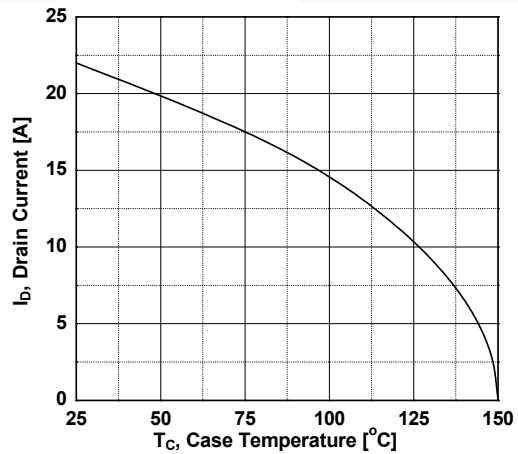
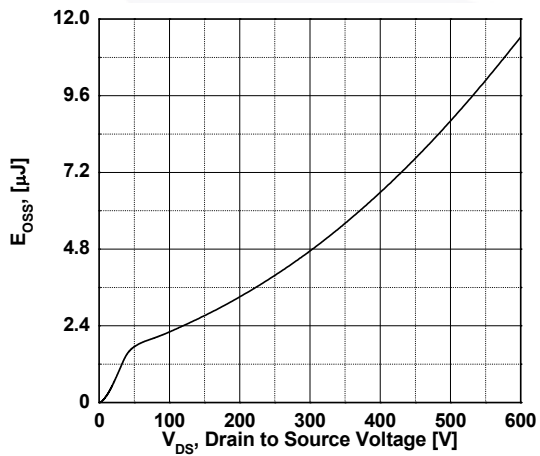
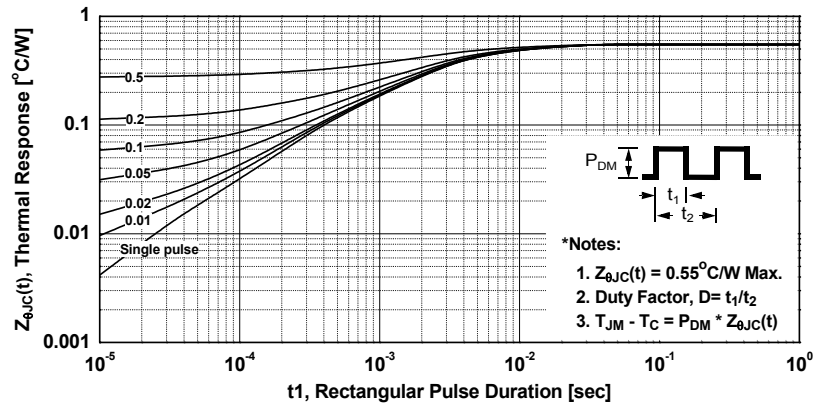


Figure 11. E\_oss vs. Drain to Source Voltage



Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve



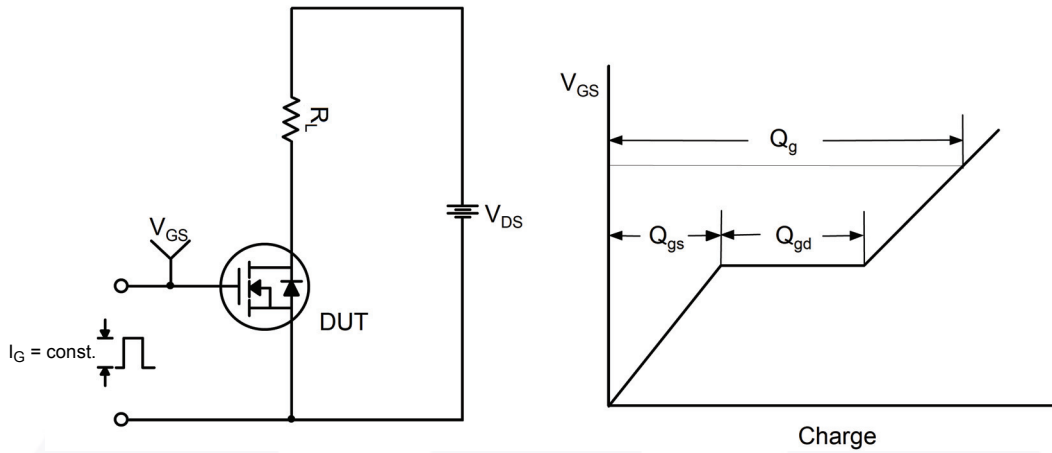


Figure 13. Gate Charge Test Circuit & Waveform



Figure 14. Resistive Switching Test Circuit & Waveforms

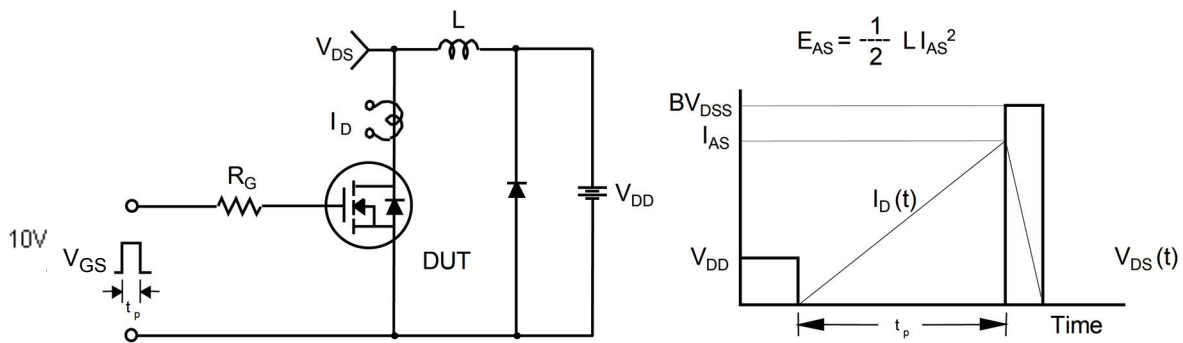


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

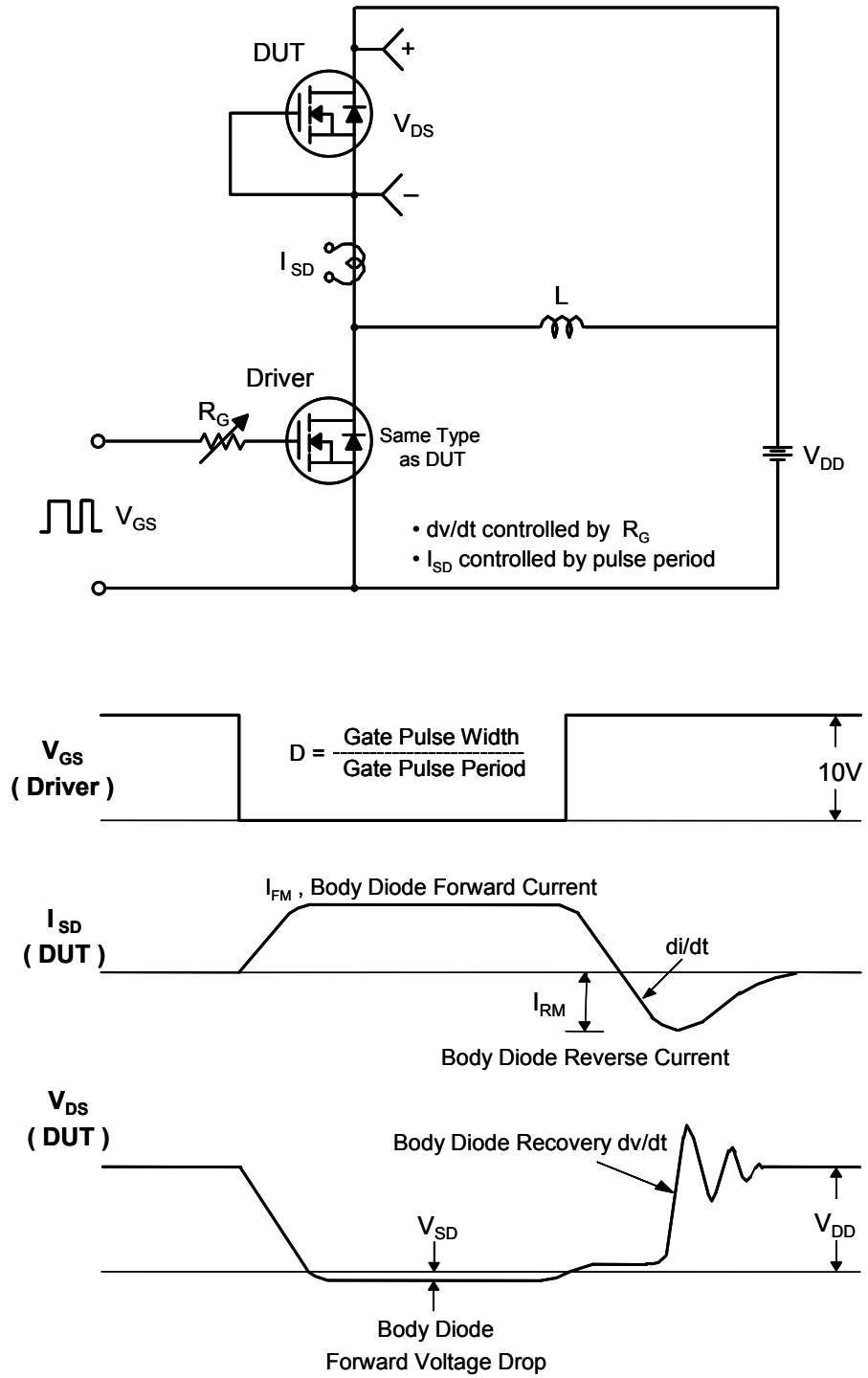


Figure 16. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms





- NOTES:
- A) REFERENCE JEDEC, TO-220, VARIATION AB
  - B) ALL DIMENSIONS ARE IN MILLIMETERS.
  - C) DIMENSIONS COMMON TO ALL PACKAGE SUPPLIERS EXCEPT WHERE NOTED [ ].
  - D) LOCATION OF MOLDED FEATURE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
  - E) DOES NOT COMPLY JEDEC STANDARD VALUE.
  - F) "A1" DIMENSIONS AS BELOW:  
 SINGLE GAUGE = 0.51 - 0.61  
 DUAL GAUGE = 1.10 - 1.45
  - G) DRAWING FILE NAME: TO220B03REV9
  - H) PRESENCE IS SUPPLIER DEPENDENT
  - I) SUPPLIER DEPENDENT MOLD LOCKING HOLES IN HEATSINK.

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