# TPS542A50 4-V to 18-V Input, 15-A, Synchronous Buck Converter With Differential Remote Sense and I^{2}C

1 Features

- Integrated 9.1-mΩ and 2.6-mΩ MOSFETs support up to 15-A output current
- 0.5-V to 5.5-V output voltage range
- Fixed-frequency voltage control mode with selectable internal compensation
- Seven selectable frequency settings from 400 kHz to 2.2 MHz
- Synchronizes to an external clock
- Fully differential remote sense
- Device configurable by analog pinstrap resistors or through I^{2}C interface
- V_{OUT} adjustment with controlled slew rate through I^{2}C from –20% to +10% in 0.25% steps
- Six selectable overcurrent limits, four soft-start slew rates, and two I^{2}C addresses
- Monotonic start-up into pre-biased outputs
- EN pin allowing for adjustable input UVLO
- Power good indicator
- 17-µA typical shutdown quiescent current draw
- Selectable FCCM or PFM for light load efficiency
- –40 to +150°C operating junction temperature
- 4-mm × 4.5-mm VQFN package
- Create a custom design using the TPS542A50 with the WEBENCH® Power Designer
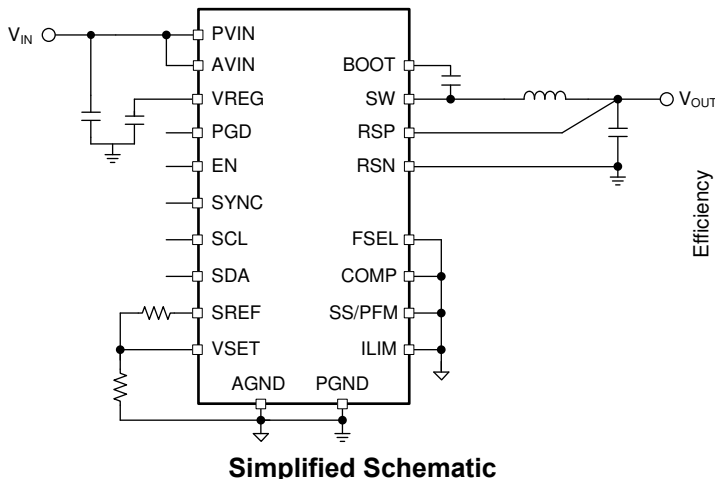
2 Applications

- Enterprise storage, SSD
- ASIC, SoC, FPGA, DSP core, and I/O rails
- Wired networking switches and routers
- Industrial machines and machine tools

3 Description

The TPS542A50 is a high-efficiency synchronous buck converter with differential remote sense and I^{2}C. This device features fixed-frequency, voltage-control mode with pinstrap selectable internal compensation for reduced system cost and complexity. The PWM can be synchronized to an external clock through the SYNC pin. Other key features include PFM for high light load efficiency, low shutdown quiescent current draw, adjustable UVLO through the EN pin and monotonic start up into pre-biased conditions. This device also features an I^{2}C interface for device configuration and output voltage adjustment. The TPS542A50 is a lead-free device. It is fully RoHS compliant without exemption.

Device Information

PART NUMBER	PACKAGE[(1)]	BODY SIZE (NOM)
TPS542A50	VQFN (33)	4.50 mm × 4.00 mm

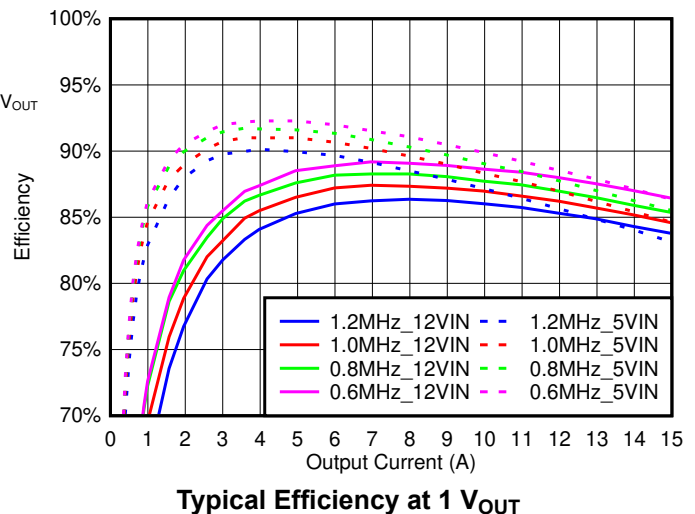(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

Typical Efficiency at 1 V_{OUT}

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 2020) to Revision A (October 2020)	**Page**
• Updated Figure 3-1 1	

5 Pin Configuration and Functions
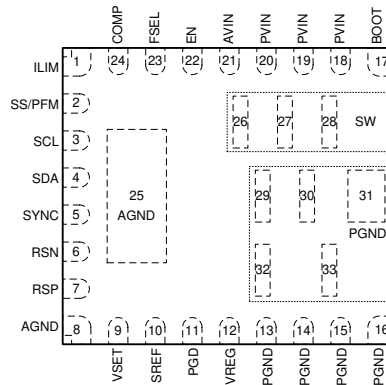
Figure 5-1. 33-Pin VQFN RJM Package (Top View)

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	8, 25	G	Ground of the internal analog and digital circuitry
AVIN	21	P	Power input to the controller. Tie this pin to PVIN. It is best to use an RC filter from PVIN such as 10 Ω and 100 nF to 1 µF.
BOOT	17	P	Gate drive voltage for high-side FET. Connect a bootstrap capacitor between this pin and SW.
COMP	24	I	A resistor to ground sets the I^{2}C address and compensation network. This pin can be grounded to select the default compensation and reduce BOM count.
EN	22	I	Enable pin. Float to enable, enable/disable with an external signal, or adjust the input undervoltage lockout with a resistor divider.
FSEL	23	I	A resistor to ground sets the switching frequency of the converter. This pin can be grounded to select the default switching frequency to reduce BOM count.
ILIM	1	I	A resistor to ground sets the overcurrent protection limit. This pin can be grounded to select default settings and reduce BOM count.
PGD	11	O	Open-drain power good status
PGND	13-16, 29-33	G	Power ground. These pins are internally connected to the return of the internal low-side FET.
PVIN	18-20	P	Power inputs to the power stage. Low impedance bypassing of these pins to PGND is critical. At least 10 nF to 100 nF capacitor from PVIN to PGND is required.
RSN	6	I	Remote sense ground return
RSP	7	I	Remote sense connection to V$_{OUT}$
SCL	3	I	Clock input for I^{2}C programming
SDA	4	I/O	Data input for I^{2}C programming
SREF	10	O	1.2-V nominal system reference
SS/PFM	2	I	A resistor to ground sets the soft-start slew rate and PFM mode. To reduce BOM count this pin can be grounded to use the default soft-start rate and enable PFM mode.
SYNC	5	I	In shutdown mode, an active high puts the IC into programming mode. In operation, this pin is a clock input for synchronizing the oscillator.
SW	26-28	O	Switch node output of the converter. Connect this pin to the output inductor.
VREG	12	I/O	Bypass pin for the internal power stage LDO. It is recommended to use 4.7-µF ceramic capacitor to ground.
VSET	9	I	Output voltage reference for the control loop. This must be the mid-point of a resistive divider from SREF to AGND. Set this voltage to be 1/5 of the desired V$_{OUT}$.

Product Folder Links: *TPS542A50*

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Input	PVIN, AVIN	−0.3	20	V
	PVIN - SW	−0.3	24	
	BOOT	−0.3	27.5	
	BOOT-SW	−0.3	5.5	
	EN, SYNC, SDA, SCL	−0.3	6	
	FS, COMP, ILIM, SS/PFM, SREF, VSET	−0.3	1.98	
	RSP	−0.3	6	
	PGD	−0.3	6	
Output	SW	−0.3	22	V
	SW transient (<10 ns)	−2	22	
	VREG	−0.3	6	
	Operating junction temperature, T_J	−40	150	°C
	Storage temperature, T_{stg}	−55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*s. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins[1]	±2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

T_J = -40°C to 150°C (unless otherwise noted)

		MIN	NOM	MAX	UNIT
PVIN, AVIN	Input voltage	4	12	18	V
VOUT	Output voltage	0.5		5.5	V
IOUT	Output current	0		15	A
EN,SDA, SCL		0		5.5	V
SYNC		0		3.3	V
FS, COMP, ILIM, SS/ PFM,SREF, VSET		0		1.8	V
T_J	Junction temperature	−40		150	°C

6.4 Thermal Information

THERMAL METRIC[1]		TPS542A50 RJM (VQFN) 33 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	54.9	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance EVM PCB Layout	22.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	23.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	17.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1)   For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

T_J = -40℃ to 150℃ (unless otherwise noted)

PARAMETER[1]		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY (PVIN, AVIN PINS)						
V_{IN}	PVIN and AVIN supply range		4	12	18	V
I_Q	Shutdown current	EN < 0.4 V		17		µA
	PFM Mode current	V_{IN} = 12 V, V_{OUT} = 1 V, EN > 1.2 V, no switching, V_{VRSF} > 5*V_{VSET}		1800		
ENABLE and UVLO (EN PIN)						
V_{EN}	Enable threshold: ON/OFF	Rising and falling		1.2		V
I_{EN}	Enable input current	Enable threshold – 50 mV		−0.6		µA
		Enable threshold + 50 mV		−5		
UVLO (AVIN, PVIN PINS)						
AVIN, PVIN	UVLO rising threshold		3.75	3.85	4	V
	UVLO falling threshold		3.50	3.6	3.7	
	Hysteresis			0.25		
INTERNAL REGULATOR, POWER STAGE (VREG PIN)						
V_{VREG}	LDO output voltage	LDO output current = 0A	4.3	4.7	4.96	V
V_{VREG}	LDO output voltage	LDO output current = 30mA		4.7		V
	Output current limit	V_{VREG} = 4.7V	120	170	220	mA
	Nominal output current	f_{sw} = 2.2 MHz, output current = 15 A, V_{VREG} = 4.7V		30		mA
$V_{REG(UVLO)}$	UVLO rising yhreshold			2.8		V
	UVLO falling threshold			2.6		
	UVLO hysteresis			0.2		
CONTROL REFERENCE VOLTAGE (SREF PIN)						
V_{SREF}	SREF output voltage	Tolerance included in RSP/RSN accuracy		1.2		V
ISREF	SREF current sourcing capability	Resistance > 6 KΩ			200	µA

T_J = -40℃ to 150℃ (unless otherwise noted)

PARAMETER[1]		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT VOLTAGE REGULATION ACCURACY						
	Output Voltage Accuracy; Vout = 1V	Total internal accuracy, measured at the RSP and RSN pins = 5*VSET, VSET = 0.2V, –40 to 150°C	-15		15	mV
	Output Voltage Accuracy; Vout =1V	Total internal accuracy, measured at the RSP and RSN pins = 5*VSET, VSET = 0.2V, –40 to 125°C	-13		13	mV
	Output Voltage Accuracy; Vout = 1V	Total internal accuracy, measured at the RSP and RSN pins = 5*VSET, VSET = 0.2V, 0 to 105°C	-11.0		9.0	mV
	Output Voltage Accuracy; Vout = 0.8V	Total internal accuracy, measured at the RSP and RSN pins = 5*VSET, VSET = 0.16V, –40 to 150°C	-15		15	mV
	Output Voltage Accuracy; Vout = 1.2V	Total internal accuracy, measured at the RSP and RSN pins = 5*VSET, VSET = 0.24V, –40 to 150°C	-15		15	mV
	Output Voltage Accuracy; Vout = 5.5V [1]	Total internal accuracy, measured at the RSP and RSN pins = 5*VSET, VSET = 1.1V, –40 to 150°C	-30		30	mV
REMOTE SENSE AMPLIFIER						
	Unity gain bandwidth [1]			7		MHz
	Open loop gain [1]			83		dB
	Slew rate [1]			2.5		V/us
	Input common mode range [1]		-0.05		1.1	V
Vos	Input offset voltage (RSA and EA combined offset trim) [1]			0.25		mV
SWITCHING FREQUENCY						
FSW_1MHz	Switching frequency 1MHz	R_{FSEL} = 33.2 kΩ or Short, Digital Code = 011	900	1000	1100	kHz
FSW_400KHz	Switching frequency 400KHz	R_{FSEL} = 10 kΩ, Digital Code = 000	-10		+15	%
FSW_600KHz	Switching frequency 600KHz	R_{FSEL} = 16.2 kΩ, Digital Code = 001	-10		+15	%
FSW_800KHz	Switching frequency 800KHz	R_{FSEL} = 23.7 kΩ, Digital Code = 010	-10		+15	%
FSW_1.2MHz	Switching frequency 1.2MHz	R_{FSEL} = 44.2 kΩ, Digital Code = 100	-9		+11	%
FSW_2MHz	Switching frequency 2MHz	R_{FSEL} = 61.9 kΩ, Digital Code = 101	-10		+15	%
FSW_2.2MHz	Switching frequency 2.2MHz	R_{FSEL} = 82.5 kΩ, Digital Code = 110	-10		+15	%
	Minimum on-time			12		ns
	Minimum Off-Time			85		ns
SYNC						
$V_{IH(SYNC)}$	High-level input voltage	EN = High	1.35			V
$V_{IL(SYNC)}$	Low-level input voltage				0.8	V
	Sync input minimum pulse width				50	ns
Δf_{SYNC}	SYNC pin frequency range from f_{SW}		–10%		15%	
$V_{IH(SYNC)-PROG}$	High-level input voltage to enter programming mode when EN = 0V	EN = Low	1.35			V
I2C COMMUNICATION (SDA, SCL)						
$V_{IH(I2C)}$	High-level input voltage		1.35			V
$V_{IL(I2C)}$	Low-level input voltage				0.8	V

Product Folder Links: *TPS542A50*

T_J = -40℃ to 150℃ (unless otherwise noted)

PARAMETER[1]		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{IH(I2C)}$	High-level input leakage current		–5		5	µA
$I_{IL(I2C)}$	Low-level input leakage current		–5		5	µA
$V_{OL(I2C)}$	Low-level output voltage	I_{PULLUP} = 20mA			0.4	V
I_{PULLUP}	Current through pull-up resistor				20	mA
$f_{CLK(I2C)}$	I2C operating frequency		10		1000	kHz
C_{Pin}	Typical pin capacitance for each line (SDA, SCL)			10		pF
POWER STAGE						
$R_{ds(on)1}$	Main high-side MOSFET on-resistance	V_{VREG} = 4.7 V, T_J = 25°C		9.1		mΩ
$R_{ds(on)2}$	Main Low-side MOSFET on-resistance	V_{VREG} = 4.7 V, T_J = 25°C		2.6		mΩ
Tdt(L-H)	Dead-time between low-side off and high-side on transition	VREG = 4.7V, T_J = 25°C		10		ns
Tdt(H-L)	Dead-time between high-side off and low-side on transition	VREG = 4.7V, T_J = 25°C		10		ns
CURRENT SENSE AND PROTECTION						
IS1	OC limit HS FET			20		A
IS2	OC limit LS FET 6	R_{ILIM} = 61.9KΩ; Digital Code = 101	17.60	20	22	A
	OC limit LS FET 5	R_{ILIM} = 44.2KΩ; Digital Code = 100	14.78	16.5	18.48	
	OC limit LS FET 4	R_{ILIM} = 33.2KΩ; Digital Code = 011	11.56	13	15.62	
	OC limit LS FET 3	R_{ILIM} = 23.7KΩ; Digital Code = 010	9.26	10.5	13.56	
	OC limit LS FET 2	R_{ILIM} = 16.2KΩ; Digital Code = 001	6.96	8	11.60	
	OC limit LS FET 1	R_{ILIM} = 10.0KΩ; Digital Code = 000	4.66	5.5	9.60	
IS2	Negative OC limit LS FET			-8.5		A
IS2	Zero-cross detection comparator trip point			135		mA
SOFT-START COUNTER						
t_{SS}	SS setting 1: 2.0MHz CLK	V_{VSET} = 0.1 V to 0.28 V		0.45		ms
	SS setting 2: 1.0MHz CLK	V_{VSET} = 0.1 V to 0.28 V		0.9		
	SS setting 3: 0.5MHz CLK	V_{VSET} = 0.1 V to 0.28 V		1.8		
	SS setting 4: 0.25MHz CLK	V_{VSET} = 0.1 V to 0.28 V		3.6		
OUTPUT ADJUSTMENT						
	Output voltage adjust upper limit			10		%
	Output voltage adjust lower limit			–20		%
	Step size				0.5	%
INTERNAL BOOTSTRAP SWITCH						
	Forward voltage	$V_{VREG(BOOT)}$, I_F = 10 mA, T_A = 25°C		0.16	0.3	V
OUTPUT VOLTAGE OVERSHOOT REDUCTION						
POWER-ON DELAY						
	Power-on delay time	From EN to SS; V_{IN} > 4 V		500		us
POWER GOOD and OV/UV WARNING						
V_{RSP}	OV warning level	RSP rising (fault)	105	110	115	% 5*V VSET
	OV warning level	RSP falling (reset)	100	105	109	
	UV warning level	RSP falling (fault)	87	90	93.5	
	UV warning level	RSP rising (reset)	91	95	99	
	PGD delay time	Delay from SS finish to PGD high		500		µs

T_J = -40℃ to 150℃ (unless otherwise noted)

PARAMETER[1]		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RDS_ON_P GFET		PGOOD FET On Resistance, I_{PGOOD} =5mA	4.1	5.8	9.1	Ω
OUTPUT OVERVOLTAGE PROTECTION (OVP)						
V_{RSP}	OVP trip level	RSP rising (fault), V_{VSET} ≤ 1.04 V	110	115	120	% 5*V VSET
	OVP reset level	RSP falling	76	80	84	
	OVP delay			100		ns
OUPUT UNDERVOLTAGE PROTECTION (UVP)						
V_{RSP}	UVP detect voltage		76	80	84	% 5*V SET
	UV delay			100		ns
THERMAL SHUTDOWN						
T_{SDN}	Shutdown temperature[1]		155	165		℃
	Hysteresis[1]			15		℃

(1)   Specified by design. Not production tested.

6.6 Typical Characteristics

Measured at 25°C unless otherwise specified

V_{OUT} = 1 V f_{SW} = 1 MHz, FCCM
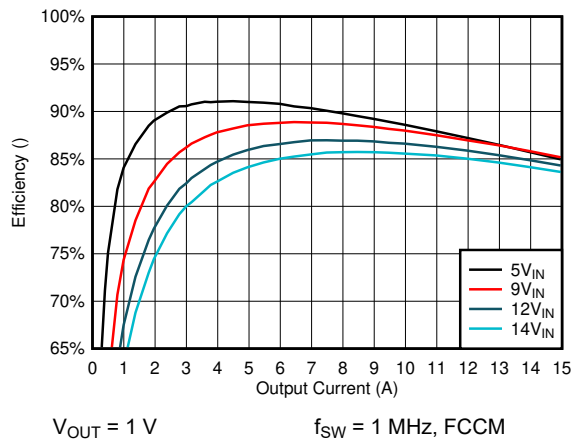
Figure 6-1. Efficiency vs Output Current

V_{OUT} = 1 V f_{SW} = 1 MHz, FCCM
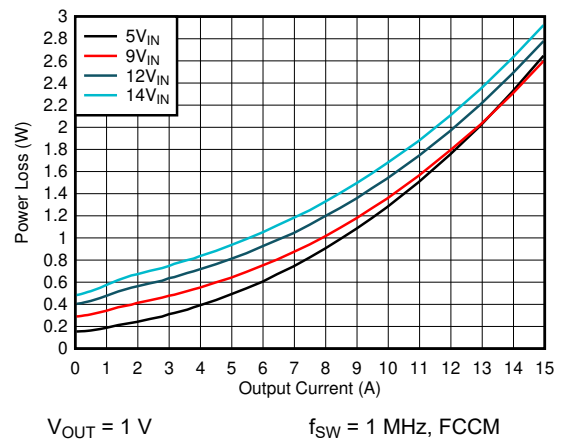
Figure 6-2. Power Loss vs Output Current

V_{OUT} = 1 V f_{SW} = 1 MHz, DCM versus FCCM
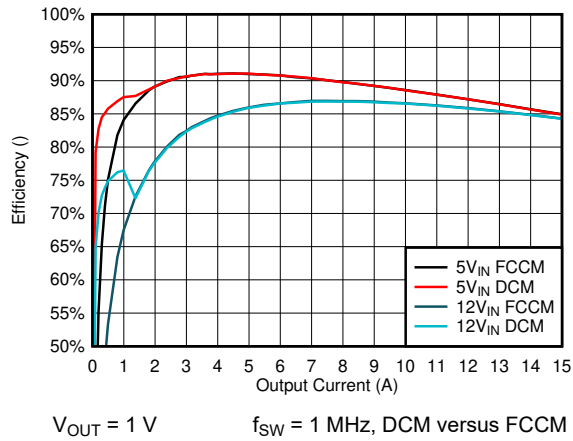
Figure 6-3. Efficiency vs Output Current

V_{OUT} = 1 V f_{SW} = 1 MHz, DCM versus FCCM
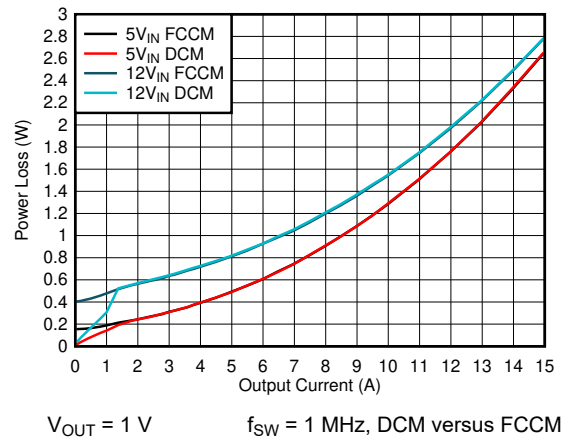
Figure 6-4. Power Loss vs Output Current

V_{OUT} = 5 V f_{SW} = 400 kHz, FCCM
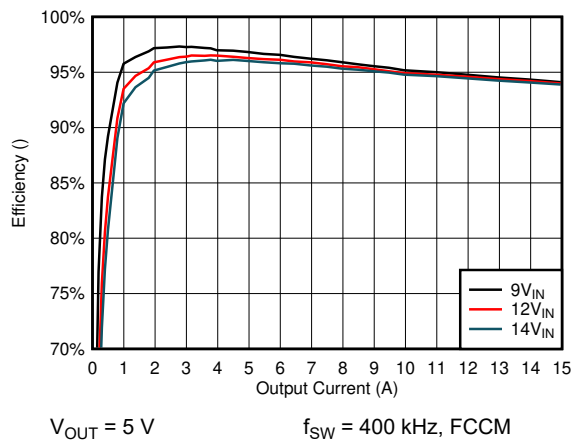
Figure 6-5. Efficiency vs Output Current

V_{OUT} = 5 V f_{SW} = 400 kHz, FCCM
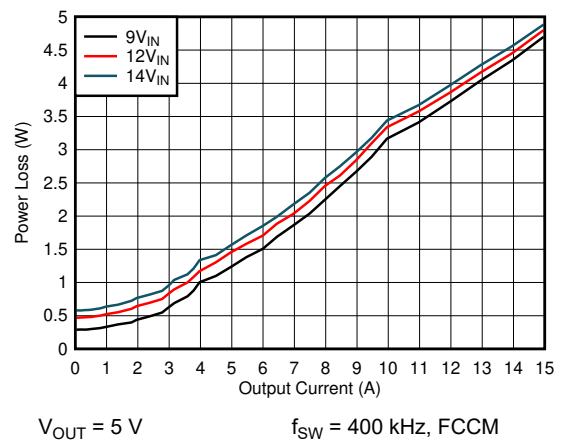
Figure 6-6. Power Loss vs Output Current

Product Folder Links: *TPS542A50*

V_{OUT} = 1 V f_{SW} = 1 MHz, FCCM
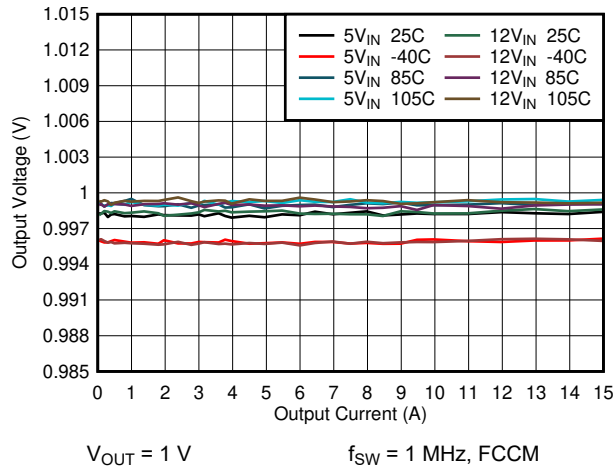
Figure 6-7. Load Regulation
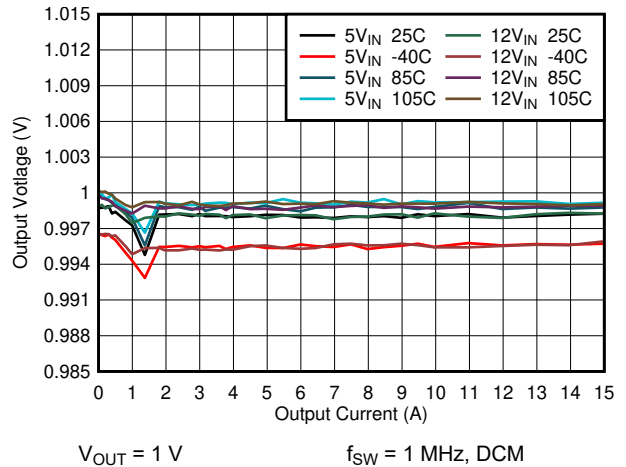
V_{OUT} = 1 V f_{SW} = 1 MHz, DCM

Figure 6-8. Line Regulation

V_{IN} = 12 V V_{OUT} = 5 V f_{SW} = 400 KHz, FCCM
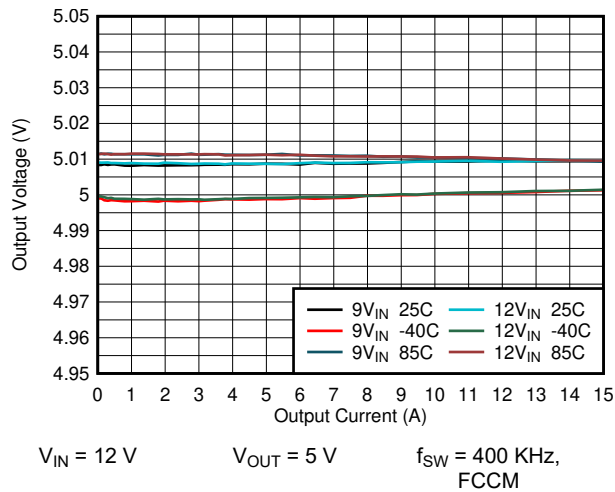
Figure 6-9. Line Regulation

V_{IN} = 12 V V_{OUT} = 1 V f_{SW} = 1 MHz
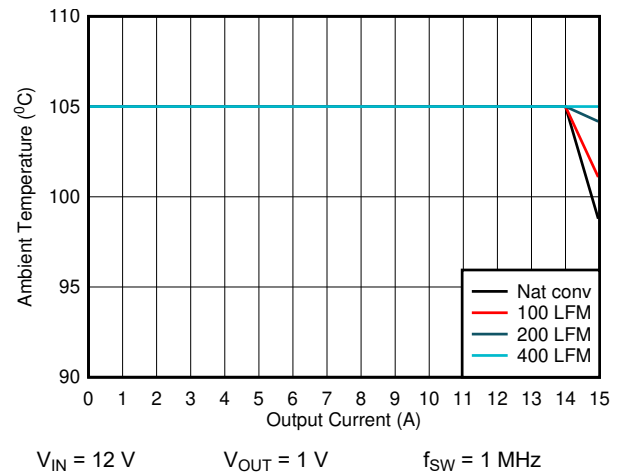
Figure 6-10. Ambient Temperature vs Output Current

V_{IN} = 12 V V_{OUT} = 5 V f_{SW} = 600 kHz
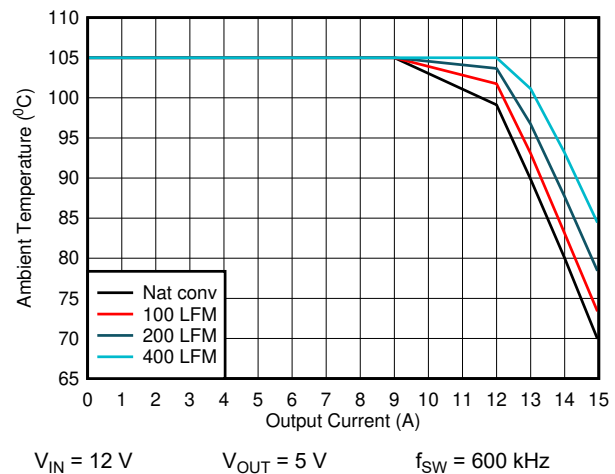
Figure 6-11. Ambient Temperature vs Output Current

V_{IN} = 5.5 V V_{OUT} = 1 V f_{SW} = 2.2 MHz
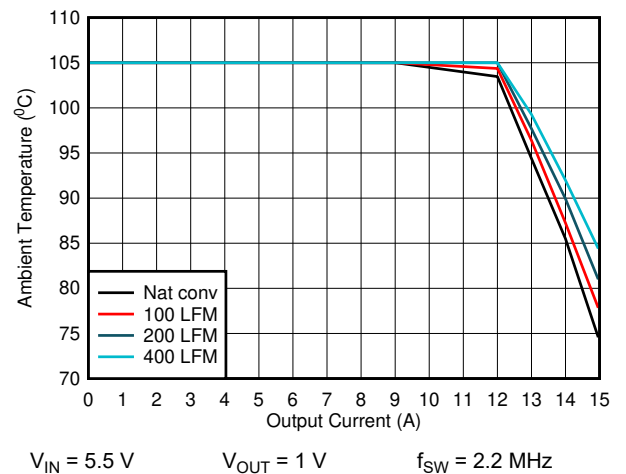
Figure 6-12. Ambient Temperature vs Output Current

Product Folder Links: *TPS542A50*
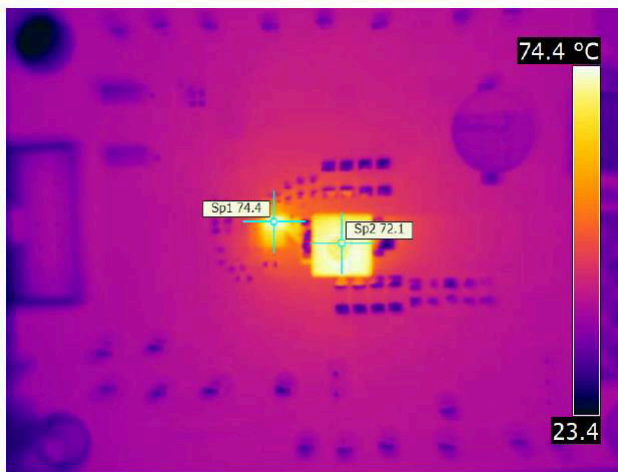
V_{IN} = 12 V V_{OUT} = 1 V f_{SW} = 1 MHz
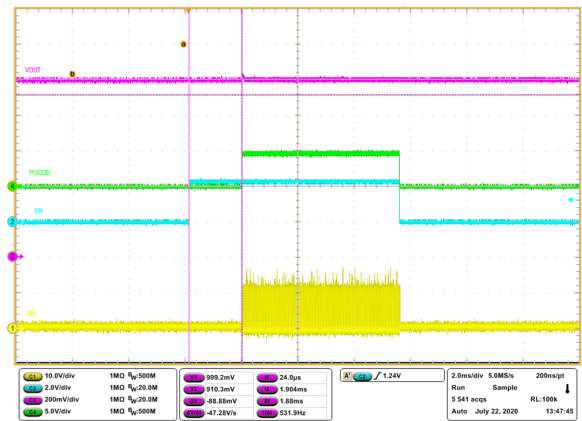
Figure 6-13. Thermal Image at 15-A Output Current

V_{IN} = 5.5 V V_{OUT} = 1 V f_{SW} = 2.2 MHz

Figure 6-14. Thermal Image at 14-A Output Current

V_{IN} = 12 V V_{OUT} = 5 V f_{SW} = 0.6 MHz

Figure 6-15. Thermal Image at 12-A Output Current

V_{IN} = 12 V V_{OUT} = 1 V f_{SW} = 1.0 MHz BOM

Figure 6-16. 100% Pre-biased Start-up by EN at 0-A Output Current
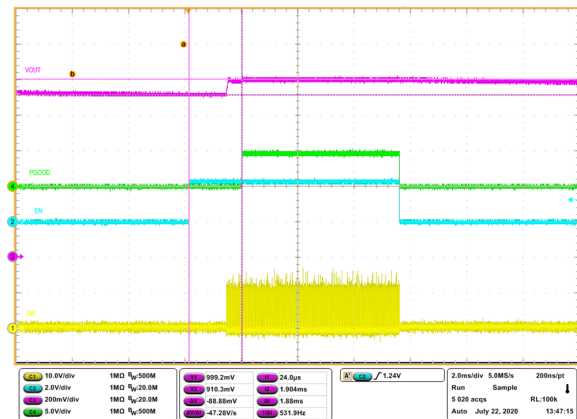
V_{IN} = 12 V V_{OUT} = 1 V f_{SW} = 1.0 MHz BOM

Figure 6-17. 90% Pre-biased Start-up by EN at 0-A Output Current

V_{IN} = 12 V V_{OUT} = 1 V f_{SW} = 1.0 MHz BOM

Figure 6-18. 50% Pre-biased Start-up by EN at 0-A Output Current

Product Folder Links: *TPS542A50*

V$_{IN}$ = 12 V   V$_{OUT}$ = 1 V   f$_{SW}$ = 1.0 MHz BOM

Figure 6-19. Start-up and Shutdown by EN at 0-A Output Current
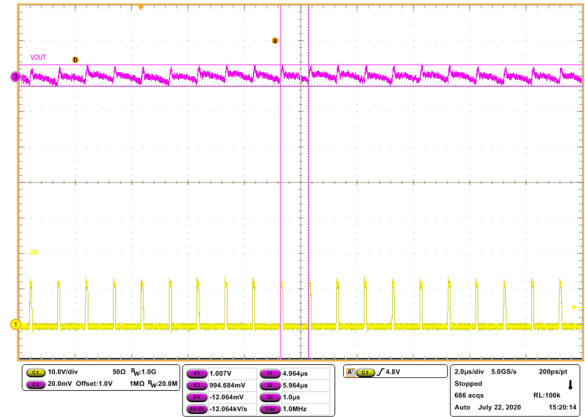
V$_{IN}$ = 12 V   V$_{OUT}$ = 1 V   f$_{SW}$ = 1.0 MHz BOM

Figure 6-20. Steady State at 0-A Output Current
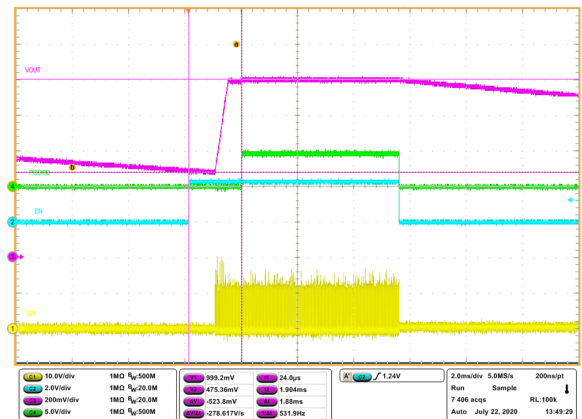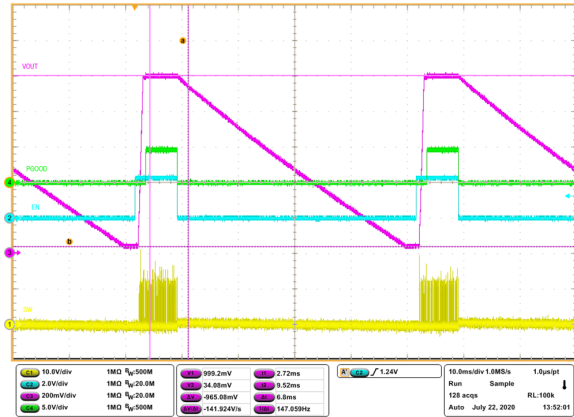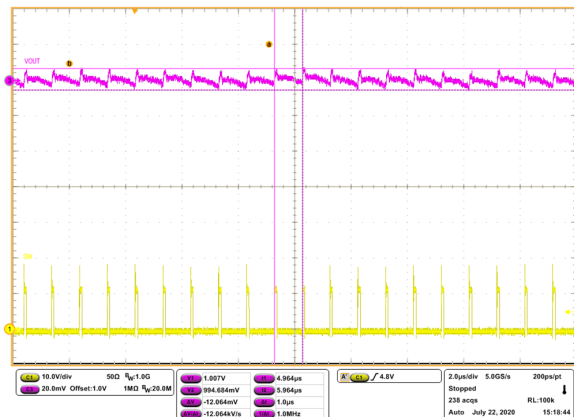

V$_{IN}$ = 12 V   V$_{OUT}$ = 1 V   f$_{SW}$ = 1.0 MHz BOM

Figure 6-21. Steady State at 10-A Output Current

V$_{IN}$ = 12 V   V$_{OUT}$ = 1 V   f$_{SW}$ = 1.0 MHz BOM

Figure 6-22. Switch Node Ringing and Dead-Time at 10-A Output Current
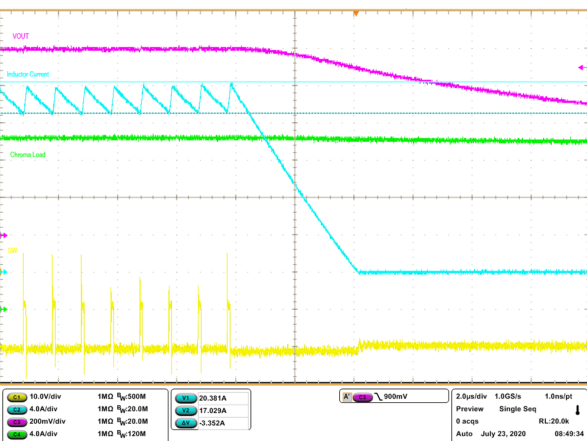
V$_{IN}$ = 12 V   V$_{OUT}$ = 1 V   f$_{SW}$ = 1.0 MHz BOM

Figure 6-23. 20-A Overcurrent Protection by Chroma Electronic Load
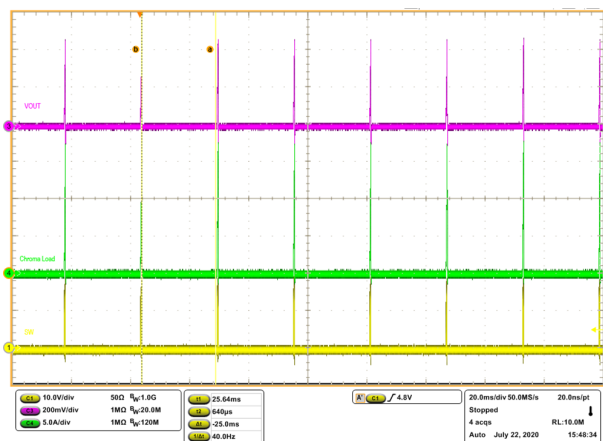
V$_{IN}$ = 12 V   V$_{OUT}$ = 1 V   f$_{SW}$ = 1.0 MHz BOM

Figure 6-24. Short Overcurrent Protection Hiccup by Chroma Electronic Load

Product Folder Links: *TPS542A50*
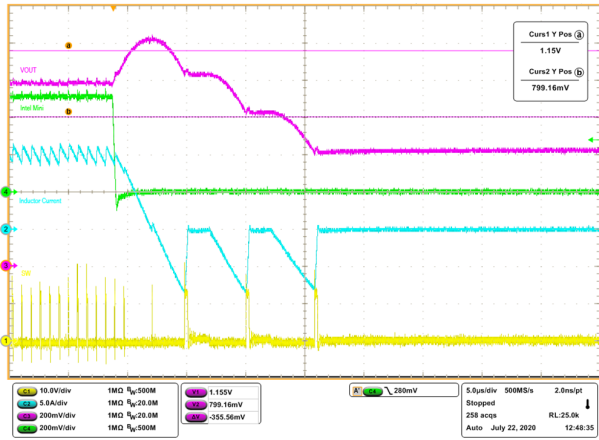
V_{IN} = 12 V V_{OUT} = 1 V f_{SW} = 1.2 MHz BOM

Figure 6-25. Overvoltage Protection, Negative OCP, then Undervoltage Protection by Load Stepdown
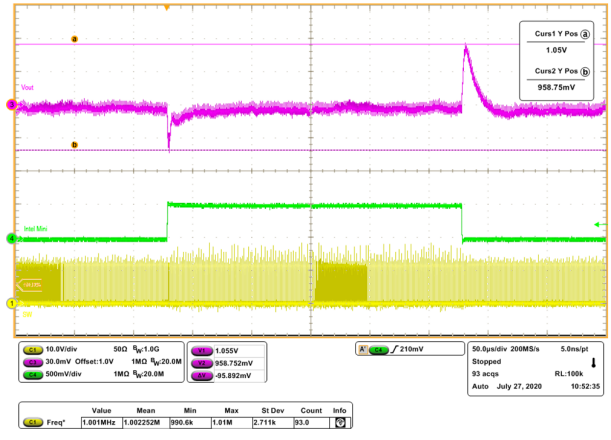
V_{IN} = 12 V V_{OUT} = 1 V f_{SW} = 1.0 MHz BOM

Figure 6-26. Load Transient 2 A to 12 A to 2 A at 20 A/μs
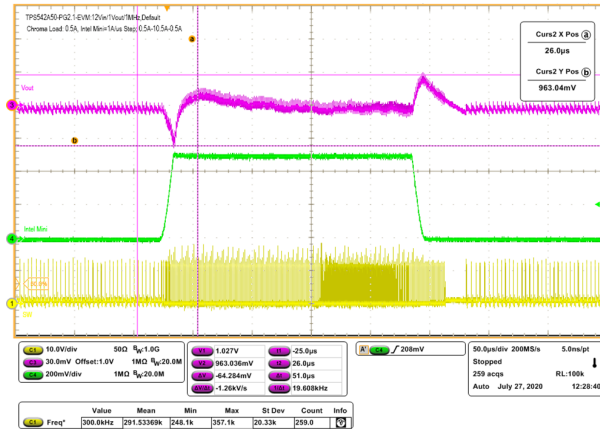
V_{IN} = 12 V V_{OUT} = 1 V f_{SW} = 1.0 MHz BOM

Figure 6-27. Load Transient in DCM to FCM 0.5 A to 10.5 A to 0.5 A at 1 A/μs

7 Detailed Description

7.1 Overview

The TPS542A50 is a high-efficiency, single-channel, synchronous buck converter with integrated n-channel MOSFETs. The device suits low-output voltage point-of-load applications with 15-A or lower current. The TPS542A50 has a maximum operating junction temperature of 150°C, making it suitable for high-ambient temperature applications such as wireless infrastructure. The input voltage range is 4 V to 18 V, and the output voltage range is 0.5 V to 5.5 V. The device features a fixed-frequency, voltage-control mode with a switching frequency range of 400 kHz to 2.2 MHz, allowing for efficiency and size optimization when selecting output filter components. The controller features selectable internal compensation that makes the device easy to use with low external component count. The internal compensation networks support a wide range of output inductance and capacitance, supporting all types of capacitors. The controller uses a digital PWM modulator that allows for very narrow on-times with low jitter, making it ideal for high-frequency and high-step down ratio applications. The switching frequency of the device can be synchronized to an external clock applied to the SYNC pin. The TPS542A50 also features an I^{2}C interface for device configuration and output voltage adjustment.

7.2 Functional Block Diagram

Product Folder Links: *TPS542A50*
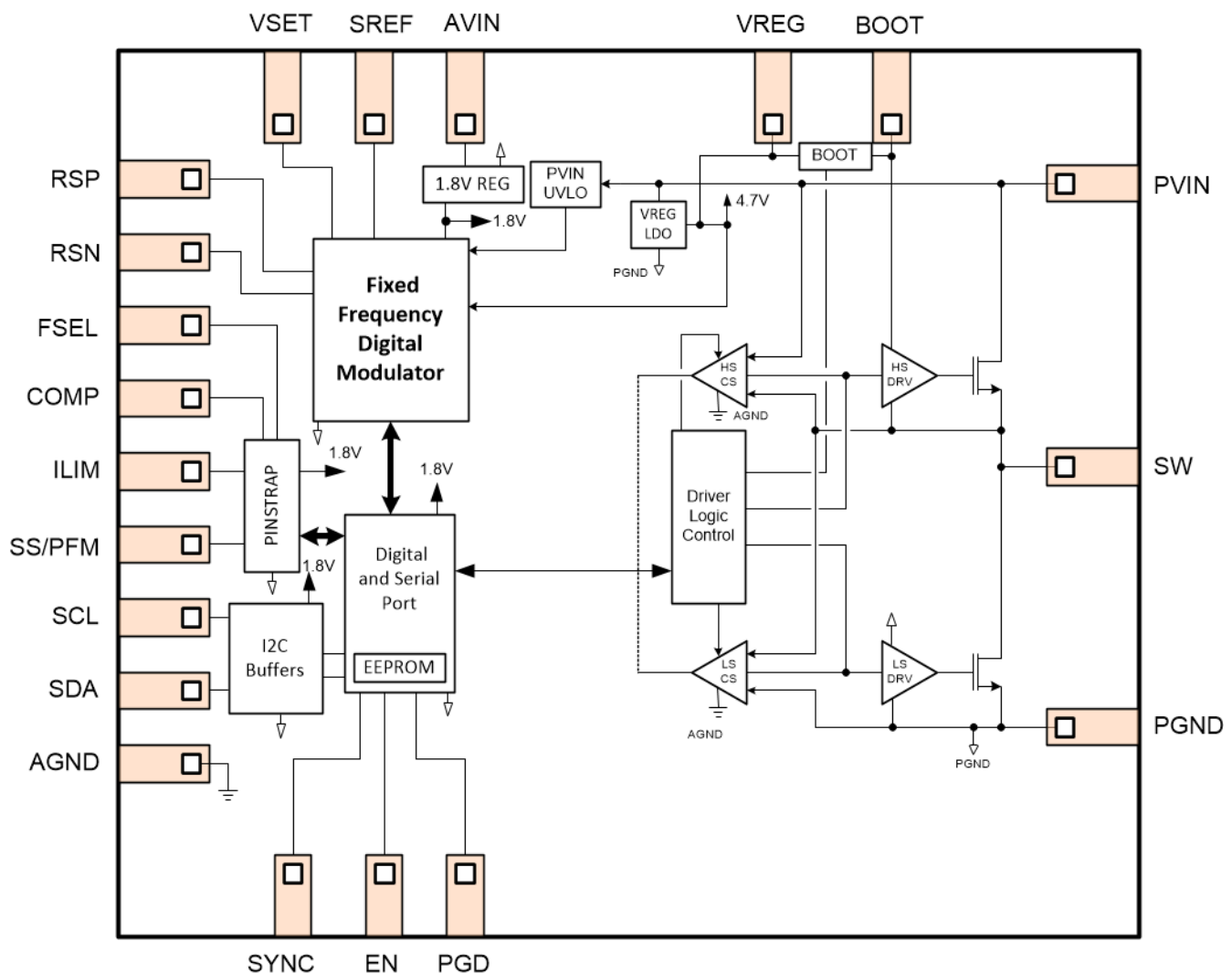
7.3 Feature Description

7.3.1 Enable and Adjustable Undervoltage Lockout

The EN pin provides electrical on/off control of the device. Once the EN pin voltage exceeds the threshold voltage (typically 1.2 V), the device starts operation. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low power shutdown.

The EN pin has an internal pullup current source, allowing the user to float the EN pin for enabling the device. The EN pin can also be externally driven high or low.

For adjustable input undervoltage lockout (UVLO), connect the EN pin to the middle point of an external resistor divider. Once the EN pin voltage exceeds the threshold, an additional 5 µA of hystersis current is added to facilitate UVLO hysteresis. Equation 1 shows the calculation of resistor divider network.
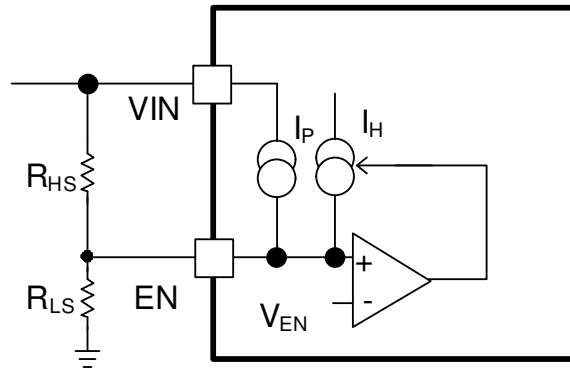
Figure 7-1. EN UVLO

$$R_{HS} = \frac{V_{START} - V_{STOP}}{I_H}$$

$$R_{LS} = \frac{R_{HS} \cdot V_{EN}}{V_{STOP} - V_{EN} + R_{HS}(I_P + I_H)}$$

$$V_{EN} = 1.2V; \ I_P = 0.6\mu A; \ I_H = 5\mu A$$

(1)

7.3.2 Input and VREG Undervoltage Lockout Protection

The TPS542A50 provides fixed VIN and VREG UVLO thresholds and hysteresis. The typical VIN turnon threshold is 3.85 V and hystersis is 0.25 V. The typical VREG turnon threshold is 2.8 and hysteresis is 0.2 V. There is no power-up sequence. Once all of the UVLO requirements have been met and the EN pin voltage exceeds the enable threshold, the converter begins operation.

7.3.3 Voltage Reference and Setting the Output Voltage

The device has a 1.2-V reference that comes out on the SREF pin. To set the reference voltage of the converter, connect the VSET pin to the mid-point of a resistor divider between SREF and AGND. TI recommends that the total impedance of this divider network be > 6 kΩ. Do not connect anything other than a resistor divider network to SREF.

There is an internal 5:1 resistor divider between the RSP and RSN feedback pins, so the VSET voltage must be set to 1/5 of the desired output voltage. VSET can be programmed to any value between 0.1 and 1.1 V.

7.3.4 Remote Sense Function

RSP and RSN pins are used for remote sensing purposes. Always connect RSP to the positive sensing point of the load, and always connect the RSN pin to the load return. There is an internal 5:1 divider in the device, so do not connect an external feedback resistor divider. The converter loop gain can tolerate between 10 Ω to 50 Ω in series with RSP and output voltage.

7.3.5 Switching Frequency

The internal oscillator of the device can be set to one of seven switching frequencies by a resistor to ground on the FSEL pin or through I²C programming. The FSEL pin can be shorted to ground to reduce BOM component count. When shorted to ground, the default converter switching frequency is used. If the user programs the switching frequency using the I²C interface, TI recommends shorting the FSEL pin to ground to reduce component count. The following frequencies can be programmed on the FSEL pin.

Table 7-1. Frequency Resistor Selection

R_{FSEL} (kΩ)	f_{SW} (kHz)
Short	1000
10	400
16.2	600
23.7	800
33.2	1000
44.2	1200
61.9	2000
82.5	2200

The oscillator can also be synchronized to an external clock on the SYNC pin. The external clock frequency must be within -10% and +15% of the programmed frequency of the converter. The SYNC pin has an internal pulldown so it can be left floating externally.

When the converter operates at 2 MHz or 2.2 MHz, it is recommended to set the OCP at 13 A or lower and without a snubber circuit. For operation with OCP at 16.5 A, a snubber circuit is required. The snubber circuit components can start with a 470-pF cap and 2-Ω resistor. The component values will need to be tuned to achieve optimal results.

7.3.6 Voltage Control Mode Internal Compensation

The TPS542A50 has 15 unique internal compensation settings to cover a wide range of output inductors and capacitors. For each switching frequency option, there are four compensation options that can be chosen using a single resistor to ground on the COMP pin or through I²C programming.

In addition to selecting the compensation option, the COMP pin also selects the device I²C address. The following compensation settings and I²C address combinations can be programmed on the COMP pin.

Table 7-2. Compensation and I²C Address Resistor Selection

R_{COMP} (kΩ)	I²C ADDRESS	COMPENSATION SETTING
Short	0x60	COMP 2
10		COMP 1
16.2	0x60	COMP 2
23.7		COMP 3
33.2		COMP 4
44.2		COMP 1
61.9	0x61	COMP 2
82.5		COMP 3
100		COMP 4

Each compensation network consists of two zeros and one high frequency pole. Table 7-3 maps the compensation settings to the first zero frequency at different output voltage range, second zero frequency, and high frequency pole.

Table 7-3. Compensation Settings

FREQUENCY (kHz)	COMPENSATION SETTING	ZERO 1 (kHz) FOR VOUT = 0.5 V-1.1 V	ZERO 1 (kHz) for VOUT = 1.2 V-1.5 V	ZERO 1 (kHz) FOR VOUT = 1.6 V-2.8 V	ZERO 1 (kHz) FOR VOUT = 2.9 V-4.0 V	ZERO 1 (kHz) for VOUT = 4.1 V-5.5 V	ZERO 2 (kHz)	POLE (kHz)
400	COMP 1	2.2	2.1	1.8	1.6	1.2	5.5	60
	COMP 2	2.2	2.1	1.8	1.6	1.2	7.3	80
	COMP 3	3.6	3.4	3.0	2.7	2.0	14.5	159
	COMP 4	7.2	7.0	6.1	5.4	4.1	28.4	312
600	COMP 1	2.2	2.1	1.8	1.6	1.2	5.5	60
	COMP 2	2.7	2.6	2.3	2.0	1.5	11.0	121
	COMP 3	4.5	4.3	3.8	3.4	2.5	18.1	199
	COMP 4	10.5	10.1	8.8	7.9	5.9	45.2	497
800	COMP 1	2.2	2.1	1.8	1.6	1.2	7.3	80
	COMP 2	3.6	3.4	3.0	2.7	2.0	14.5	159
	COMP 3	7.2	7.0	6.0	5.4	4.1	28.4	312
	COMP 4	13.5	13	11.4	10.1	7.6	55.6	612
1000	COMP 1	2.2	2.1	1.9	1.7	1.2	9.0	99
	COMP 2	4.5	4.3	3.8	3.4	2.5	18.1	199
	COMP 3	9.0	8.7	7.6	6.7	5.1	37.1	408
	COMP 4	18.8	18.2	15.9	14.1	10.6	72.3	796
1200	COMP 1	2.7	2.6	2.3	2.0	1.5	11.0	121
	COMP 2	4.5	4.3	3.8	3.4	2.5	18.1	199
	COMP 3	10.5	10.1	8.8	7.9	5.9	45.2	497
	COMP 4	23.5	22.7	19.9	17.7	13.3	90.4	995
2000	COMP 1	4.5	4.3	3.8	3.4	2.5	18.1	199
	COMP 2	9	8.7	7.6	6.7	5.1	37.1	408
	COMP 3	18.8	18.2	15.9	14.1	10.6	72.3	796
	COMP 4	37.7	36.4	31.8	28.3	21.2	144.7	1592
2200	COMP 1	4.5	4.3	3.8	3.4	2.5	18.1	199
	COMP 2	9	8.7	7.6	6.7	5.1	37.1	408
	COMP 3	18.8	18.2	15.9	14.1	10.6	72.3	796
	COMP 4	37.7	36.4	31.8	28.3	21.2	144.7	1592

Table 7-4 shows the second zero frequency placement about two times based on a ratio (f_O/f_{SW}) of the LC frequency (f_O) to the switching frequency and lists the values in Table 7-3. The second zero frequency does not change with the output voltage. The high frequency pole is about 10 times of the second zero frequency to attenuate the switching frequency noise and to have a safe gain margin.

The output filter LC frequency must be designed between the first and second zero frequencies. The ratio of the LC frequency to the switching frequency in Table 7-4 is a guide to select the LC frequency f_O. For example, the LC frequency for 1-MHz switching frequency is 10 KHz at 1% ratio. Given 1-V output voltage, COMP2 has the first zero at 4.5 kHz to compensate the LC filter double poles. For the same LC filter and switching frequencies of 3.3-V output voltage, COMP3 has the first zero at 6.7 kHz to compensate the LC filter double poles. The compensation setting needs to consider for the output capacitor derating, especially ceramic capacitor, and inductor tolerance. It is recommended to verify the load transient and bode plot based upon the compensation selection.

Table 7-4. Second Zero Frequency

f_O/f_{SW}	COMPENSATION SETTING	SECOND ZERO FREQUENCY
0.5%	COMP 1	~2X of 0.5% f_O/f_{SW}
1%	COMP 2	~2X of 1% f_O/f_{SW}
2%	COMP 3	~2X of 2% f_O/f_{SW}

Table 7-4. Second Zero Frequency (continued)

f_O/f_{SW}	COMPENSATION SETTING	SECOND ZERO FREQUENCY
4%	COMP 4	~2X of 4% f_O/f_{SW}

7.3.7 Soft Start and Prebiased Output Start-up

The TPS542A50 uses a programmable soft-start rate to gradually ramp the output voltage reference to reduce inrush currents. The device prevents current from being discharged from the output during start-up when a pre-biased condition exists. No switching pulses occur until the internal soft-start reference exceeds the voltage on the error amplifier input voltage (RSP and RSN pins). The TPS542A50 supports the output voltage with pre-biased up to 100%.

The soft-start clock in Table 7-5 can be programmed on the SS/PFM pin along with enabling/disabling PFM and hiccup time. These same options can also be programmed through the I^2C interface. The SS/PFM pin can be shorted to ground to reduce BOM component count. When shorted to ground the default soft-start slew rate is used, and PFM is disabled. If the user programs these functions frequently using the I^2C interface, TI recommends shorting the SS/PFM pin to ground to reduce component count. The soft-start timing in Table 7-6 can be programmed based upon the output voltage and soft-start clock. There are four choices of soft-start times to select different soft-start clocks. Using 1-V output voltage as an example, the soft-start time equals to 1.8 ms at 0.5-MHz SS CLK and 0.45 ms at 2.0-MHz SS CLK.

Table 7-5. Soft-Start CLK and PFM Resistor Selection and Hiccup Time

$R_{SS/PFM}$ (kΩ)	PFM	SS CLK (MHz)	HICCUP DURATION (ms)
Short	Disable	1.0	25.2
10	Enable	2.0	12.6
16.2		1.0	25.2
23.7		0.50	50.4
33.2		0.25	100.8
44.2	Disable	2.0	12.6
61.9		1.0	25.2
82.5		0.50	50.4
100		0.25	100.8

Product Folder Links: *TPS542A50*

Table 7-6. Soft-Start Timing versus Output Voltage

VSET (V)	VOUT (V)	LSB SIZE (mV)	SS TIMING (ms) AT CLK: 2.0 MHz	SS TIMING (ms) AT CLK: 1.0 MHz	SS TIMING (ms) AT CLK: 0.5 MHz	SS TIMING (ms) AT CLK: 0.25 MHz
0.1	0.5	0.112	0.45	0.9	1.8	3.6
0.2	1	0.223	0.45	0.9	1.8	3.6
0.28	1.4	0.313	0.45	0.9	1.8	3.6
0.3	1.5	0.167	0.9	1.8	3.6	7.2
0.4	2.0	0.223	0.9	1.8	3.6	7.2
0.5	2.5	0.279	0.9	1.8	3.6	7.2
0.56	2.8	0.313	0.9	1.8	3.6	7.2
0.6	3.0	0.167	1.8	3.6	7.2	14.4
0.7	3.5	0.195	1.8	3.6	7.2	14.4
0.8	4	0.223	1.8	3.6	7.2	14.4
0.9	4.5	0.251	1.8	3.6	7.2	14.4
1	5.0	0.279	1.8	3.6	7.2	14.4

7.3.8 Power Good

The power good pin is an open-drain output and needs to pull up to a voltage supply if a designer uses this feature. During normal converter operation, the device leaves this pin floating. Power good warnings occur if the output voltage is not within the OV or UV warning levels. Power Good (PGD) is forced low when a fault occurs, when the converter is in soft start, and when the converter is in shutdown or programming mode. The PGD pin is released to floating after the PGD delay time when all of the above conditions are met.

TI recommends connecting a pullup resistor to a voltage source that is 5.5 V or less, such as to the device VREG pin.

7.3.9 Overvoltage and Undervoltage Protection

An output overvoltage (OV) fault is triggered if the output voltage, sensed by RSP/RSN, is greater than the OVP trip level. When this condition is detected, the converter terminates the switching cycle and turns on the low-side FET to discharge the output voltage. The low-side FET remains on until the low-side FET current reaches the negative overcurrent limit. When the negative overcurrent limit is reached, the low set FET turns off for 2000 ns. After the 2000 ns delay, the low-side FET turns back on until the negative overcurrent limit is reached. This process repeats until the output voltage is discharged below the undervoltage fault threshold (typically 80% set V_{OUT}). The converter then enters hiccup for seven cycles of soft-start CLK frequency due to the output voltage being below the UV threshold.

An output undervoltage fault is triggered if the output voltage, sensed by RSP/RSN, is less than UVP threshold. When this condition is detected, power conversion is disabled, and the converter enters hiccup for seven cycles of soft-start CLK frequency.

7.3.10 Overcurrent Protection

The device senses overcurrent (OC) in both the high-side and low-side power MOSFETs using cycle by cycle detection. OC is detected in the low-side FET by sensing the voltage across the FET while it is on. After the low-side FET turns on, there is a blanking time of approximately 70 ns to allow noise to settle before the OC comparator begins sensing. Once an OC fault condition is detected, the device stops switching and enters hiccup for seven cycles of soft-start CLK frequency. The overcurrent limit is set through a single resistor to ground on the ILIM pin or through I^2C programming. The ILIM pin can be shorted to ground to reduce BOM component count. When shorted to ground, the default current limit is used. If the user programs the current limit using the I^2C interface, TI recommends shorting the ILIM pin to ground to reduce component count. Current limits shown in Table 7-7 can be programmed on the ILIM pin.

Table 7-7. Current Limit Resistor Selection

R_{ILIM} (kΩ)	TYPICAL LIMIT (A)
Short	20
10	5.5
16.2	8
23.7	10.5
33.2	13
44.2	16.5
61.9	20

The device also senses negative overcurrent in the low-side FET by sensing the voltage across the FET while it is on. After the low-side FET turns on, there is a blanking time to allow noise to settle before the OC comparator begins sensing. Once a negative OC fault condition is detected, the device stops switching and enters hiccup for seven cycles of soft-start CLK frequency. The negative overcurrent threshold is fixed to a single value.

Overcurrent is detected in the high-side FET by sensing the voltage across the FET while it is on. After the high-side FET turns on, there is a blanking time to allow noise to settle before the OC comparator begins sensing. Once an OC fault condition is detected, the device stops switching and enters hiccup for seven cycles of soft-start CLK frequency. The high-side overcurrent threshold is fixed to a single value. For an application with on-time less than 70 ns, the high-side FET overcurrent is not guaranteed to enable. In this case, the low-side OC will dominate and protect the load while the output current ramps up gradually. With on-times less than 70 ns and a hard short at the load, the controller loop will extend the on-time to respond to the output voltage drooping, and as a result, both high-side and low-side OC protections will engage to protect the load.

7.3.11 High-Side FET Throttling

When the high-side FET turns on or off, the ringing voltage across the FET depends on the output current, loop inductance, and PCB parasitic inductance. To diminish the ringing voltage during turning on or off, the TPS542A50 reduces the gate driver strength when TPS542A50 detects PVIN higher than 14 V with 0.5-V hysteresis.

7.3.12 Overtemperature Protection

When the device senses a temperature above the thermal shutdown limit (typically 165°C), power conversion is disabled. The converter remains disabled until the temperature cools down to the thermal recovery limit (typically 150°C). At this point, the converter enters hiccup for seven cycles of soft-start CLK frequency.

7.4 Device Functional Modes

7.4.1 Pulse-Frequency Modulation Eco-mode™ Light Load Operation

When the SS/PFM pin is terminated with a 33.2-kΩ or lower resistance, the TPS542A50 operates in pulse-frequency modulation (PFM) for light load conditions to maintain high efficiency.

As the output current decreases from heavy-load conditions, the inductor current also decreases until the valley of the inductor current reaches zero amps, which is the boundary between continuous-conduction mode (CCM) and discontinuous-conduction mode (DCM). The synchronous MOSFET turns off when this zero inductor current is detected. As the load current decreases further, the converter runs in DCM. In DCM operation, the on-time is maintained to a level approximately the same as during CCM and the converter off-time is modulated to maintain the proper output voltage. For the application of 5-V input voltage, it is not recommend to operate in PFM due to the accuracy of the zero comparator which will be reduced because of the low input voltage.

7.4.2 Forced Continuous-Conduction Mode

When the SS/PFM pin is terminated with a 44.2-kΩ or higher resistance, the TPS542A50 operates in forced continuous conduction mode (FCCM) for all load currents. During FCCM, the switching frequency is set by an internal oscillator for which the frequency can either be selected by the FSEL pin, programmed through I^2C, or synchronized to an external clock on the SYNC pin.

7.4.3 Soft Start

The TPS542A50 operates in FCCM during soft start regardless of the setting selected by the SS/PFM pin. If PFM is enabled by the SS/PFM pin, the PFM operation begins after PGD is asserted. The delay between soft start finishing and PGD being asserted is typically 500 µs. During the start-up, the TPS542A50 has the low-side current limit at 16.5 A when the OCP configures 20 A. However, if the OCP configures below 16.5 A such as 13 A, then the current limit during soft start sets to be at 13 A.

7.5 Programming

7.5.1 I^2C Address Selection

The I^2C address is selected by a single resistor to ground on the COMP pin. Note that this function is combined with setting the compensation value. Refer to Table 7-8 for selecting a COMP pin resistor value for your application.

Table 7-8. COMP Resistor Selection for I^2C Address

R_{COMP} (kΩ)	I^2C ADDRESS
≤ 33.2	0x60
≥ 44.2	0x61

7.5.2 Powering Device Into Programming Mode

The TPS542A50 can be powered on into programming mode for pre-operation configuration by bringing the SYNC pin above the SYNC threshold. This wakes up the device from low-power shutdown mode and the I^2C interface is active for communication. Once the device configuration is complete, the EN pin can be brought above the EN threshold to begin power conversion. After this, the SYNC pin can either be driven low, hi-z, or used to synchronize the switching frequency to an external clock.

7.5.3 Device Configuration

The device settings can be configured when in programming mode before the device begins power conversion. When in programming mode, the switching frequency, current limit, internal compensation, soft-start rate, and FCCM enable/disable can be configured. Once the voltage on the EN pin exceeds the EN threshold and power conversion begins, these registers are read only. Configuration settings will be lost if device is allowed to go back into low-power shutdown mode.

When the TPS542A50 detects an individual fault of OCP, OT, OV, or UV, the STATUS register (0x01) asserts a logic high or "1" in its respective bit field. The asserted fault bits will remain high even after the fault is removed. To clear the asserted fault bits, cycle power to the device, or write a logic high to the bit field of the STATUS register for the desired bits to be cleared. Bits can be cleared individually or all at once by writing "0xDE." In the case of both OCP and OT bits detection, they are designed to automatically clear one another. For example, in the case of an OCP fault followed by an OT fault, the OCP will initially assert a logic high, but when the OT is encountered, the OCP will automatically clear to a logic low or "0", and only the OT fault bit will remain asserted as a logic high. If the events are encountered in the reverse order, then only the OCP will remain asserted as a logic high and the OT fault bit will be cleared to a logic low.

7.5.4 Output Voltage Adjustment

The TPS542A50 output voltage can be adjusted in 0.25% increments from –20% to +10% of the set output voltage. This function can only be performed after PGOOD goes high. During programming mode, these registers are read only.

Table 7-9. Higher Output Voltage Adjustment

VSET (V)	VSET LSB (mV)	VOUT ADJUSTMENT TARGET (mV)	VOUT LSB (mV)	VOUT ADJUSTMENT STEP	BINARY CODE	REGISTER BINARY CODE
0.2	VSET divided by 3583 = 0.056	10	0.056 * 5 = 0.28	10 mV divided by 0.28mV = 36	0010 0100	0000 0000 0010 0100
0.2	VSET divided by 3583 = 0.056	50	0.056 * 5 = 0.28	50 mV divided by 0.28mV = 179	1011 0011	0000 0000 1011 0011
0.2	VSET divided by 3583 = 0.056	100	0.056 * 5 = 0.28	100 mV divided by 0.28mV = 358	0001 0110 0110	0000 0001 0110 0110
0.36	VSET divided by 3583 = 0.1	18	0.1 * 5 = 0.5	18 mV divided by 0.5mV = 36	0010 0100	0000 0000 0010 0100
0.36	VSET divided by 3583 = 0.1	90	0.1 * 5 = 0.5	90 mV divided by 0.5mV = 180	1011 0100	0000 0000 1011 0100
0.36	VSET divided by 3583 = 0.1	180	0.1 * 5 = 0.5	180 mV divided by 0.5mV = 360	0001 0110 1000	0000 0001 0110 1000
1	VSET divided by 3583 = 0.28	50	0.28 * 5 = 1.4	50 mV divided by 1.4mV = 36	0010 0100	0000 0000 0010 0100
1	VSET divided by 3583 = 0.28	250	0.28 * 5 = 1.4	250 mV divided by 1.4mV = 179	1011 0011	0000 0000 1011 0011
1	VSET divided by 3583 = 0.28	500	0.28 * 5 = 1.4	500 mV divided by 1.4mV = 358	0001 0110 0110	0000 0001 0110 0110

Table 7-10. Lower Output Voltage Adjustment

VSET (V)	VSET LSB (mV)	VOUT ADJUSTMENT TARGET (MV)	VOUT LSB (mV)	VOUT ADJUSTMENT STEP	BINARY CODE	2's COMPLEMENT BINARY CODE	REGISTER BINARY CODE
0.2	VSET divided by 3583 = 0.056	10	0.056 * 5 = 0.28	10 mV divided by 0.28mV = 36	0010 0100	1101 1100	1111 1111 1101 1100
0.2	VSET divided by 3583 = 0.056	50	0.056 * 5 = 0.28	50 mV divided by 0.28mV = 179	1011 0011	0100 1101	1111 1111 0100 1101
0.2	VSET divided by 3583 = 0.056	100	0.056 * 5 = 0.28	100 mV divided by 0.28mV = 358	0001 0110 0110	1110 1001 1010	1111 1110 1001 1010
0.2	VSET divided by 3583 = 0.056	200	0.056 * 5 = 0.28	200 mV divided by 0.28mV = 717	0010 1100 1101	1101 0011 0011	1111 1101 0011 0011
0.36	VSET divided by 3583 = 0.1	18	0.1 * 5 = 0.5	18 mV divided by 0.5mV = 36	0010 0100	1101 1100	1111 1111 1101 1100
0.36	VSET divided by 3583 = 0.1	90	0.1 * 5 = 0.5	90 mV divided by 0.5mV = 180	1011 0100	0100 1100	1111 1111 0100 1100
0.36	VSET divided by 3583 = 0.1	180	0.1 * 5 = 0.5	180 mV divided by 0.5mV = 360	0001 0110 1000	1110 1001 1000	1111 1110 1001 1000

Product Folder Links: *TPS542A50*

Table 7-10. Lower Output Voltage Adjustment (continued)

VSET (V)	VSET LSB (mV)	VOUT ADJUSTMENT TARGET (MV)	VOUT LSB (mV)	VOUT ADJUSTMENT STEP	BINARY CODE	2's COMPLEMENT BINARY CODE	REGISTER BINARY CODE
0.36	VSET divided by 3583 = 0.1	360	0.1 * 5 = 0.5	360 mV divided by 0.5mV = 720	0010 1101 0000	1101 0011 0000	1111 1101 0011 0000
1	VSET divided by 3583 = 0.28	50	0.28 * 5 = 1.4	50 mV divided by 1.4mV = 36	0010 0100	1101 1100	1111 1111 1101 1100
1	VSET divided by 3583 = 0.28	250	0.28 * 5 = 1.4	250 mV divided by 1.4mV = 179	1011 0011	1011 0011	1111 1111 0100 1101
1	VSET divided by 3583 = 0.28	500	0.28 * 5 = 1.4	500 mV divided by 1.4mV = 358	0001 0110 0110	1110 1001 1010	1111 1110 1001 1010
1	VSET divided by 3583 = 0.28	1000	0.28 * 5 = 1.4	1000 mV divided by 1.4mV = 714	0010 1100 1010	1101 0011 0110	1111 1101 0011 0110

7.6 Pin-Strap Programming

Table 7-11 and Table 7-12 provide the binary code for these pin-strap pins.

Table 7-11. Pin-Strap Programming 1

R_{ILIM} (kΩ)	R_{FSEL} (kΩ)	BINARY CODE
10	10	000
16.2	16.2	001
23.7	23.7	010
33.2	33.2	011
44.2	44.2	100
61.9	61.9	101
N/A	82.5	110
N/A	N/A	111

Table 7-12. Pin-Strap Programming 2

$R_{SS/PFM}$ (kΩ)	BINARY CODE	COMPENSATION SETTING	I²C ADDRESS	BINARY CODE
10	00	COMP 1	0x60	00
16.2	01	COMP 2		01
23.7	10	COMP 3		10
33.2	11	COMP 4		11
44.2	00	COMP 1	0x61	00
61.9	01	COMP 2		01
82.5	10	COMP 3		10
100	11	COMP 4		11

7.7 Register Maps

Table 7-13 lists the memory-mapped registers for the Device registers. All register offset addresses not listed in Table 7-13 should be considered as reserved locations and the register contents should not be modified.

Table 7-13. Device Registers

Offset	Acronym	Register Name	Section
0x0	ID		Go
0x1	STATUS		Go
0x2	VOUT_ADJ1		Go

Table 7-13. Device Registers (continued)

Offset	Acronym	Register Name	Section
0x3	VOUT_ADJ2		Go
0x4	CONFIG1		Go
0x5	CONFIG2		Go

Complex bit access types are encoded to fit into small table cells. Table 7-14 shows the codes that are used for access types in this section.

Table 7-14. Device Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.7.1 ID Register (Offset = 0x0) [reset = 0x21]

ID is shown in Figure 7-2 and described in Table 7-15.

Return to Summary Table.

Figure 7-2. ID Register

7	6	5	4	3	2	1	0
IC_Revision							
R-0x21							

Table 7-15. ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	IC_Revision	R	0x21	IC Revision

7.7.2 STATUS Register (Offset = 0x1) [reset = 0x0]

STATUS is shown in Figure 7-3 and described in Table 7-16.

Return to Summary Table.

Figure 7-3. STATUS Register

7	6	5	4	3	2	1	0
RESERVED			OT_FAULT	OC_FAULT	OV_FAULT	UV_FAULT	PGOOD
R-0x0			R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0

Table 7-16. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4	OT_FAULT	R/W	0x0	Overtemperature Fault Flag
3	OC_FAULT	R/W	0x0	Overcurrent Fault Flag
2	OV_FAULT	R/W	0x0	Output Overvoltage Fault Flag
1	UV_FAULT	R/W	0x0	Output Undervoltage Fault Flag
0	PGOOD	R/W	0x0	Power Good Indicator

7.7.3 VOUT_ADJ1 Register (Offset = 0x2) [reset = 0x0]

VOUT_ADJ1 is shown in Figure 7-4 and described in Table 7-17.

Return to Summary Table.

Figure 7-4. VOUT_ADJ1 Register

7	6	5	4	3	2	1	0
RESERVED				VOUT_ADJ			
R-0x0				R/W-0x0			

Table 7-17. VOUT_ADJ1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	Reserved
3-0	VOUT_ADJ	R/W	0x0	Output Voltage Adjustment Most Significant Bits

7.7.4 VOUT_ADJ2 Register (Offset = 0x3) [reset = 0x0]

VOUT_ADJ2 is shown in Figure 7-5 and described in Table 7-18.

Return to Summary Table.

Figure 7-5. VOUT_ADJ2 Register

7	6	5	4	3	2	1	0
VOUT_ADJ							
R/W-0x0							

Table 7-18. VOUT_ADJ2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	VOUT_ADJ	R/W	0x0	Output Voltage Adjustment Least Significant Bits

7.7.5 CONFIG1 Register (Offset = 0x4) [reset = 0x0B]

CONFIG1 is shown in Figure 7-6 and described in Table 7-19.

Return to Summary Table.

Figure 7-6. CONFIG1 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	COMP		FSW		
R-0x0	R-0x0	R-0x0	R/W-0x1		R/W-0x3		

Table 7-19. CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4-3	COMP	R/W	0x1	Internal Compensation
2-0	FSW	R/W	0x3	Switching Frequency

7.7.6 CONFIG2 Register (Offset = 0x5) [reset = 0x2D]

CONFIG2 is shown in Figure 7-7 and described in Table 7-20.

Return to Summary Table.

Figure 7-7. CONFIG2 Register

7	6	5	4	3	2	1	0
RESERVED		ILIM			FCCM	SS	
R-0x0		R/W-0x3			R/W-0x1	R/W-0x1	

Table 7-20. CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved
5-3	ILIM	R/W	0x3	Overcurrent Limit
2	FCCM	R/W	0x1	Force Continuous Conduction Mode
1-0	SS	R/W	0x1	Soft Start Rate

Product Folder Links: *TPS542A50*

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS542A50 is a high-efficiency, single-channel, synchronous buck converter with integrated n-channel MOSFETs. The device suits low-output voltage point-of-load applications with 15-A or lower current. The TPS542A50 has a maximum operating junction temperature of 150°C, which makes it suitable for high-ambient temperature applications such as wireless infrastructure. The input voltage range is 4 V to 18 V, and the output voltage range is 0.5 V to 5.5 V. The device features a fixed-frequency voltage-control mode with a switching frequency range of 400 kHz to 2.2 MHz, allowing for efficiency and size optimization when selecting output filter components. The controller features selectable internal compensation making the device easy to use with a low external-component count. The internal compensation networks are able to support a wide range of output inductance and capacitance, supporting all types of capacitors. The controller utilizes a digital PWM modulator that allows for very narrow on-times making it ideal for high-frequency and high-step down ratio applications. The switching frequency of the device can be synchronized to an external clock applied to the SYNC pin. The TPS542A50 also features an I^2C interface for device configuration and output voltage adjustments.

8.2 Typical Application

8.2.1 Full Analog Configuration

A resistor to ground on the FSEL, COMP, SS/PFM, and ILIM pins configure the device. Any of these pins can be grounded to use the default values and reduce component count.
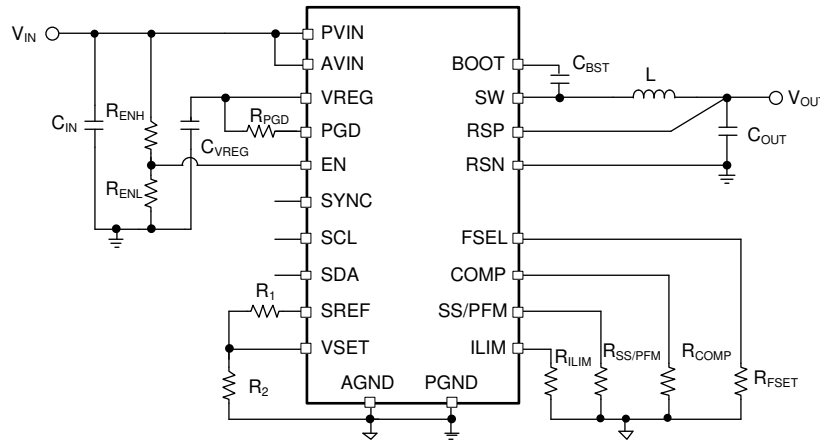

Figure 8-1. Full Analog Configuration

8.2.1.1 Design Requirements

For this design example, use the input parameters shown in Table 8-1.

Table 8-1. Design Example Specifications

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN}, Input Voltage		9	12	14	V
$V_{IN(ripple)}$, Input Ripple Voltage				0.2	V
V_{OUT}, Output Voltage			1		V
V_{PP}, Ouput Ripple Voltage			15		mV

Table 8-1. Design Example Specifications (continued)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{OVER}, Transient Response Overshoot	I_{STEP} = 5 A at 1 A/µs		30		mV
V_{UNDER}, Transient Response Undershoot	I_{STEP} = 5 A at 1 A/µs		30		mV
I_{OUT}, Output Current			10		A
I_{OC}, Over-Current Trip Point			16		A
F_{SW}, Switching Frequency			1.2		MHz
t_{SS}, Soft-start time			0.5		ms

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS542A50 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:
*   Run electrical simulations to see important waveforms and circuit performance
*   Run thermal simulations to understand board thermal performance
*   Export customized schematic and layout into popular CAD formats
*   Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.1.2.2 Output Voltage Calculation

The output voltage equals five times of VSET. To set VSET voltage, a resistor divider network is required from SREF (1.2 V). Equation 2 shows the output voltage calculation. It is recommended to use R_1 and R_2 in the range of 1 kΩ to 100 kΩ. For example, R_1 equals 50 kΩ and R_2 equals 10 kΩ for 1-V output voltage.

$$V_{OUT} = 5 \times VSET$$
$$VSET = \frac{R2}{R1 + R2} \times 1.2$$
$$V_{OUT} = 5 \times \frac{R2}{R1 + R2} \times 1.2$$

(2)

8.2.1.2.3 Switching Frequency Selection

There is a trade off between higher and lower switching frequencies. Higher switching frequencies can produce a smaller solution size using lower valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. However, the higher switching frequency causes extra switching losses, which decreases efficiency and impacts thermal performance. In this design, a moderate switching frequency of 1.2 MHz that achieves both a small solution size and a high efficiency operation is selected. TPS542A50 offers seven choices of switching frequency in Table 7-1. RFSET equals to 44.2 kΩ for 1.2-MHz switching frequency.

8.2.1.2.4 Inductor Selection

The inductor value is a compromise between having a good load step transient response, output ripple voltage, and efficiency. A good practice is to select the inductor ripple current value between 15% to 50% of the maximum output current. The output capacitor absorbs the inductor-ripple current. Therefore, selecting a high inductor-ripple current impacts the selection of the output capacitor because the output capacitor must have a

ripple-current rating equal to or greater than the inductor-ripple current. Using 35% target ripple current, the required inductor size can be calculated as shown in Equation 3.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times I_{OUT} \times 0.35} = \frac{1.0\ V \times (12\ V - 1.0\ V)}{12\ V \times 1.2\ MHz \times 10\ A \times 0.35} = 218\ nH \tag{3}$$

A standard inductor value of 220 nH is selected.

8.2.1.2.5 Input Capacitor Selection

The TPS542A50 requires a high-quality, ceramic, type X5R or X7R, input decoupling capacitor with a value of at least 1 µF of effective capacitance on the PVIN pin, relative to PGND. The power stage input decoupling capacitance (effective capacitance at the PVIN and PGND pins) must be sufficient to supply the high switching currents demanded when the high-side MOSFET switches on, while providing minimal input voltage ripple as a result. This effective capacitance includes any DC bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple to the device during full load. The input ripple current can be calculated by Equation 4.

$$I_{CIN(rms)} = I_{OUT(max)} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \frac{(V_{IN} - V_{OUT})}{V_{IN}}} = 2.8\ Amps \tag{4}$$

The minimum input capacitance and ESR values for a given input voltage ripple specification, $V_{IN(ripple)}$, are shown in Equation 5. The input ripple is composed of a capacitive portion, $V_{IN(RIPPLE\_CAP)}$, and a resistive portion, $V_{IN(RIPPLE\_ESR)}$.

$$C_{IN(min)} = \frac{I_{OUT(max)} \times (1-D) \times D}{V_{IN(RIPPLE\_CAP)} \times f_{SW}} = 6.4\ \mu F$$

$$ESR_{CIN(max)} = \frac{V_{IN(RIPPLE\_ESR)}}{I_{OUT(max)} + \frac{I_{RIPPLE}}{2}} = 8.5\ m\Omega$$

where

- D is the duty cycle

(5)

The value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power regulator capacitors because they have a high capacitance to volume ratio and are fairly stable over temperature. The input capacitor must also be selected with the DC bias taken into account. For this example design, a ceramic capacitor with at least a 25-V voltage rating is required to support the maximum input voltage. For this design, allow 0.1-V input ripple for $V_{IN(RIPPLE\_CAP)}$, and 0.1-V input ripple for $V_{IN(RIPPLE\_ESR)}$. Using Equation 5, the minimum input capacitance for this design is 6.4 µF, and the maximum ESR is 8.5 mΩ. In a real application, it is recommended to use a combination of small capacitors such as 0.1 µF and larger value 10-µF or 22-µF ceramic capacitors in parallel for the power stage.

8.2.1.2.6 Bootstrap Capacitor Selection

A ceramic capacitor with a value of 0.1 µF must be connected between the BOOT and SW pins for proper operation. It is recommended to use a ceramic capacitor with X5R or better grade dielectric. Use a capacitor with a voltage rating of 25 V or higher.

8.2.1.2.7 R-C Snubber and VIN Pin High-Frequency Bypass

Though it is possible to operate the TPS542A50 within absolute maximum ratings without voltage ringing reduction techniques, some designs may require external components to further reduce ringing levels. This

example uses two approaches: a high frequency power stage bypass capacitor on the VIN pins, and an R-C snubber between the SW area and GND.

The high-frequency VIN bypass capacitor is a lossless ringing reduction technique which helps minimize the outboard parasitic inductances in the power stage, which store energy during the high-side MOSFET on-time, and discharge once the high-side MOSFET is turned off. For this example two of 0.1-µF to 1-µF, 25-V, 0402-sized high-frequency capacitors are used. The placement of these capacitors is critical to its effectiveness.

Additionally, an optional R-C snubber circuit is added to this example. To balance efficiency and spike levels, a 220-pF capacitor and a 2-Ω resistor are chosen. In this example, a 0805-sized resistor is chosen, which is rated for 0.125 W, nearly twice the estimated power dissipation. See the *Seminar 900 Topic 2 - Snubber Circuits: Theory, Design and Application* application note for more information about snubber circuits.

8.2.1.2.8 Output Capacitor Selection

There are three primary considerations for selecting the value of the output capacitor. The output capacitor affects three criteria:

- Stability
- Regulator response to a change in load current or load transient
- Output voltage ripple

These three considerations are important when designing regulators that must operate where the electrical conditions are unpredictable. The output capacitance needs to be selected based on the most stringent of these three criteria.

8.2.1.2.9 Response to a Load Transient

The output capacitance must supply the load with the required current when current is not immediately provided by the regulator. When the output capacitor supplies load current, the impedance of the capacitor greatly affects the magnitude of voltage deviation (such as undershoot and overshoot) during the transient.

Use Equation 6 and Equation 7 to calculate the minimum output capacitance to meet the undershoot and overshoot requirements. For this example, $C_{OUT(min\_under)}$ is 136 µF and 92 µF for $C_{OUT(min\_over)}$. In a real application, the value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. It is recommended to check the capacitor datasheet and account for the capacitance derating.

$$C_{OUT(min\_under)} = \frac{L \times \Delta I_{LOAD(max)}^2}{2 \times \Delta V_{LOAD(INSERT)} \times (V_{IN}\text{-}V_{VOUT})} + \frac{\Delta I_{LOAD(max)} \times (1-D) \times t_{SW}}{\Delta V_{LOAD(INSERT)}}$$

(6)

$$C_{OUT(min\_over)} = \frac{L_{OUT} \times (\Delta I_{LOAD(max)})^2}{2 \times \Delta V_{LOAD(release)} \times V_{OUT}}$$

(7)

where

- $C_{OUT(min\_under)}$ is the minimum output capacitance to meet the undershoot requirement
- $C_{OUT(min\_over)}$ is the minimum output capacitance to meet the overshoot requirement
- D is the duty cycle
- L is the output inductance value (0.22 µH)
- $\Delta I_{LOAD(max)}$ is the maximum transient step (5 A)
- V_{OUT} is the output voltage value (1 V)
- t_{SW} is the switching period (0.833 µs)
- V_{IN} is the minimum input voltage for the design (12 V)
- $\Delta V_{LOAD(insert)}$ is the undershoot requirement (30 mV)
- $\Delta V_{LOAD(release)}$ is the overshoot requirement (30 mV)

Product Folder Links: *TPS542A50*

8.2.1.2.10 Pin-Strap Setting

For overcurrent protection at 16.5 A, 44.2 kΩ is chosen from Table 7-7. For 0.5-ms soft start and FCCM operation, 44.2 kΩ is chosen from Table 7-5 and Table 7-6.

For converter stability and selecting the compensation network, Table 7-3 provides four compensation choices. First, the power stage double pole filter frequency needs to be known. For this example, the output capacitor bank selects as 4x100-µF ceramic capacitors in 0805 size to account the capacitor de-rate factors. Next, the LC filter frequency is calculated to 17 kHz. Finally, COMP3 becomes the best choice to select by using a 23.7-kΩ or 82.5-kΩ resistor on the COMP pin to GND.

8.2.1.3 Application Curves

V$_{IN}$ = 12 V   V$_{OUT}$ = 1 V   f$_{SW}$ = 1.2 MHz
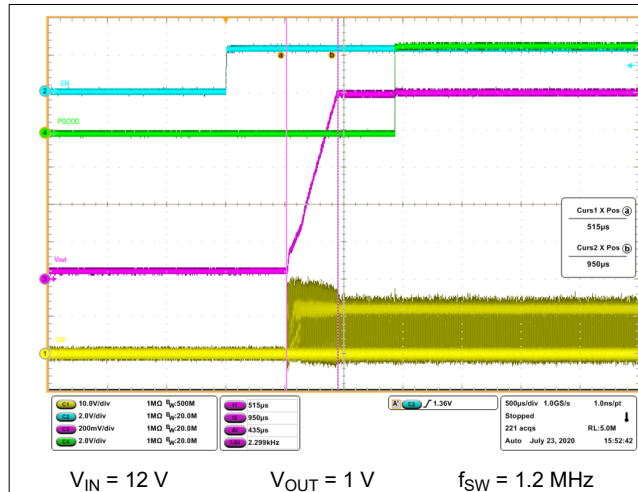
Figure 8-2. 450 µs Start-up by EN at 0-A Output Current

V$_{IN}$ = 12 V   V$_{OUT}$ = 1 V   f$_{SW}$ = 1.2 MHz
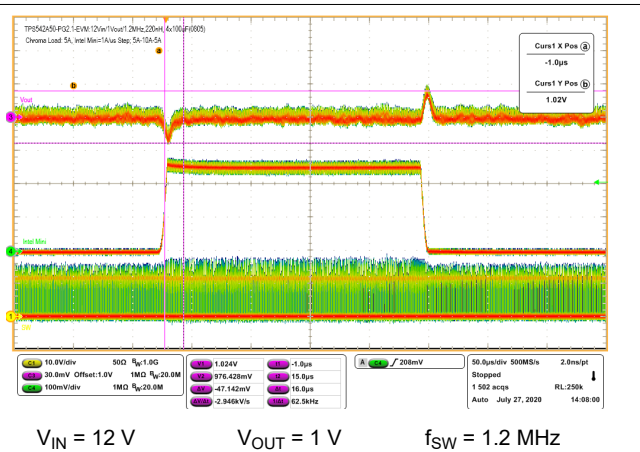
Figure 8-3. Load Transient 5 A to 10 A to 5 A at 1 A/µs

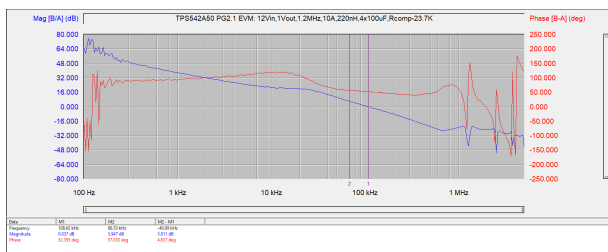V$_{IN}$ = 12 V   V$_{OUT}$ = 1 V   f$_{SW}$ = 1.2 MHz

Figure 8-4. Bode Plot at 10-A Output Current

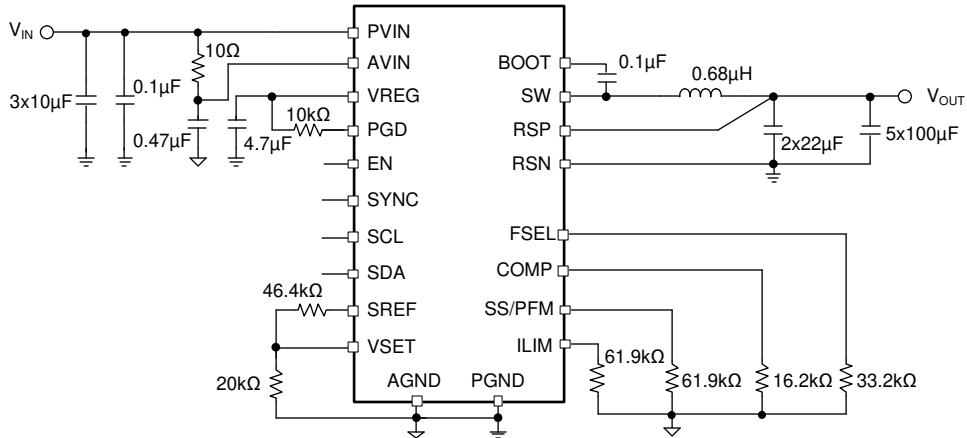### 8.2.1.4 Typical Application Circuits

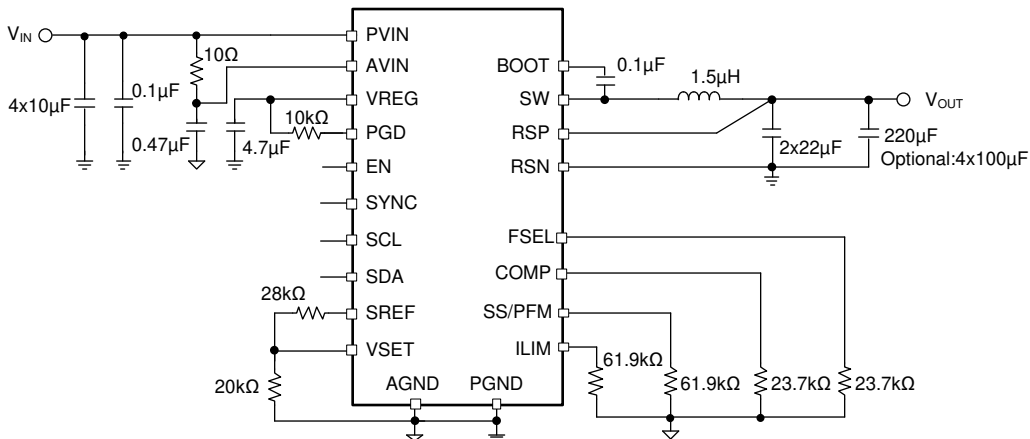**Figure 8-5. Typical Application Circuit for 1.8-V Output at 1.0 MHz**

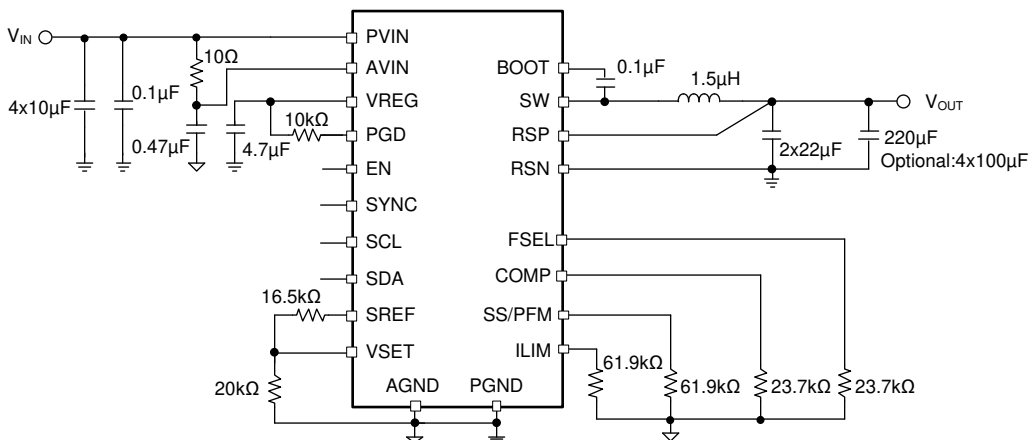**Figure 8-6. Typical Application Circuit for 2.5-V Output at 0.8 MHz**

Figure 8-7. Typical Application Circuit for 3.3-V Output at 0.8 MHz
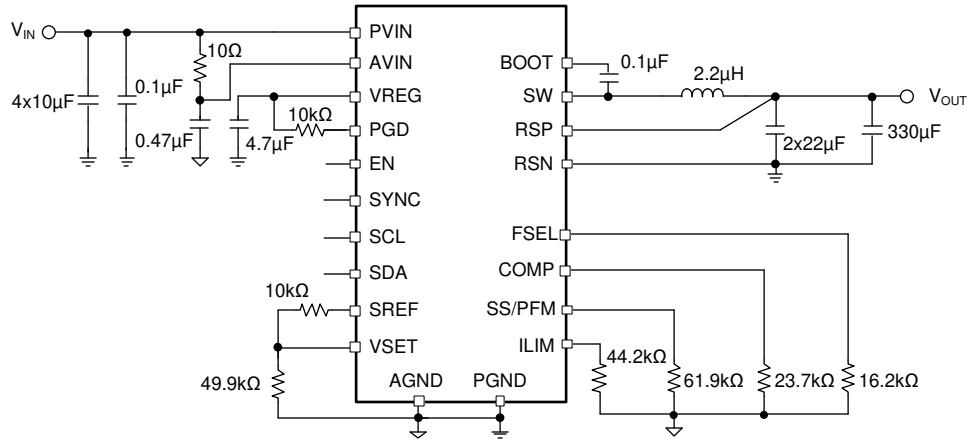
Product Folder Links: *TPS542A50*

Figure 8-8. Typical Application Circuit for 5-V Output at 0.6 MHz

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 4 V and 18 V. This input supply must be well regulated. Proper bypassing of input supplies (AVIN and PVIN) is critical for noise performance, as is the PCB layout and grounding scheme. See the recommendations in *Section 10*.

Product Folder Links: *TPS542A50*

10 Layout

10.1 Layout Guidelines

- The PVIN pins are the power inputs to the main half bridge and AVIN is the power input to the controller.
- Connect AVIN and PVIN together on the PCB. It is important that these pins are at the same voltage potential because the controller feedforward block uses this voltage information in the modulator to increase transient performance. For AVIN, it is best to use RC filter from PVIN such as 10-Ω and 100 nF.
- To minimize the power loop inductance for the half bridge, place the bypassing capacitors as close as possible to the PVIN pins on the converter. When using a multilayer PCB (more than two layers), the power loop inductance is minimized by having the return path to the input capacitor small and directly underneath the first layer as shown below. Loop inductance is reduced due to flux cancellation as the return current is directly underneath and flowing in the opposite direction.
- Place the bias capacitor for VREG pin as close as possible to the pin as shown below.
- The resistor divider network for SREF and VSET needs to placed as close as possible to the pins. Limit the high frequency noise source coupling onto these components.
- RSP and RSN signals are best to route parallel to the load sense location. It is recommended to limit high frequency noise source coupling onto these traces.
- PGND thermal vias: It is recommended to add vias under and outside the IC of PGND plane as shown below.
- AGND thermal vias: It is recommended to add at least two vias under the IC of AGND plane as shown below.
- AGND plane can be routed as a separate island in an internal layer. AGND can connect as a net tied to PGND between the two thermal grounds under the IC as shown below.
- Total PCB area can be routed in 17 mm by 14 mm as shown below. See the *Using the TPS542A50EVM-059* user's guide for more details.
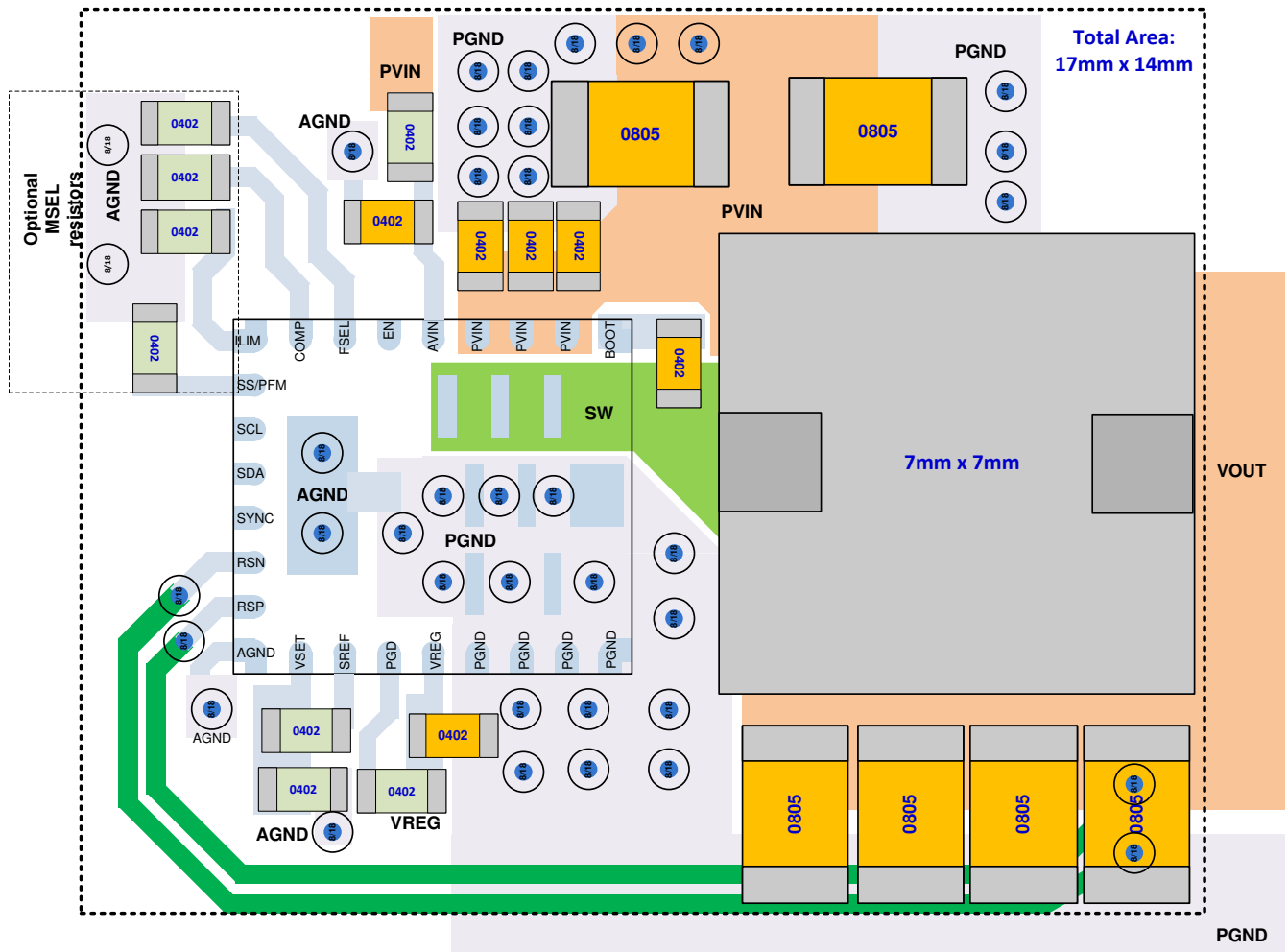
10.2 Layout Example

Figure 10-1. Example PCB Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS542A50 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:
• Run electrical simulations to see important waveforms and circuit performance
• Run thermal simulations to understand board thermal performance
• Export customized schematic and layout into popular CAD formats
• Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.4 Trademarks

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All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

Product Folder Links: TPS542A50

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: *TPS542A50*

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS542A50RJMR	ACTIVE	VQFN-HR	RJM	33	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	542A50	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
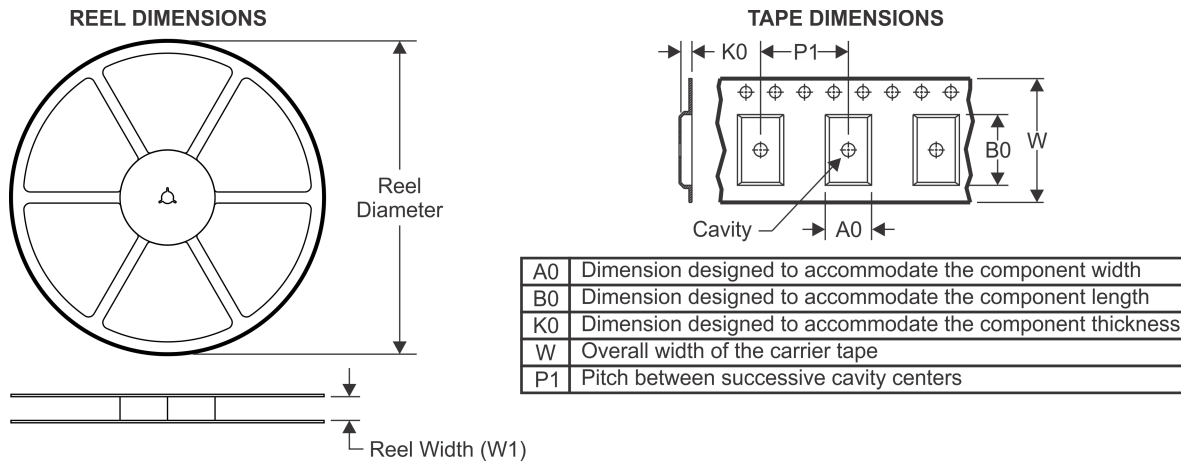
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS542A50RJMR	VQFN-HR	RJM	33	3000	330.0	12.4	4.25	4.75	1.2	8.0	12.0	Q3

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS542A50RJMR	VQFN-HR	RJM	33	3000	367.0	367.0	38.0

A | 4.6 / 4.4 | B

PIN 1 INDEX AREA

4.1 / 3.9

1 MAX

0.05 / 0.00

C

SEATING PLANE

0.08 C

2X 3.5

0.95± 0.1

7X 0.175± 0.05
PKG ₵

(2X 0.375)

(0.127) TYP

21X 0.5

8

9

16

4X (0.2)

32   33

0.388± 0.1

5X 1

3.5

2.05± 0.1

25

29   30   31

PKG ₵

26   27   28

8X 0.7± 0.1

PIN 1 ID

1

24

17

24X 0.3 / 0.2

(2X 0.375)

24X 0.4 / 0.3

1.225

0.000

0.3   0.6   0.9   1.2   1.5

1.906

2X   2X

0.1 Ⓜ C A B

0.05 Ⓜ
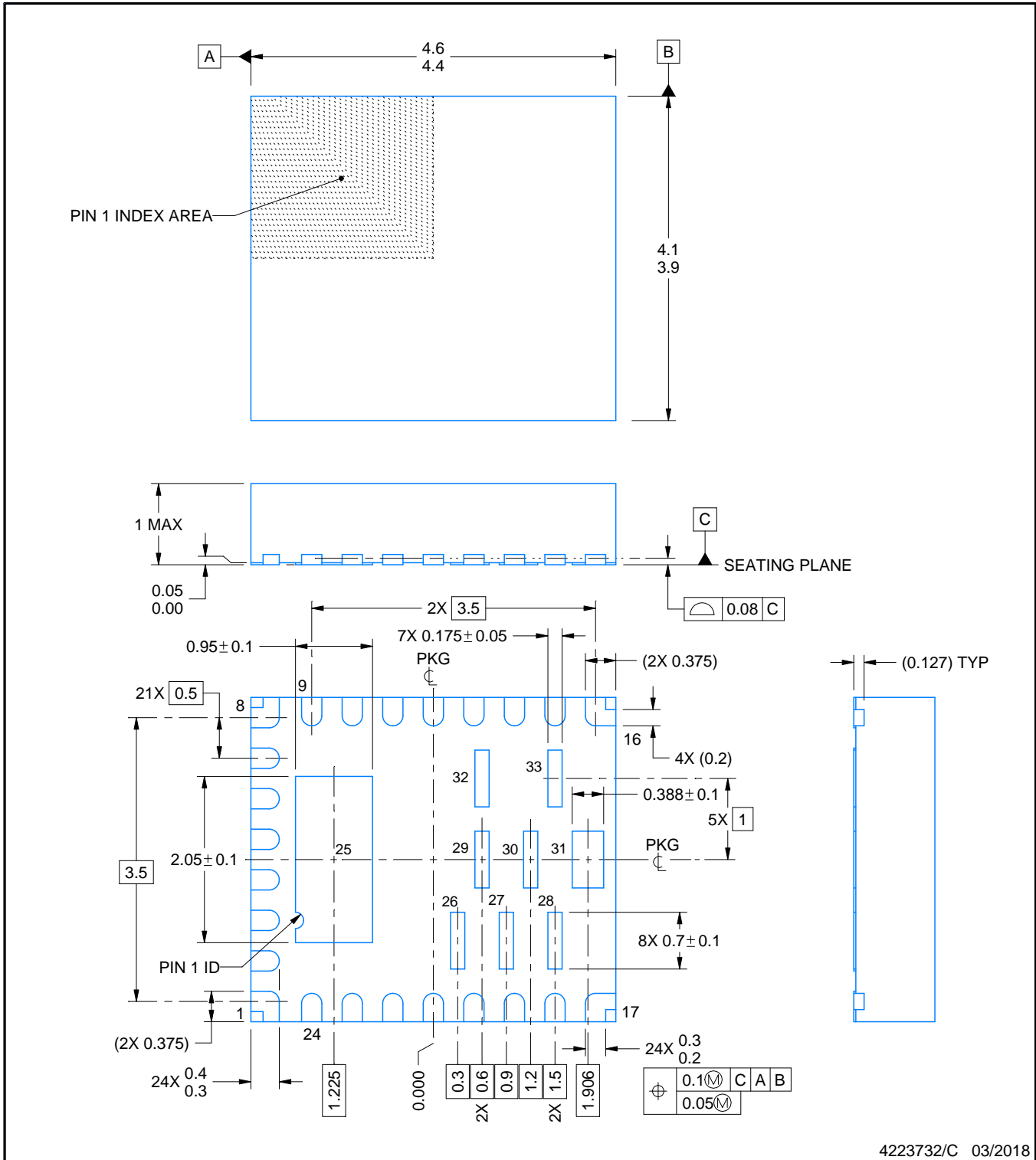
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

TEXAS INSTRUMENTS
www.ti.com

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

0.07 MAX
ALL AROUND

METAL EDGE

EXPOSED METAL

SOLDER MASK
OPENING

NON SOLDER MASK
DEFINED
(PREFERRED)

0.07 MIN
ALL AROUND

SOLDER MASK
OPENING

EXPOSED METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 1, 8, 16, 17: 95%; PADS 25-33: 80%
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.