MCP1633

Low-Side PWM Controller with LED Dimming Capability

Features

- High Speed Current Mode Pulse-Width Modulator (PWM) Controller
- Easy to Interface with PIC® Microcontroller for Implementing High-Performance LED Drivers
- Integrated General Purpose Operational Amplifier that can be Used for Current Sensing
- Internal Oscillator with Adjustable Frequency via External Resistor
- External Synchronization Option for the Oscillator
- Internal Slope Compensation Circuit
- Current Sense to V_{EXT} Response <120 ns Typical
- Internal Leading Edge Blanking Circuit for Current Sense Input
- Programmable Current Sense Offset
- Internal Reference Voltage Generator
- Soft Start Capability
- Internal Push-Pull MOSFET Driver with 1A Peak Current Capability
- Internal MOSFET Driver for Dimming/Load Disconnect
- Input Voltage Range: 3V to 5.5V
- Undervoltage Lockout Circuit
- Output Overvoltage Protection
- Output Short Circuit Protection
- Overtemperature Protection
- Small 16-Pin QFN 3 x 3 mm Package

Applications

- LED Drivers
- Switch Mode Power Supplies
- Brick DC-DC Converters

General Description

The MCP1633 High Speed PWM Controller is a pulse-width modulator developed for standalone power supply applications. The MCP1633 design is based on the MCP1632 PWM Controller but includes specific blocks for PWM LED dimming. It is suitable for use in topologies requiring a low side MOSFET, such as Boost, Flyback, SEPIC, CUK, etc.

The MCP1633 uses Current Mode Control to provide superior bandwidth and transient response, and also cycle-by-cycle current limiting with adjustable peak offset. The MCP1633 is also capable of operating in Voltage Mode Control if required.

The switching frequency of the MCP1633 can be set by an external resistor between 200 kHz and 2.2 MHz.

The MCP1633 reference voltage is adjustable by using only one external resistor.

The MCP1633 integrates a current sense amplifier with programmable gain using external resistors.

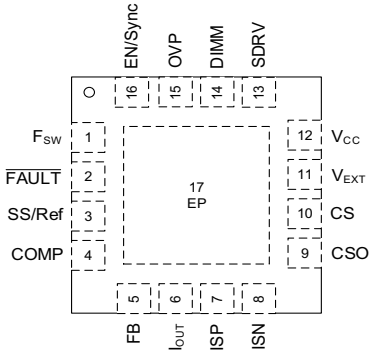
The MCP1633 can achieve high performance LED dimming by “freezing” the compensation network and load disconnect capability.

The MCP1633 integrates a high speed comparator with a high performance error amplifier with a PWM latch to perform the high speed analog Power Supply PWM function.

Integrated Undervoltage Lockout, Overvoltage protection and Overtemperature Protection make designs using the MCP1633 robust over a range of external conditions.

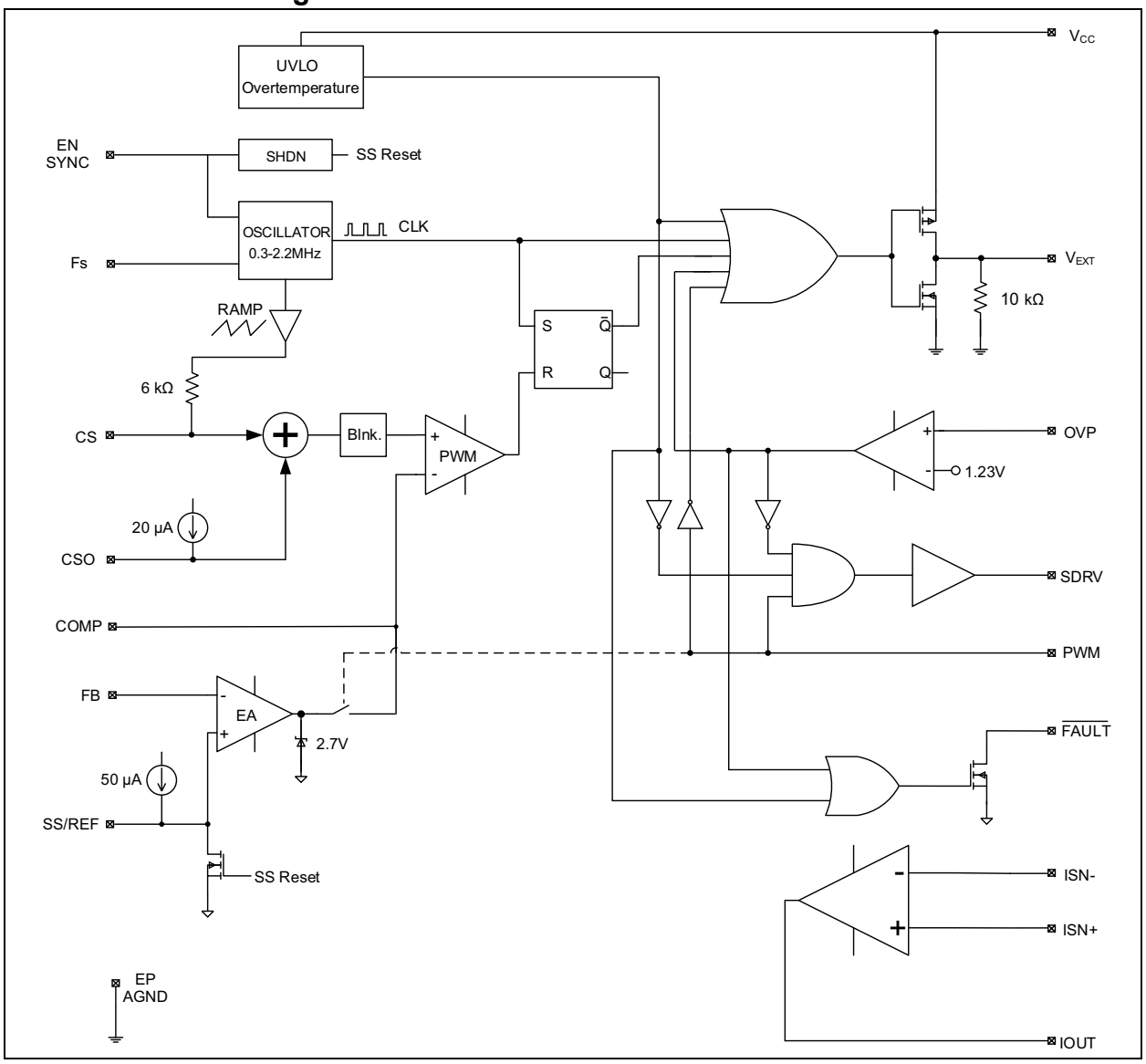
Package Type

3 x 3 x 0.9 mm QFN

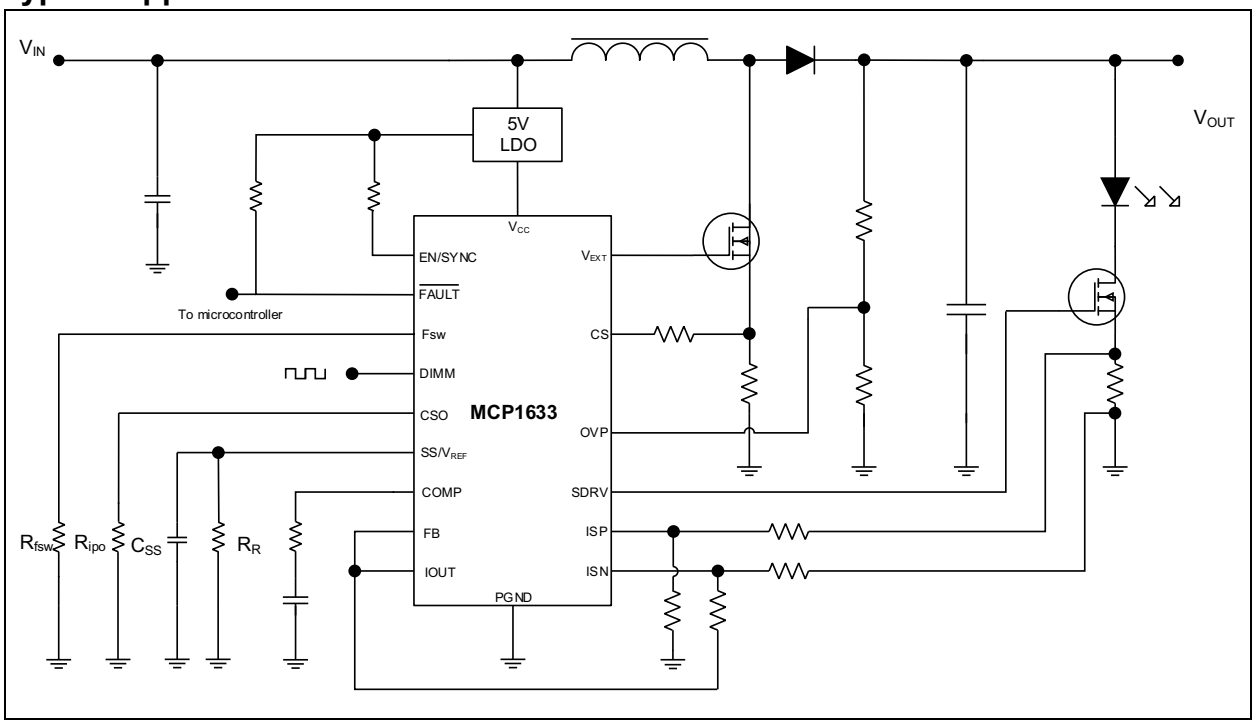


See Table 3-1 for pin information

Functional Block Diagram



Typical Application for LED Driver



1.0 ELECTRICAL CHARACTERISTICS

1.1 Absolute Maximum Ratings†

V_{DD}.....6V
Maximum Voltage on Any Pin .....(V_{GND}-0.3)V to (V_{IN}+0.3)V
V_{EXT} Short Circuit Current .....Internally Limited
Storage Temperature .....-65°C to +150°C
Maximum Junction Temperature .....+150°C
Operating Junction Temperature.....-40°C to +125°C
ESD protection on all pins (HBM) .....2 kV

†Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, during characterization, V_{IN} = 3.3V to 5.5V, F_{SW} = 600 kHz with CIN = 1.0 µF, T_A = +25°C, T_A = -40°C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Inputs						
Input Operating Voltage	V_{IN}	**3**	—	**5.5**	V	
Input Quiescent Current	$I(V_{IN})$	—	5	**5.75**	mA	I_{EXT} = 0 mA, V_{dd}=5V, F_{sw}=1200 kHz
Shutdown Current	I_{IN_SHDN}	—	—	1	µA	EN = 0V
EN Input						
EN Input Voltage Low	EN_{LOW}	—	—	0.8	V	
EN Input Voltage High	EN_{HIGH}	**75**	—	—	% of V_{IN}	
Oscillator						
Internal Oscillator Range	F_{OSC}	**200**	—	**2200**	kHz	Refer to **Section 4.6 "Internal Oscillator"** for details
F_{SW} Output Voltage	V_{RFSW}	0	—	3	V	
External Synchronization Signal Frequency Rage	F_{SYNC}	200	—	2500	kHz	
SYNC Signal Low Voltage	V_{SYNCL}	—	—	0.8	V	
SYNC Signal High Voltage	V_{SYNCH}	2	—	—	V	
SYNC Signal Time Low	T_{SYNC_MAX}	—	10	—	ns	Note 1
SYNC Signal Time High	T_{SYNC_MIN}	—	10	—	ns	Note 1
SYNC Signal Rise/Fall Time	$T_{SYNC\ RISE/FALL}$	0.001	—	10	us	Note 1
Error Amplifier						
Input Voltage Offset	V_{OS}	-7.5	—	7.5	mV	
Error Amplifier PSRR	PSRR	80	—	—	dB	V_{IN} = +5V
Common Mode Input Range	V_{CM}	0	—	2	V	
Common Mode Rejection Ratio	CMRR	60	—	—	dB	V_{CM} = 0 to 2V (Note 1)
Transconductance	g_m	160	200	240	µS	V_{CM} = 0 to 2V
Output Source Current	$I_{OSOURCE}$	13	—	—	µA	V_{dd} = 5V
Output Sink Current	I_{OSINK}	13	—	—	µA	V_{dd} = 5V

Note 1: Determined by characterization, not production tested.

DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, during characterization, V_{IN} = 3.3V to 5.5V, F_{SW} = 600 kHz with CIN = 1.0 µF, T_A = +25°C, T_A = -40°C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Gain Bandwidth Product	GBWP	3.5	—	—	MHz	Note 1
Reference Voltage Section						
Reference Voltage Input Voltage	V_{REF}	0	—	3	V	Refer to **Section 4.5 "Reference Voltage Generator"** for details
Internal Constant Current Generator	I_{REF}	48	50	52	µA	Refer to **Section 4.5 "Reference Voltage Generator"** for details
Current Sense Input						
Maximum Input	V_{CS_MAX}	0.85	0.9	0.95	V	
Blanking Time	T_{BLANK}	—	30	—	ns	Note 1
Delay from CS to VEXT	T_{CS_Vext}	—	—	35	ns	Note 1
Current Sense Input Bias Current	I_{CS_B}	—	-0.1	—	µA	Note 1
Current Sense Operational Amplifier						
Input Offset Voltage	V_{OS}	-2.8	—	2.8	mV	
Operational Amplifier PSRR	PSRR	60	—	—	dB	V_{IN} = 5V
Input Bias Current	I_B	—	1	—	nA	Note 1
Common Mode Input Range	V_{CM}	GND - 0.3	—	2	V	
Common Mode Rejection Ratio	CMRR	—	80	—	dB	Note 1
Open Loop Voltage Gain	A_{VOL}	85	—	150	dB	Note 1
Low Level Output	V_O	—	15	20	mV	
Gain Bandwidth Product	GBWP	1.5	2	—	MHz	
Amplifier Sink Current	I_{SINK}	5	10	—	mA	
Amplifier Source Current	I_{SOURCE}	5	10	—	mA	
Pedestal Voltage Generator						
Internal Constant Current Generator	CSO	17.5	20	25	µA	
PWM						
Minimum Duty Cycle	DC_{MIN}	—	—	0	%	
CMaximum Duty Cycle	DC_{MAX}	85	90	98	%	
Slope Compensation Ramp Generator						
Ramp Amplitude	V_{RAMP}	0.8	0.9	1	V_{PP}	
DC Offset Low	—	0.15	0.32	0.45	V	
DC Offset High	—	1.12	1.22	1.32	V	
Ramp Generator Output Impedance	Z_{RG}	5.5	6	6.5	kΩ	
Internal Driver						
R_{DSon} P-Channel	R_{DSonP}	—	—	4.5	Ω	Typical for V_{IN} = 5.0V
R_{DSon} N-Channel	R_{DSonN}	—	—	4.5	Ω	Typical for V_{IN} = 5.0V
V_{EXT} Rise Time	T_{RISE}	—	10	—	ns	CL = 100 pF, V_{IN} = 5.0V (Note 1)
V_{EXT} Fall Time	T_{FALL}	—	10	—	ns	CL = 100 pF, V_{IN} = 5.0V (Note 1)
Input Dimming PWM						

Note 1: Determined by characterization, not production tested.

DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, during characterization, V_{IN} = 3.3V to 5.5V, F_{SW} = 600 kHz with CIN = 1.0 µF, T_A = +25°C, T_A = -40°C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Dimm Signal Low Voltage	V_{DIMM_L}	—	—	0.8	V	
Dimm Signal High Voltage	V_{DIMM_H}	2	—	—	V	
Series MOSFET Driver						
R_{DSon} P-Channel	R_{DSonP}	—	60	—	Ω	
R_{DSon} N-Channel	R_{DSonN}	—	60	—	Ω	
Shut-Down						
Minimum Low Period for EN to Enter in Shut-Down Mode	T_{MIN_EN}	88	100	—	us	
Overvoltage Protection						
Overvoltage Protection Threshold	V_{OVP}	1.19	1.23	1.3	V	
Overvoltage Protection Hysteresis	$V_{OVP-HYS}$	—	50	—	mV	
Undervoltage Lockout						
Undervoltage Protection Threshold	UVLO	—	3	—	V	
Undervoltage Protection Hysteresis	$UVLO_{HYS}$	—	100	—	mV	
Thermal Shutdown						
Thermal Shutdown	T_{SHD}	—	150	—	°C	
Thermal Shutdown Hysteresis	T_{SHD_HYS}	—	20	—	°C	
Fault Indicator						
Open-Drain Fault Indicator	$\overline{FAULT}$	—	—	—	Ω	

Note 1: Determined by characterization, not production tested.

TEMPERATURE SPECIFICATIONS

Electrical Specifications: V_{IN} = 3.0V to 5.5V, F_{OSC} = 600 kHz, C_{IN} = 1.0 µF. T_A = -40°C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Junction Temperature Range	T_A	-40	—	+125	°C	Steady State
Storage Temperature Range	T_A	-65	—	+150	°C	
Maximum Junction Temperature	T_J	—	—	+150	°C	Transient
Thermal Package Resistances						
Thermal Resistance 16L-QFN (3 mm x 3 mm)	θ_{JA}	—	36	—	°C/W	

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, V_{IN} = 5V, FOSC=600 kHZ, CIN=0.1 µF, T_A= +25°C.

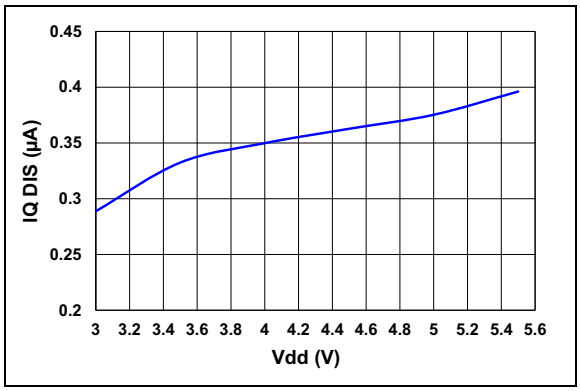


FIGURE 2-1: *Input Quiescent Disable Current vs. Input Voltage.*

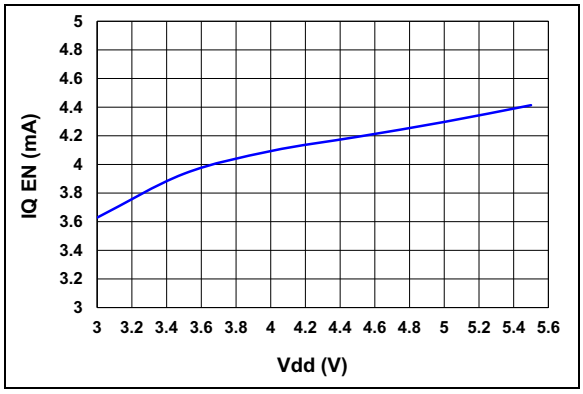


FIGURE 2-2: *Input Quiescent Enable Current vs. Input Voltage.*

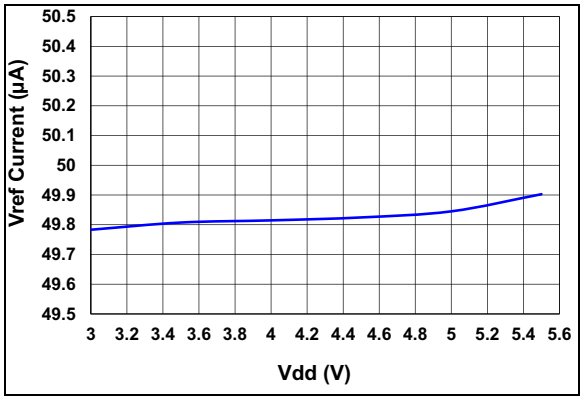


FIGURE 2-3: *VREF Current vs. Input Voltage.*

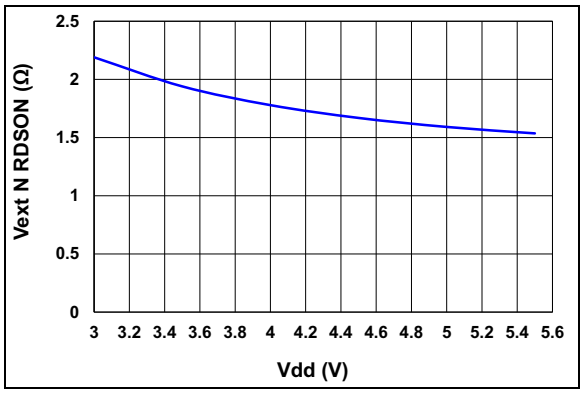


FIGURE 2-4: *Vext N-Channel RDSON vs. Input Voltage.*

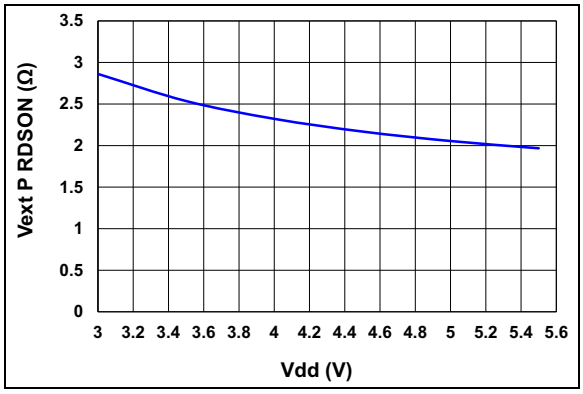


FIGURE 2-5: *Vext P-Channel RDSON vs. Input Voltage.*

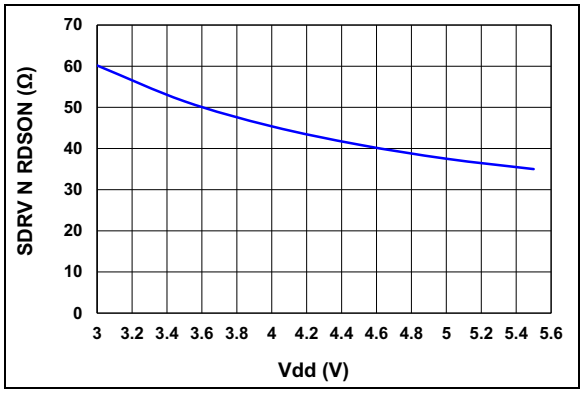


FIGURE 2-6: *SRDV N-Channel RDSON vs. Input Voltage.*

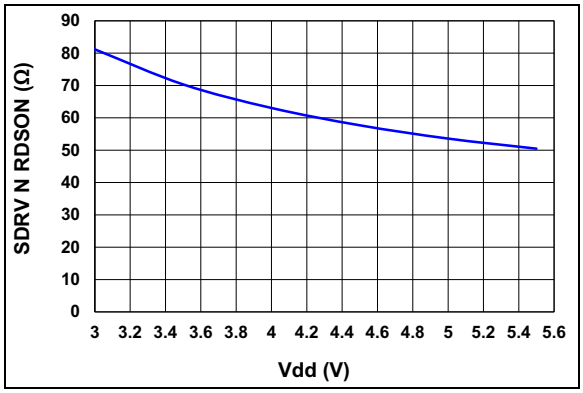


FIGURE 2-7: *SRDV P-Channel RDSON vs. Input Voltage.*

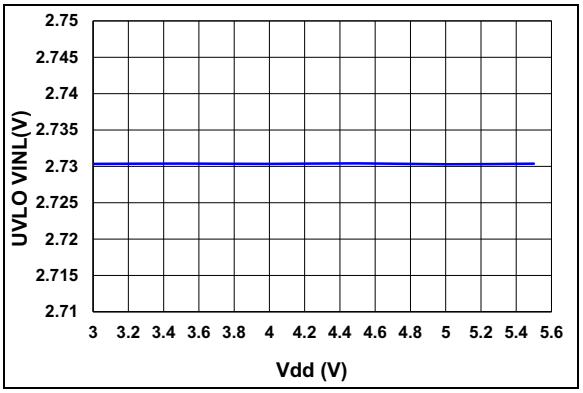


FIGURE 2-10: *UVLO VINL Threshold vs. Input Voltage.*

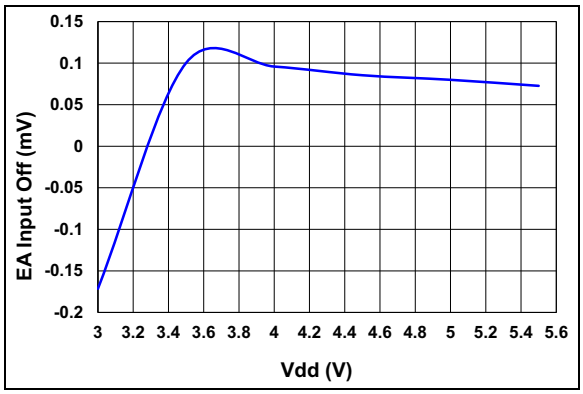


FIGURE 2-8: *Error Amplifier Input Offset vs. Input Voltage.*

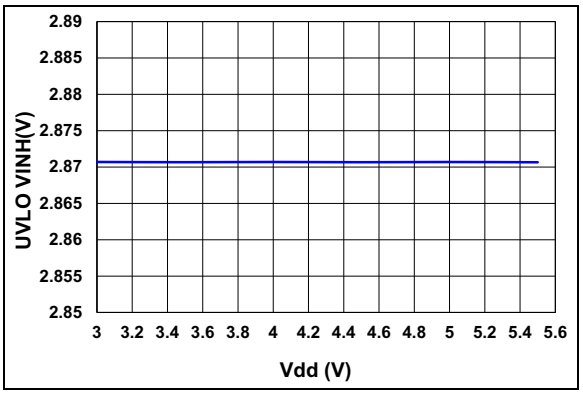


FIGURE 2-11: *UVLO VINH Threshold vs. Input Voltage.*

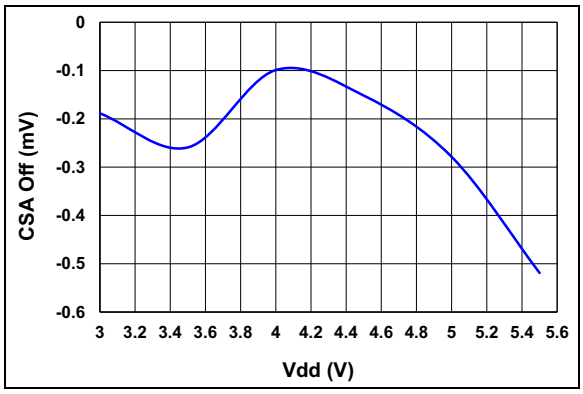


FIGURE 2-9: *Current Sense Amplifier Offset vs. Input Voltage.*

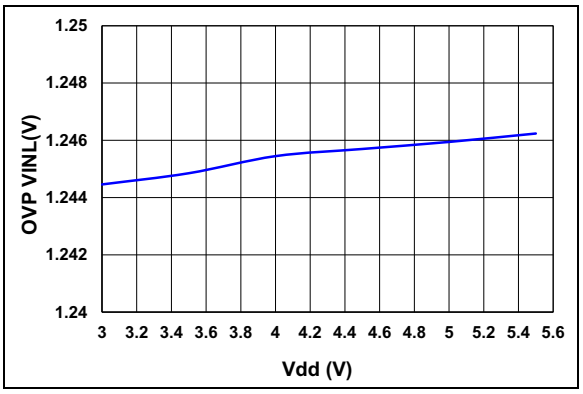


FIGURE 2-12: *OVP VINL Threshold vs. Input Voltage.*

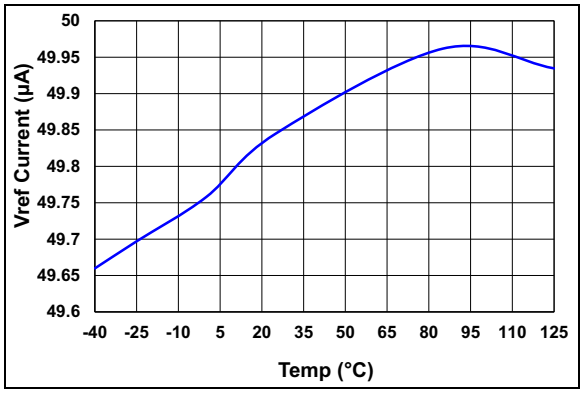


FIGURE 2-13: *Vref Current vs. Temperature.*

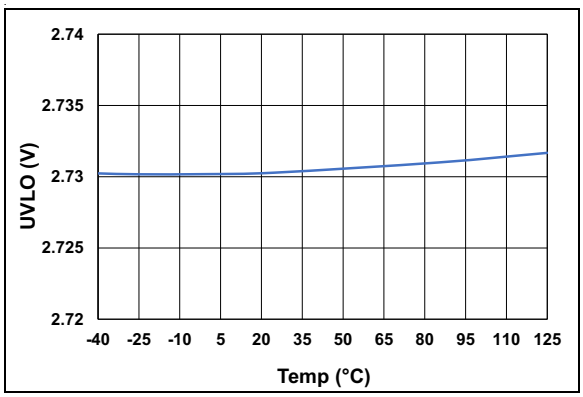


FIGURE 2-16: *UVLO VINLO Threshold vs. Temperature.*

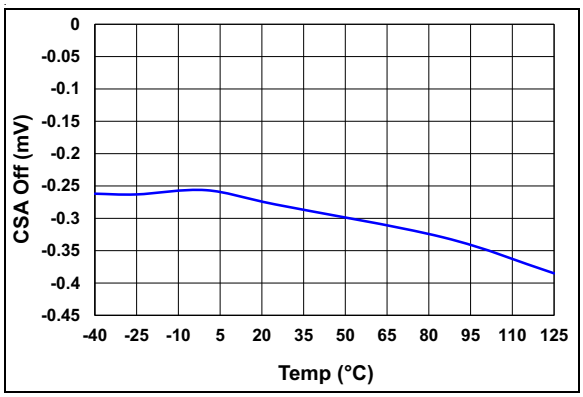


FIGURE 2-14: *Current Sense Amplifier Offset Voltage vs.Temperature.*

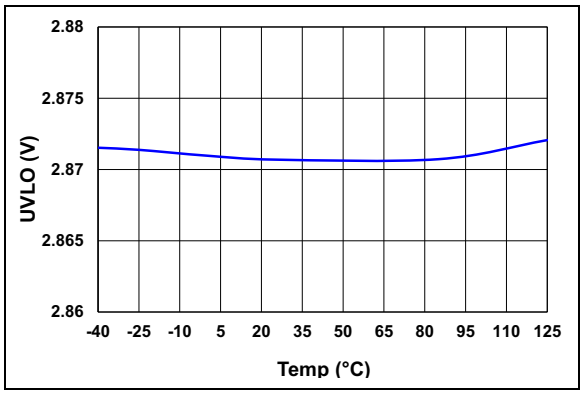


FIGURE 2-17: *UVLO VINHI Threshold vs. Temperature.*

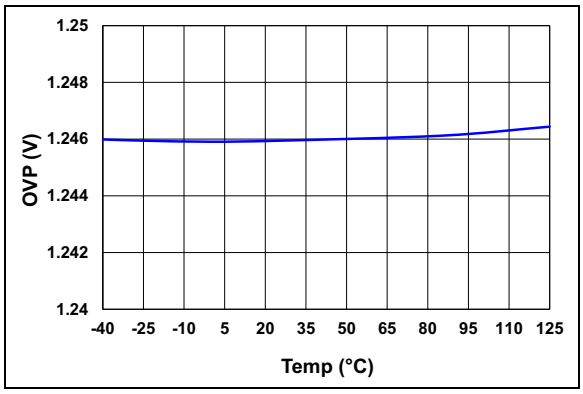


FIGURE 2-15: *OVP vs. Temperature.*

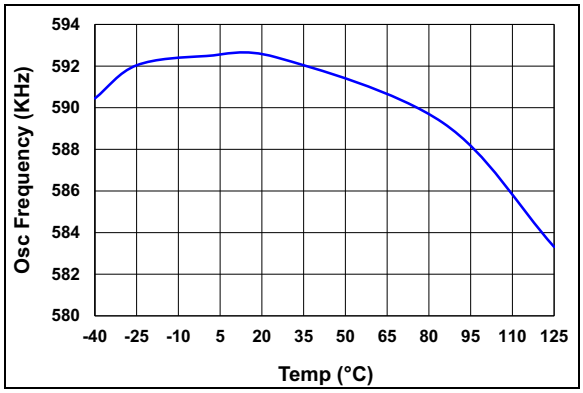


FIGURE 2-18: *Oscillating Frequency vs. Temperature at 600 kHz.*

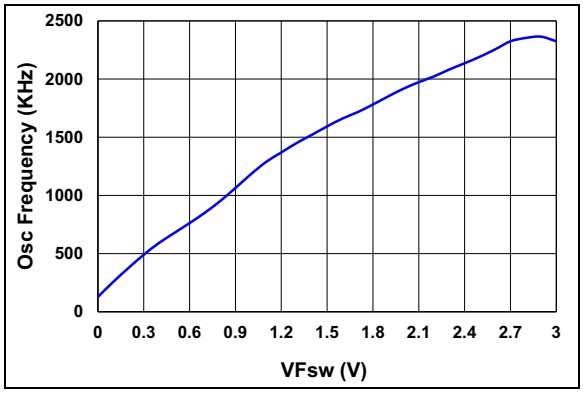


FIGURE 2-19: *Oscillator Frequency vs. F_{sw} Pin Voltage (V_{DD}=5V, Temperature=25°C).*

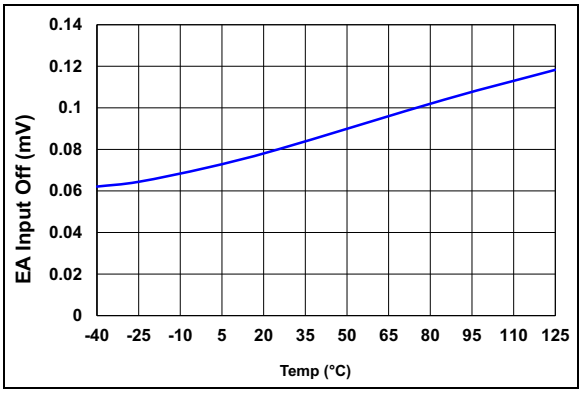


FIGURE 2-22: *Error Amplifier Input Offset vs. Temperature).*

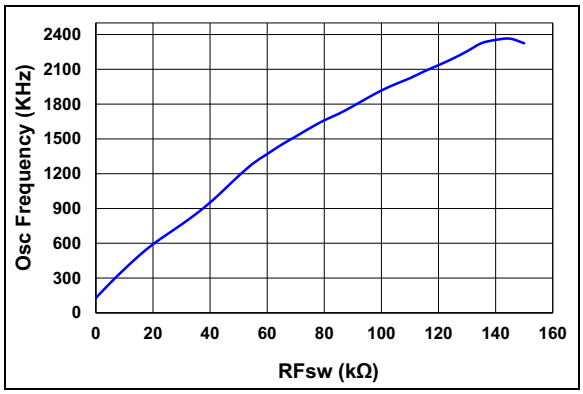


FIGURE 2-20: *Oscillator Frequency vs. RF_{sw} (V_{DD}=5V, Temperature=25°C).*

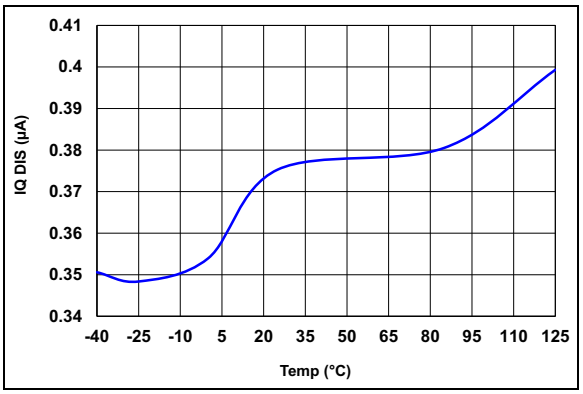


FIGURE 2-23: *Input Quiescent Disable Current vs.Temperature.*

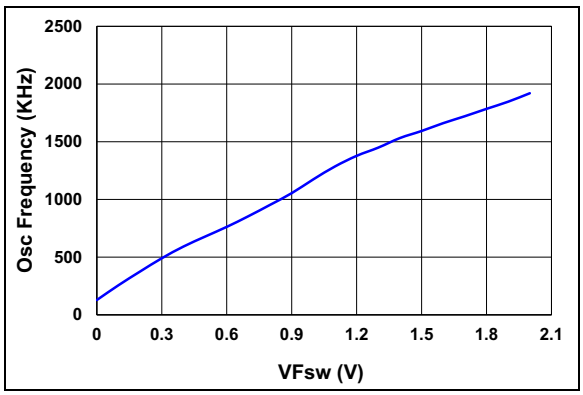


FIGURE 2-21: *Oscillator Frequency vs. F_{sw} Pin Voltage (V_{DD}=3V, Temperature=25°C).*

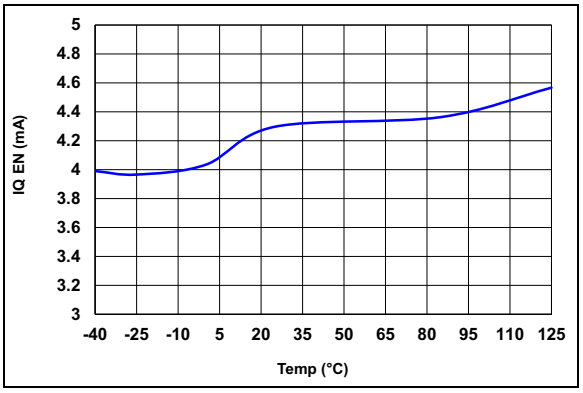


FIGURE 2-24: *Input Quiescent Enable Current vs.Temperature.*

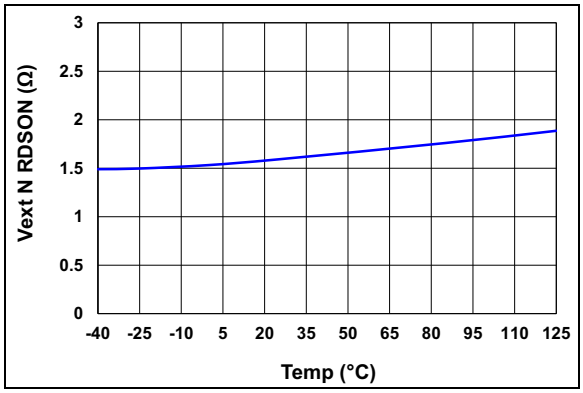


FIGURE 2-25: *Vext N-Channel RDSON vs. Temperature.*

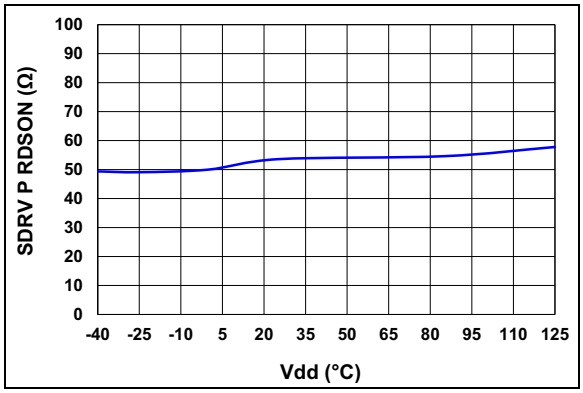


FIGURE 2-28: *SRDV P-Channel RDSON vs. Temperature.*

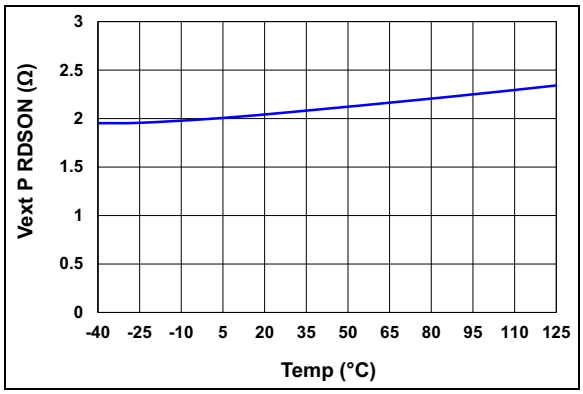


FIGURE 2-26: *Vext P-Channel RDSON vs. Temperature.*

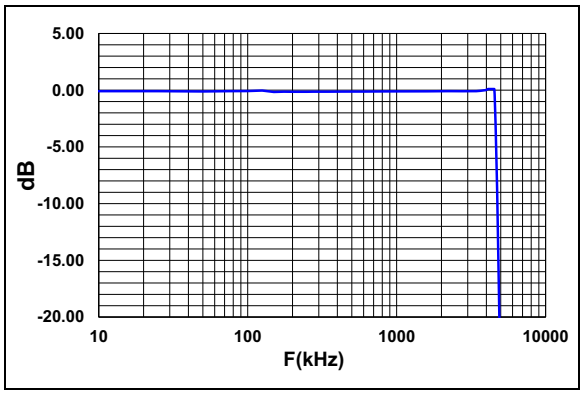


FIGURE 2-29: *Current Sense Amplifier BW at V_{DD} = 5V.*

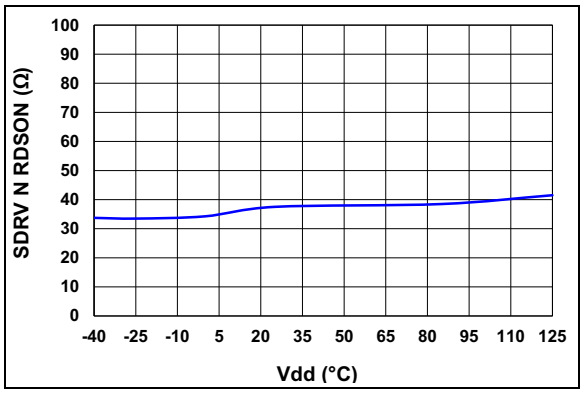


FIGURE 2-27: *SRDV N-Channel RDSON vs. Temperature.*

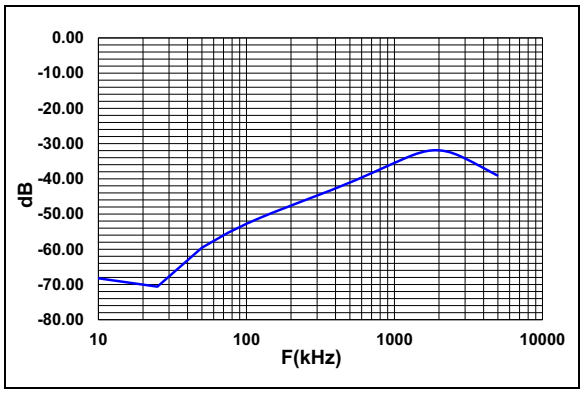


FIGURE 2-30: *Current Sense Amplifier CMRR at V_{DD} = 5V.*

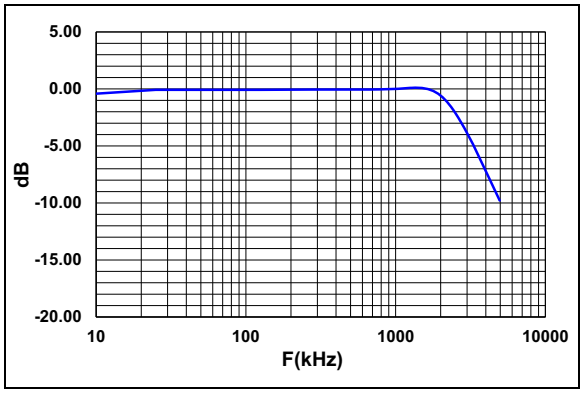


FIGURE 2-31: *Error Amplifier BW at V_{DD}=5V.*

3.0 PIN DESCRIPTION

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP1633 QFN16	Symbol	Description
1	F_{SW}	Switching Frequency Set
2	$\overline{FAULT}$	Open-Drain Fault Indicator
3	SS/V_{REF}	Soft Start/Reference Voltage Set
4	COMP	Error Amplifier Output
5	FB	Inverting Error Amplifier Input
6	I_{OUT}	Current Sense Operational Amplifier Output
7	ISP	Current Sense Operational Amplifier Positive Input
8	ISN	Current Sense Operational Amplifier Negative Input
9	CSO	Current Sense Offset
10	CS	Current Sense Input
11	V_{EXT}	PWM Output signal
12	V_{CC}	Input Bias
13	SDRV	Series Dimming MOSFET Gate Driver Output
14	DIMM	PWM Dimming Input
15	OVP	Overvoltage Protection Input
16	EN/Sync	Enable or external synchronization input
17	EP	Exposed Thermal Pad, Analog Ground and Power Ground

3.1 Switching Frequency Set (F_{SW})

The switching frequency is set by an external resistor connected between the F_{SW} pin and Ground. The frequency can be adjusted between 200 kHz and 2.2 MHz.

3.2 Open-Drain Fault Indicator (FAULT)

The open drain output provides an indication about chip status. This output is active low and is triggered by the input undervoltage, output overvoltage and over-temperature.

3.3 Soft Start/Reference Voltage Set (SS/Ref)

This pin is the output of the internal Constant Current Generator (50 µA typical). An external resistor must be connected between this pin and GND. The current flowing in this resistor will set the reference voltage. Optionally, a capacitor may also be connected between this pin and GND to set the soft start ramp behavior. This pin may be overdriven by an external voltage source, enabling the reference voltage to be controlled externally.

3.4 Error Amplifier Output (COMP)

COMP is the internal error amplifier output pin. External compensation is connected from COMP to GND for control-loop stabilization.

3.5 Inverting Error Amplifier Input (FB)

FB is the internal error amplifier inverting input pin. The output (voltage or current) is sensed and fed back to the FB pin for regulation. Inverting or negative feedback is used.

3.6 Current Sense Operational Amplifier Output (I_{OUT})

This pin is connected to the current sense operational amplifier output. It can be connected directly to the FB pin to close the current loop or to a microcontroller to measure the output current.

3.7 Current Sense Operational Amplifier Positive Input (ISP)

This pin is directly connected to the noninverting input of the current sense operational amplifier.

3.8 Current Sense Operational Amplifier Negative Input (ISN)

This pin is directly connected to the inverting input of the current sense operational amplifier.

3.9 Current Sense Offset (CSO)

This pin helps users to better set a peak current limit to protect the application. Internally this pin is connected to current source (20 µA typical). By connecting a resistor between this pin and ground, the resistor generates a DC level that is added over current sense signal.

3.10 Current Sense Input (CS)

This is the input for the switch current used for Peak Current Mode control. A blanking period of 30 ns (typical) for CS signal is provided to avoid leading edge spikes that can cause false PWM reset. The normal PWM duty cycle will be terminated when the voltage on the CS pin including the slope compensation ramp and DC offset (CSO) is equal to the output of the error amplifier. For Current Mode operation, the CS pin will control the PWM output on a cycle-by-cycle basis. To avoid the instability of the Peak Current Mode control when the duty cycle is higher than 50%, a slope compensation ramp generator is internally provided. This circuit will add to the CS signal an artificially generated ramp to avoid sub-harmonic oscillations. The amplitude of the slope compensation ramp is adjustable with one external resistor. If this pin is left open, the PWM Controller will operate in Voltage Mode Control. In this mode, the external switching MOSFET transistor is not protected against overcurrent conditions. Certain limitations related to the stability of the closed-loop system must be taken into account by the designer when the part operates in Voltage Mode Control.

3.11 PWM Output Signal (V_{EXT})

V_{EXT} is the internal MOSFET driver output pin, used to drive the external transistor.

Connect to gate of external main switching N-channel MOSFET.

3.12 Input Bias (V_{CC})

V_{CC} is the input voltage pin. Connect the input voltage source to the V_{CC} pin. For normal operation, the voltage on the V_{CC} pin should range from +3.0V to +5.5V. A bypass capacitor of at least 1 µF should be connected between the V_{CC} pin and the GND pin. This decoupling capacitor must be located as close as possible to the controller package.

3.13 Series Dimming MOSFET Gate Driver Output (SDRV)

Series dimming N-channel MOSFET gate driver output. Connect to gate of external N-channel MOSFET to implement series FET PWM dimming and fault disconnect.

3.14 PWM Dimming Input (DIMM)

External PWM dimming input. A direct PWM dimming command can be applied to control the LED current duty cycle and frequency. This PWM generates a signal that controls the V_{EXT} and SDRV outputs. Setting this pin to logic level low, turns off switching, disconnects the COMP pin, and sets SDRV to "0". Connect to V_{CC} via 100 kΩ resistor when not used for PWM dimming.

3.15 Overvoltage Protection Input (OVP)

Output voltage input. Connect a resistor divider from output voltage to GND to set output overvoltage protection. The OVP circuits turns off the MOSFET driver (V_{EXT} pin set to "0") and the series dimming MOSFET driver (SDRV pin set to "0") when the output voltage reaches the OVP threshold.

3.16 Enable or External Synchronization Input (EN/Sync)

When this pin is connected to GND (logic "0") for more than 100 µS (typical) the controller will go to DISABLE state. A logic "1" enables the normal operation of the MCP1633. When the device is disabled, the V_{EXT} output is set. This pin can also accept an external signal for synchronization from an external clock source. The user must provide a correct timing signal for synchronization to ensure consistent operation of PWM controller.

3.17 Exposed Thermal Pad (AGND)

Analog ground and power ground are both connected here. This PAD must be connected to PCB ground plane using multiple vias for good functionality.

4.0 DETAILED DESCRIPTION

4.1 Device Overview

The MCP1633 device integrates all the functions needed for designing a compact LED driver based on low side topologies. The device uses peak current mode control technique to achieve constant output current and fast transient response. The output current level is set by the analog adjust, SS/REF by using a simple resistor or external voltage to achieve analog dimming. PWM dimming is also supported by specialized internal block using an external PWM signal with 0 to 100%. The integrated low offset, current sense amplifier provides the flexibility due to differential type and external gain set. The output of the current sense amplifier can be used to close the loop and measure the output current. The application's safety is achieved by internal protections UVLO, OVLO and thermal shutdown turning off the converter and disconnecting the load and reporting the status via $\overline{\text{FAULT}}$ pin which is open drain indicator.

4.2 PWM Circuitry

MCP1633 implements a typical Peak Current Mode control loop. The V_{EXT} output of the MCP1633 device is determined by the output level of the internal high-speed comparator and the level of the internal CLK signal. When the CLK signal level is high, the PWM output (V_{EXT}) is forced low, limiting the maximum duty cycle to approximately 90% (typical). When the CLK signal is low, the PWM output is determined by the output level of the internal high-speed comparator. During UVLO and OVLO, the V_{EXT} pin is held in low state. During overtemperature operation, the V_{EXT} pin is high-impedance (10 kΩ to ground, typical).

4.3 Normal Cycle-by-Cycle Control

The beginning of a PWM cycle is defined by the internal CLK signal (a transition from high to low). Refer to Figure 4-1 for the detailed timing operation of the MCP1633 PWM controller. For normal operation, the state of the high-speed comparator output (R) is low and the Q output of the latch is low. On the high-to-low transition of the CLK signal, the SR inputs to the high-speed latch are both low and the Q output will remain unchanged (low). The output of the OR gate (V_{DRIVE}) will transition from high to low, turning on the P-Channel drive transistor in the output stage of the PWM. This will change the PWM output (V_{EXT}) from low to high, turning on the power train MOSFET and ramping current in the power train magnetic device. The sensed current in the magnetic device is fed into the CS input, shown as a ramp, and increases linearly until it reaches the same level as the divided down output of the error amplifier at the noninverting input of the high-speed comparator. The comparator output (R) changes state (low to high) and resets the PWM latch. The Q output transition from low to high turns off the V_{EXT} drive to the external MOSFET driver, thus terminating the current conduction cycle. The CLK signal will transition from low to high while the V_{EXT} pin remains unchanged. If the CS input pin never reaches the same level as the error amplifier output, the low-to-high transition on the CLK signal terminates the current switching cycle. This would be considered as the maximum duty cycle. In either case, while the CLK signal is high, the V_{EXT} drive pin is low, turning off the external power train switch. The next switching cycle will start on another transition of the CLK signal from high to low.

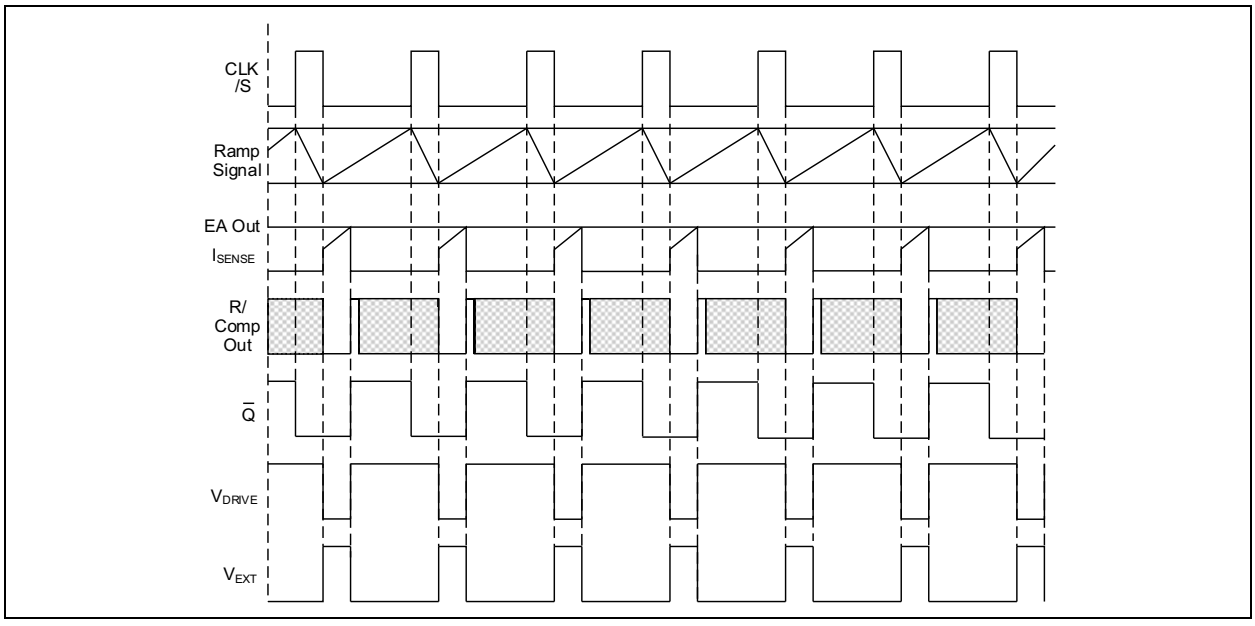


FIGURE 4-1: *PWM Timing Diagram.*

4.4 Error Amplifier/Comparator Current Limit Function

The error amplifier is of transconductance type (OTA) with external compensation network connected between the output (COMP) and the ground. The error amplifier generates an error signal proportional to the difference between the LED current sense feedback voltage and V_{REF} input voltage. The error amplifier output is clamped by a precision 2.7V internal voltage source. The output of the error amplifier is connected to the inverting input of the high-speed comparator. As the output load current demand increases, the error amplifier output increases too, causing the inverting input pin of the high-speed comparator to increase. Eventually, the output of the error amplifier will hit the clamp, limiting the input of the high-speed comparator to 2.7V maximum. Even if the FB input continues to decrease, calling for more current, the inverting input is limited to 2.7V. By limiting the inverting input to 2.7V, the current sense (IP) input is limited to 2.7V minus DC offset value (CSO), thus limiting the current that flows in the main switch. Limiting the maximum peak current in the switch prevents the destruction of the semiconductor device and the saturation of the inductor during overloads. To simplify the design when CS signal is too small so peak limit is far away, there is another feature called I peak offset (CSO). This DC value is added over current sense information to avoid output overloads. Refer to Figure 4-2 and Figure 4-3 for a detailed description. The error amplifier input includes only the GND potential.

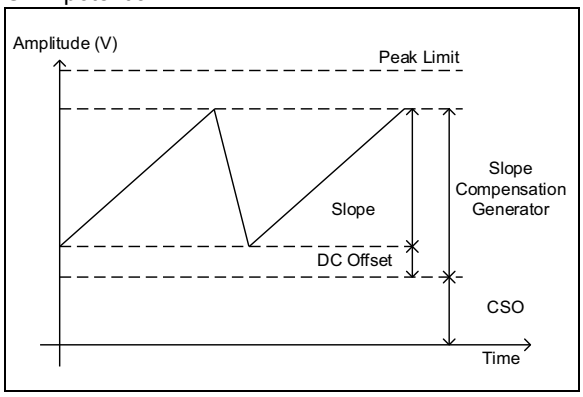


FIGURE 4-2: *Slope Compensation Signal.*

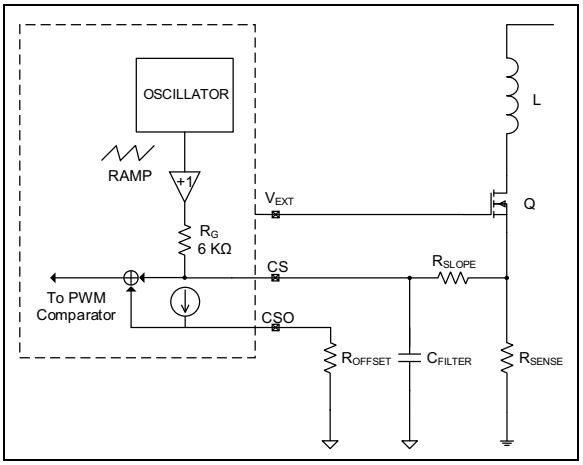


FIGURE 4-3: *Slope Compensation Circuit.*

4.5 Reference Voltage Generator

The internal precision constant current generator and an external resistor connected between the V_{REF} pin and GND form the reference voltage generator. Refer to Figure 4-4 for details. Optionally, a capacitor (CSS) can be connected in parallel with RV_{REF} to activate the soft start function that will minimize overshoots of the output voltage during start-up. The equations in Figure 4-4 calculate the value of the resistor (RV_{REF}) for a given reference voltage and the value of the soft start capacitor (CSS) based on the necessary time to reach 90% of the final value for V_{REF}. An internal circuit of the MCP1633 device will discharge the capacitor during the shutdown period. This capacitor must be of good quality, with low leakage currents, in order to avoid any errors that can affect the reference voltage. The reference voltage should not exceed 80% of the bias input voltage (V_{IN} pin) in order to avoid any errors that affect the internal constant current generator. An external low-noise, low-impedance source can be used to overdrive the V_{REF} pin in order to control the reference voltage. In this case, the resistor/capacitor group connected to GND is not necessary, and the soft start profile must be controlled by the external reference voltage generator.

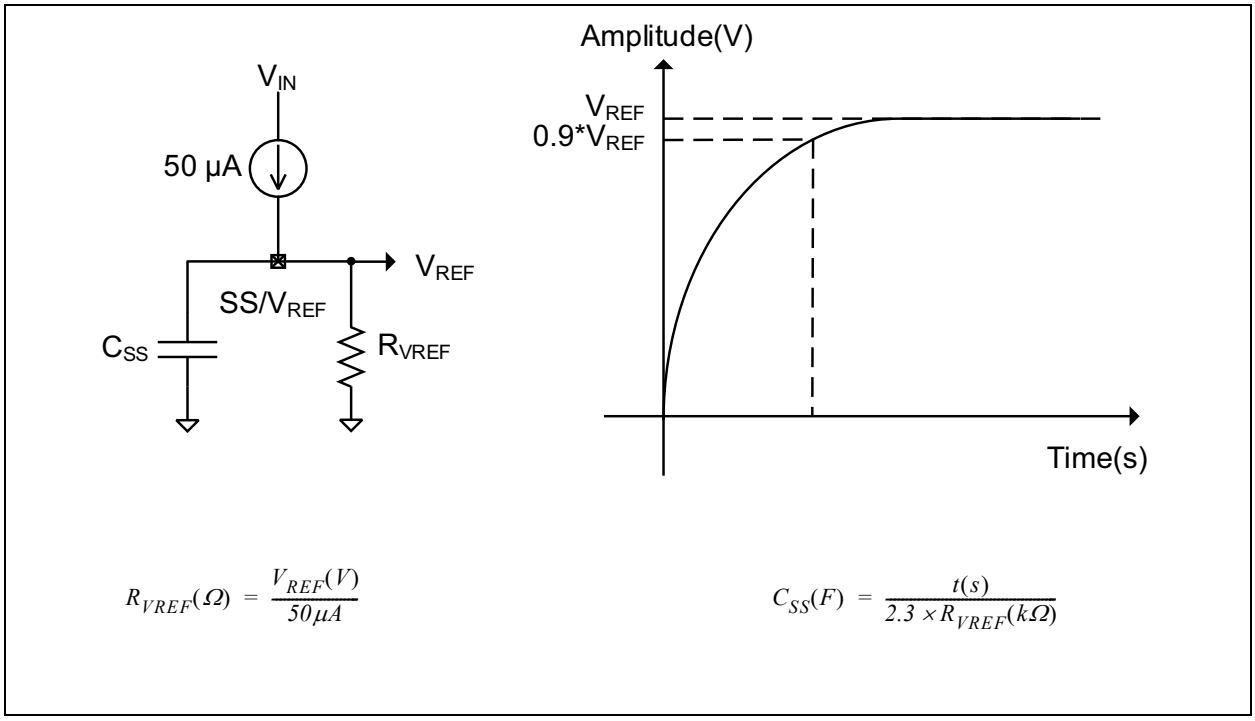


FIGURE 4-4: *Reference Voltage Generator.*

4.6 Internal Oscillator

The MCP1633 PWM controller provides programmable switching frequency with an external resistor connected between the F_{SW} pin and GND. To set a desired frequency, the resistor value can be calculated with the Equation 1 below or using the graph in Figure 2-20. A small capacitor in parallel with RF_{SW} is recommended.

EQUATION 1: RESISTOR VALUE.

$$RF_{SW} = 2E-05 \times F_{SW^2} + 0.0234 \times F_{sw} - 0.026$$

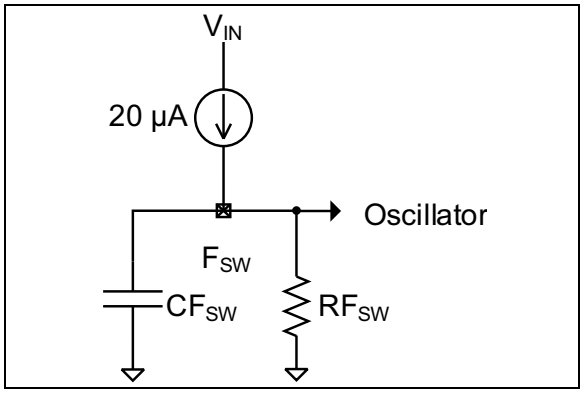


FIGURE 4-5: *Switching Frequency Set.*

The internal oscillator can be synchronized by an external clock pulse to EN/Sync pin. It is recommended that the frequency of the external synchronization pulse is within ±20% of the internal oscillator frequency programmed by the F_{SW} resistor. If the external synchronization clock is lost, then the internal oscillator takes control of the switching rate based on the F_{SW} resistor to maintain similar operating conditions. F_{SW} pin cannot be left floating.

4.7 Current Sense Amplifier

The internal current sense amplifier measures LED current based on the differential voltage drop between the ISP and ISN inputs over a common mode range of 0V to 5V. Inputs and output of the current sense amplifier are directly connected to pins (ISP, ISN, I_{OUT}) to set the gain of the amplifier by external resistors providing high flexibility in designing applications. The output of current sense amplifier should be connected to FB pin to close the loop and regulate the output current. An optional low-pass filter can be used to filter the effects of output current ripple and switching spikes. Figure 4-6 shows an example of a filter.

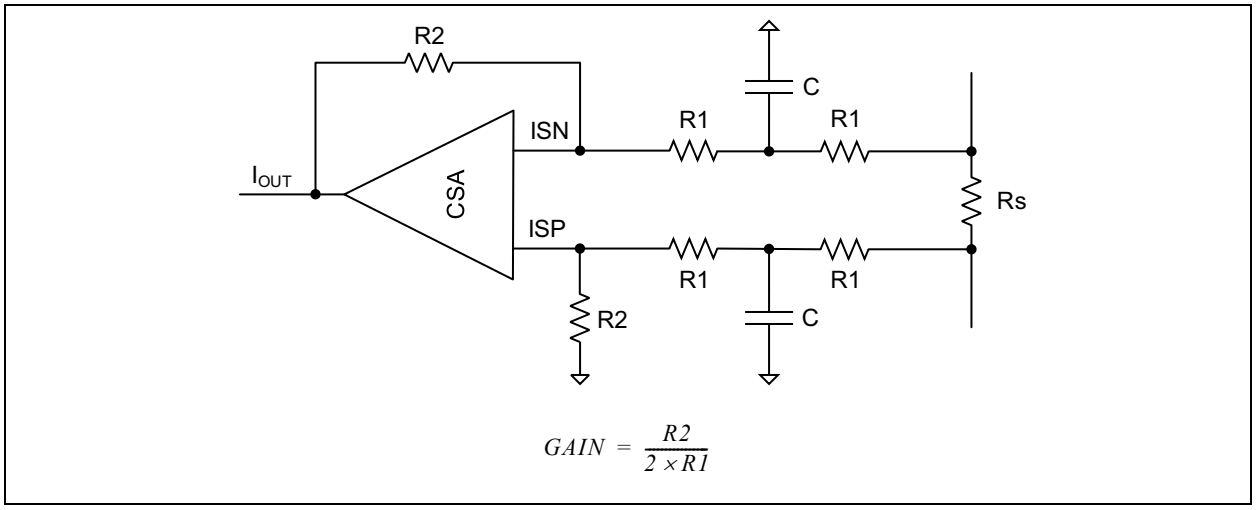


FIGURE 4-6: *Current Sense Amplifier Gain Set.*

4.8 PWM Dimming

MCP1633 incorporates a high-performance dimming mechanism. External PWM signal is used to modulate the output current. Internally this signal in low state disable the main driver (V_{EXT}), disconnects the output of error amplifier and disconnects the load (SDRV set low) to maintain the steady state condition at the next transition. When DIMM pin is high state the driver is enabled, output of error amplifier is reconnected and SDRV pin is set high. When dimming is not required, connect the DIMM pin to the V_{CC} pin. An internal pull-down resistor sets the input to logic-low and disables the device when the pin is floating. The SDRV pin is the output of a secondary driver which controls a NMOS transistor for dimming and is capable of sinking and sourcing up to 50 mA of peak current. To ensure that the applied dimming-pulse duration matches the effective dimming-pulse duration, it is recommended to synchronize the dimming pulses with the switching clock of the controller.

4.9 Undervoltage Lockout (UVLO)

When the input voltage (V_{IN}) is less than the UVLO threshold, the V_{EXT} is held in low state. This will ensure that, if the voltage is not adequate to power the MCP1633 device, the main power supply switch will be held in off state. In order to prevent oscillations when the input voltage is near the UVLO threshold, the UVLO circuit offers 100 mV (typical) hysteresis. Typically, the MCP1633 device will not start until the input voltage at V_{IN} is between 2.8V and 2.9V (typical).

4.10 Overtemperature Protection

To protect the V_{EXT} output if shorted to V_{IN} or GND, the V_{EXT} output of the MCP1632 device will be high-impedance if the junction temperature is above the thermal shutdown threshold. An internal 10 kΩ pull-down resistor is connected from V_{EXT} to ground to provide some pull-down during overtemperature conditions. The protection is set to +150°C (typical), with a hysteresis of +20°C.

4.11 Overvoltage Protection

The OVP pin is a comparator used to prevent the power system from being damaged when the load is disconnected. By comparing the divided down power train output voltage with a 1.23V internal reference voltage, the MCP1633 V_{EXT} output switching is interrupted and load disconnected when the output voltage is above a pre-set value. This limits the output voltage of the power train and the low comparator's hysteresis will operate as a ripple regulator.

5.0 APPLICATION CIRCUITS

5.1 Typical Applications

The MCP1633 PWM controller can be used for applications that require low-side MOSFET control, such as Boost, Buck-Boost, Flyback, SEPIC or CUK converters. By using an external high-side MOSFET driver (e.g. MCP14628), the MCP1633 device is able to control the buck converter. The MCP1633 PWM controller can be easily interfaced with a microcontroller in order to develop intelligent solutions for LED driving.

Figure 5-1 depicts the typical boost converter controlled by MCP1633. If the converter must operate with input voltages higher than 5.5V, a linear voltage regulator can be used to bias the MCP1633 controller. The Peak Current Mode control used in this case will ensure consistent performance over a wide range of operating conditions. The MOSFET is protected against overcurrent by internally limiting the maximum voltage at the output of the error amplifier of the controller. If the voltage applied on the CS pin exceeds the set threshold, the MCP1633 device will reduce the duty cycle in order to prevent overcurrent in MOSFET.

Note: The boost converter is not protected against the output short circuit.

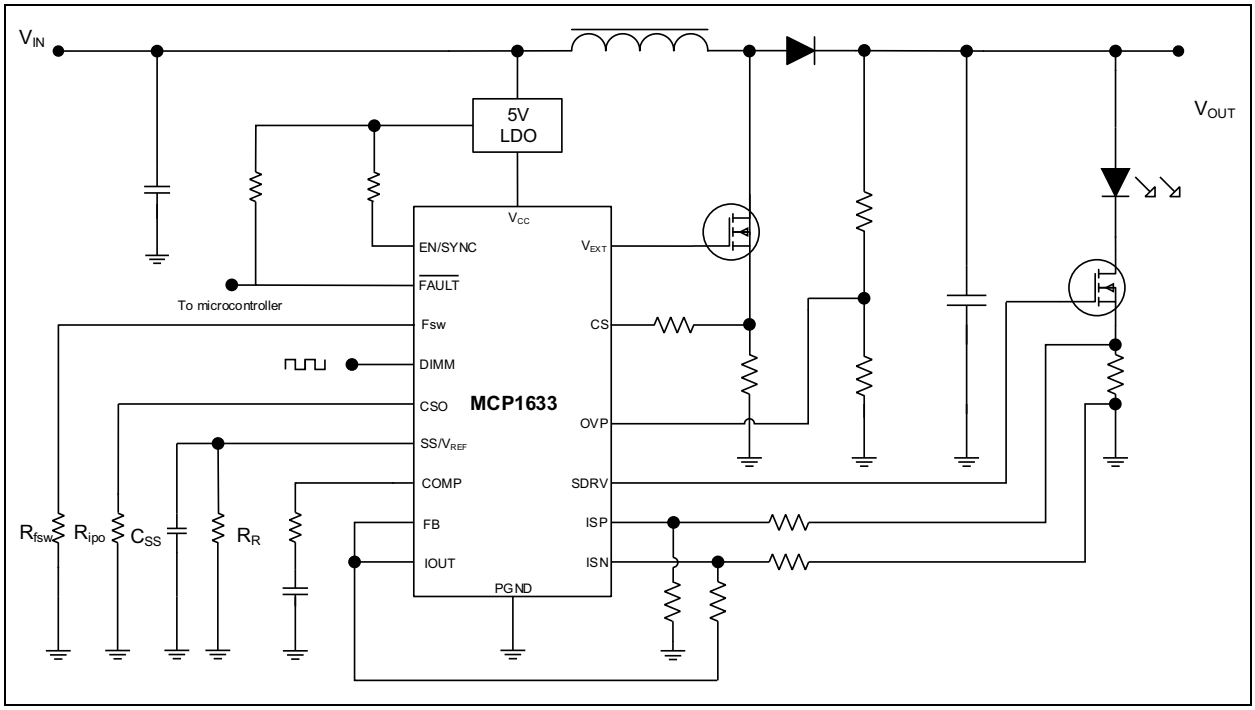


FIGURE 5-1: *MCP1633 Boost Converter.*

The single-ended primary inductor converter (SEPIC) used to drive an LED string is presented in Figure 5-2. This converter offers buck-boost functionality and is protected against the output short circuit. The inductors can share the same magnetic core (coupled inductors); in this case, the mutual inductance doubles the value of the inductor, reducing the ripple of the current.

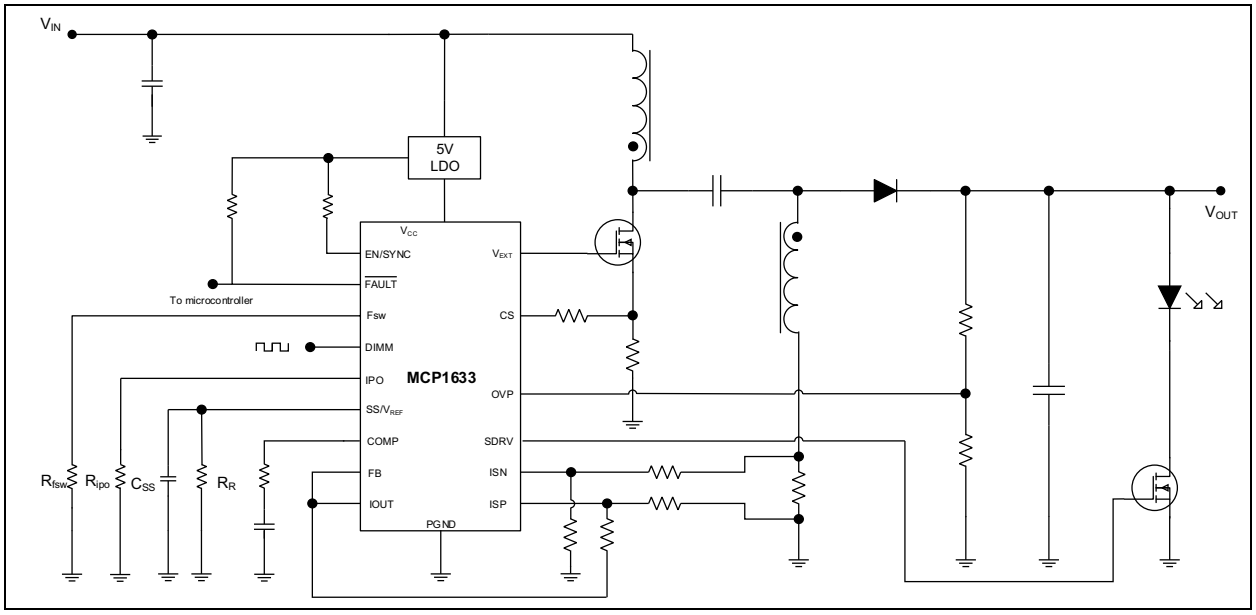


FIGURE 5-2: *MCP1633 SEPIC Converter.*

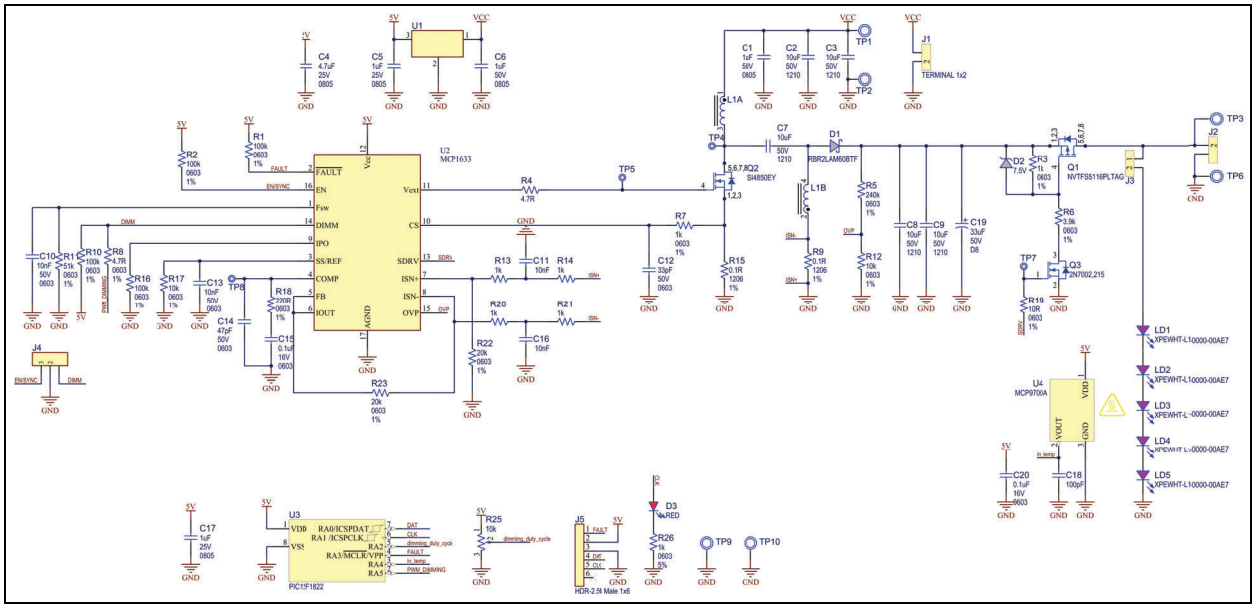


FIGURE 5-3: *Typical SEPIC Converter.*

5.2 Recommended Startup Sequence

In order to reduce the startup stress, it is recommended to use the sequence below (Figure 5-4). Depending of the capacitor placed on the F_{SW} pin, the necessary delay for DIMM signal can be calculated with Equation 2.

EQUATION 2: NECESSARY TIME TO REACH 90% OF THE FINAL VALUE FOR V_{FSW}

$$t(s) = c(nf) \times r(k\Omega) \times 2.3 \times 10^{-6}$$

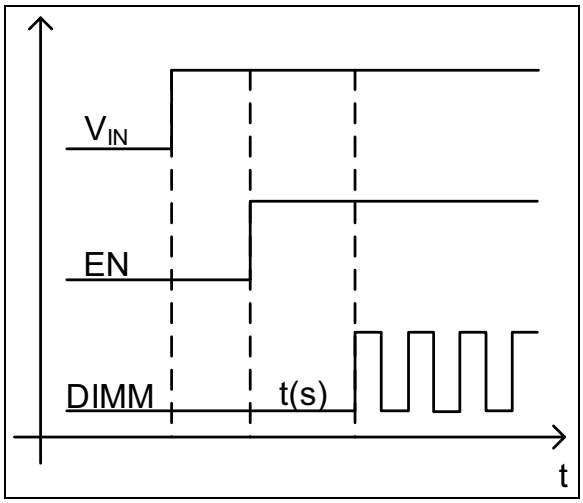


FIGURE 5-4: *Start-Up Sequence.*

5.3 Layout Recommendations

Good printed circuit board layout techniques are important to any switching circuitry and switching power supplies are no different. Here are the guidelines for the PCB layout:

- The exposed pad of MCP1633 QFN case is the only connection to the internal device ground. Connect this pad directly to the board ground plane.
- Place at least four vias in the exposed pad land to ensure good ground connection and remove heat from the device.
- Use separate grounds for power and signal paths. Keep high current paths away from sensitive components and nodes (e.g. feedback and compensation network components).
- Route the ISP and ISN together with Kelvin connections to the current sense resistor with traces as short as possible and use noise filters.
- Use short and strong connection between V_{EXT} and gate pin of the MOSFET.
- Locate the V_{REF}, CSO, F_{SW}, Comp, CSA gain components near the MCP1633 case.
- Use separate connections to close each loop directly to ground plane (V_{REF}, CSO, F_{SW}, Comp)
- Four-layer PCBs are highly recommended to obtain optimum results regarding noise/EMI. Use an internal layer as ground plane.
- Minimize the area of the high-current loops. Use copper planes or large traces for high-current connections in order to minimize the parasitic inductances.

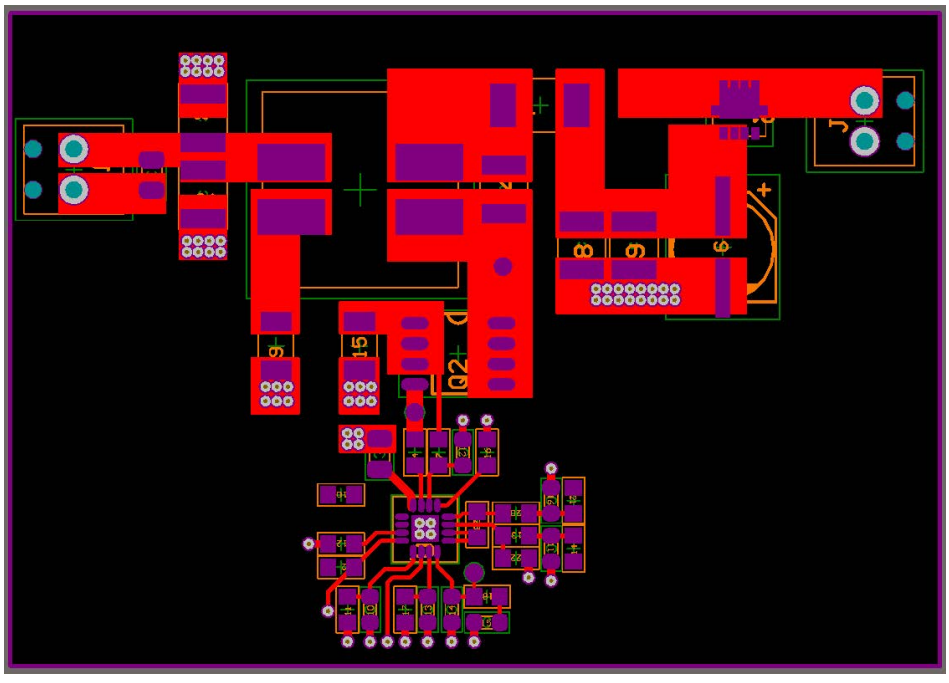
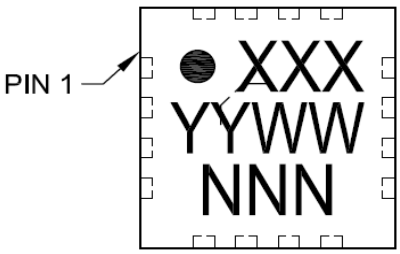


FIGURE 5-5: *Layout Example.*

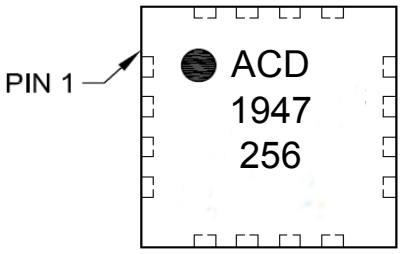
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

16-Lead QFN



Example

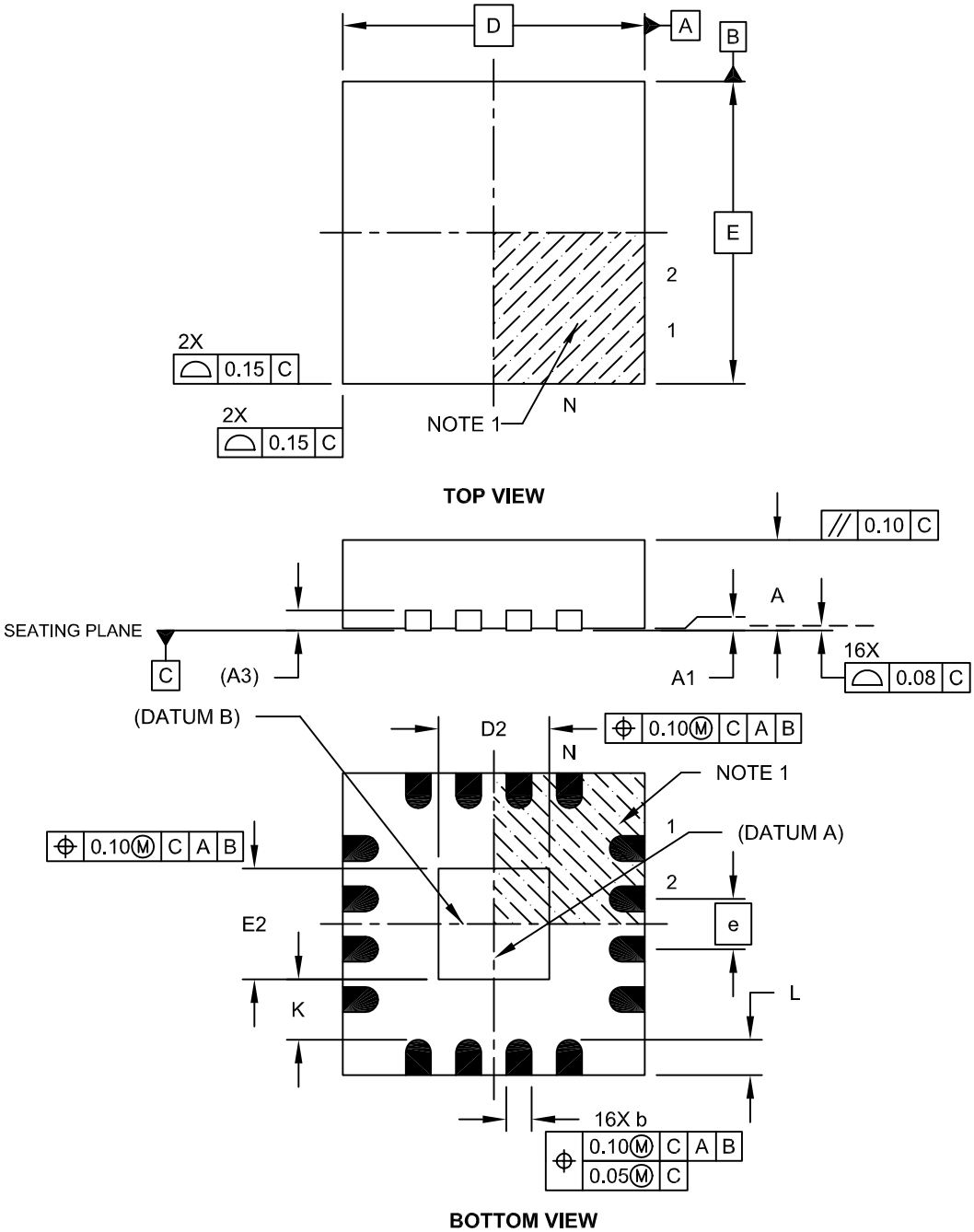


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

16-Lead Plastic Quad Flat, No Lead Package (MG) - 3x3x0.9 mm Body [QFN]

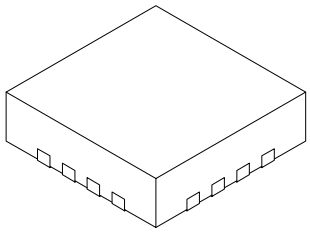
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-142A Sheet 1 of 2

16-Lead Plastic Quad Flat, No Lead Package (MG) - 3x3x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		16	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.00	1.10	1.50
Overall Length	D		3.00 BSC	
Exposed Pad Length	D2	1.00	1.10	1.50
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.25	0.35	0.45
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

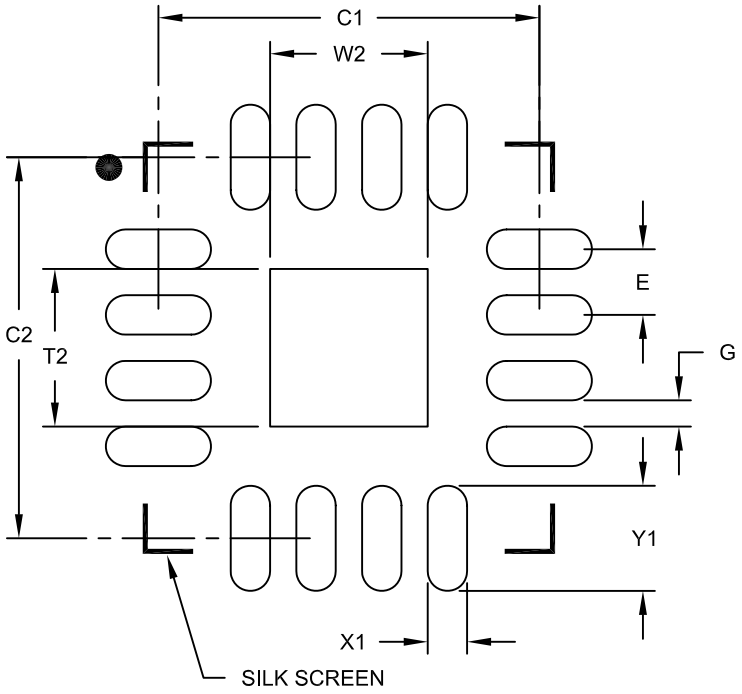
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-142A Sheet 2 of 2

16-Lead Plastic Quad Flat, No Lead Package (MG) – 3x3x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2			1.20
Optional Center Pad Length	T2			1.20
Contact Pad Spacing	C1		2.90	
Contact Pad Spacing	C2		2.90	
Contact Pad Width (X16)	X1			0.30
Contact Pad Length (X16)	Y1			0.80
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2142A

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (January 2020)

- Initial release of this document.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	X	/XX
Device	Tape and Reel Option	Temperature Range	Package

Device:	MCP1633: High-Speed PWM Controller	
Tape and Reel Option:	Blank T	= Standard Packaging (Tube or Tray) = Tape and Reel(1)
Temperature Range:	E	= -40°C to+125°C (Extended)
Package:	MG	= 16-Lead Plastic Quad Flat, No Lead Package - 3 x 3 0.9 mm Body (QFN)

Examples:

a) MCP1633-E/MG: High-Speed PWM Controller, Extended temperature, 16-Lead QFN package

b) MCP1633T-E/MG: High-Speed PWM Controller, Tape and Reel,, Extended temperature, 16-Lead QFN package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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