

General Description

The MAX14866 is a 16-channel, high-voltage (HV), analog SPST switch primarily intended for HV multiplexing in ultrasound applications.

The MAX14866 operates from one only low-voltage supply (+5V) and does not require dedicated HV supplies, resulting in cost-saving and system simplification. Moreover, for in-probe applications, HV supplies do not need to be associated with the MAX14866 in the probe/transducer head, resulting in greater safety and easier compliance with safety regulations.

The MAX14866 features best-in-class performance in terms of bandwidth (up to 50MHz), charge injection (<100pC), and linear transmit input range (up to 210V_{PKPK}). The low-signal switch $R_{DS(ON)}$ is typically about 7 Ω around 0V and remains flat in the entire input range ensuring extremely good linearity.

The latchup-free SOI (Silicon-on-Insulator) technology and the wide analog range results in extremely high robustness during undershoots and overshoots that occur in ultrasound systems due to the resonant nature of the load.

The status of the switches can be individually controlled through a high-speed SPI interface (up to 30MHz). Daisy-chain architecture is supported.

Alternatively, switches can also be controlled with global control signal (SET and CLR) for bank selections or relay replacement applications.

The MAX14866 is offered in two different packages: wafer-level packages (WLPs) and TQFNs. The 110-bump WLP size is only 5.53 x 5.47mm, resulting in less than 1.9mm²/channel footprint and allowing for very high levels of integration, which is especially beneficial for in-probe applications.

The size of the TQFN package is an industry standard 48-pin, 7mm x 7mm package.

Applications

- Medical Ultrasound Imaging
- Relays replacements
- NDT
- Printers

Benefits and Features

- Flexibility and Ease-of-Design
 - HV Switches Operate From +5V Supply Only—Eliminating Dedicated High-Voltage Supplies Eases Probe Compliance To Industry Safety Standards
 - SOI Technology—Latchup Free
 - Large Analog Input range (up to 210V_{PKPK})
 - 16 Independent SPST Ensure Flexibility Supporting All Possible MUX Combinations
 - Switches Can Be Controlled Either Individually or Globally (Bank Selection)
 - 30MHz SPI Interface for Individually Programming the Status of the Switches
 - SET and CLR CMOS for global control of the switches (Bank Selection or Relay Replacements Applications)
 - Extended Digital Logic Input Range From 1.8V to 5V
- High Level Of Integration and Density for Space-Saving Applications
 - 16 Channels Linear SPST switches
 - < 1.9mm²/channel footprint (WLP)
- High Performance:
 - Low R_{ON} (7 Ω typ) Ensures Low Insertion Loss
 - R_{ON} Flatness in the Entire Input Range Ensures Excellent Performances In Harmonic Imaging
 - Low Charge Injection <100pC.
 - Wide Bandwidth of Operation (Up to 50MHz)
 - Low On Input Capacitance (33pF)
Low Off Input Capacitance (7.7pF)
 - Excellent Off Isolation (-75dB at 5MHz)
Excellent Crosstalk Performances (-62dB at 5MHz)

Ordering Information appears at end of data sheet.

Absolute Maximum Ratings

| | | | |
|--|---------------------------------|--|-----------------|
| V _{CC} to GND | -0.3V to 5.6V | TQFN Continuous Power Dissipation (Single Layer Board, T _A = +70°C, derate 27.8mW/°C above +70°C.)..... | 0mW to 2222mW |
| V _{DD} to GND | -0.3V to 5.6V | TQFN Continuous Power Dissipation (Multilayer Board, T _A = +70°C, derate 40 mW/°C above +70°C.)..... | 0mW to 3200mW |
| COM _x to GND, x = 0..15..... | -110V to +110V | WLP Continuous Power Dissipation (Multilayer Board, T _A = +70°C, derate 37mW/°C above +70°C.) | 0mW to 2960mW |
| NO _x to GND, x = 0..15..... | -110V to +110V | Operating Temperature Range | 0°C to 85°C |
| COM _x to NO _x , x = 0..15..... | -110V to +110V | Junction Temperature | +150°C |
| SDIN to GND | -0.3V to 5.6V | Storage Temperature Range | -65°C to +150°C |
| SDO _{UT} to GND | -0.3V to V _{DD} + 0.3V | Soldering Temperature (reflow) | |
| LE to GND | -0.3V to 5.6V | | |
| CLK to GND | -0.3V to 5.6V | | |
| CLR to GND | -0.3V to 5.6V | | |
| SET to GND | -0.3V to 5.6V | | |

Package Thermal Characteristics (Note 1)

| | | | | | |
|--------------|---|-----------|-------------|---|--------|
| 110-Bump WLP | Junction-to-Ambient Thermal Resistance (θ _{JA}) | 26.93°C/W | 48-Pin TQFN | Junction-to-Ambient Thermal Resistance (θ _{JA}) | 25°C/W |
| | Junction-to-Case Thermal Resistance (θ _{JC})..... | N/A | | Junction-to-Case Thermal Resistance (θ _{JC})..... | 1°C/W |

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{CC} = 5V ±5%, V_{DD} = 1.7V to 5.5V. Typical values are V_{DD} = +2.5V, V_{CC} = 5V, T_A = +25°C. Limits are 100% tested at T_A = +85°C and are guaranteed by design in the entire temperature range)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-------------------|---|------------------------|------------------------|------|-------|
| POWER SUPPLIES | | | | | | |
| V _{DD} Logic Supply Voltage | V _{DD} | | 1.7 | | 5.5 | V |
| V _{DD} Static Current | I _D DS | | | 1 | 5 | µA |
| V _{DD} Dynamic Current | I _{DD} | V _{DD} = +5V, f _{CLK} = 5MHz, f _{DIN} = 2.5MHz, C _{DO} UT = 15pF | | 300 | | µA |
| V _{CC} Supply Static Current | I _{CC} S | All switches remain on or off, COM __ = NO __ = GND | | 240 | 425 | µA |
| V _{CC} Supply Dynamic Current | I _{CC} | All Channel Switching, f = 50kHz | | 5.2 | 8.5 | mA |
| V _{CC} Supply Voltage Range | V _{CC} | | 4.75 | 5 | 5.25 | V |
| LOGIC LEVELS | | | | | | |
| Logic-Input Low Voltage | V _{IL} | | | 0.33 x V _{DD} | | V |
| Logic-Input High Voltage | V _{IH} | | 0.66 x V _{DD} | | | V |
| Logic-Output Low Voltage | V _{OL} | I _{SINK} = 1mA | | | 0.2 | V |
| Logic-Output High Voltage | V _{OH} | I _{SOURCE} = 1mA | V _{DD} -0.2 | | | V |
| Logic-Input Capacitance | C _{IN} | | | 5 | | pF |

Electrical Characteristics (continued)

($V_{CC} = 5V \pm 5\%$, $V_{DD} = 1.7V$ to $5.5V$. Typical values are $V_{DD} = +2.5V$, $V_{CC} = 5V$, $T_A = +25^\circ C$. Limits are 100% tested at $T_A = +85^\circ C$ and are guaranteed by design in the entire temperature range)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|--------------|--|------|---------|------|-----------|
| Logic-Input Leakage | I_{IN} | CLK, DIN pins | -1 | | +1 | μA |
| LEB Pullup Resistor | R_{PU} | | 70 | 100 | | $K\Omega$ |
| CLR, SET Pulldown Resistor | R_{PDW} | | 70 | 100 | | $K\Omega$ |
| SWITCH CHARACTERISTICS | | | | | | |
| Analog Dynamic Signal Range | $V_{SW_}$ | AC operation only, $f > 500kHz$ | -105 | | +105 | V |
| Small Signal On-Resistance | R_{ONS} | $V(NO) = 0V$, $I(COM) = 5mA$ | | 7 | 13 | Ω |
| Small Signal On-Resistance Matching | DRONS | 3 std, $VNO_ = 0V$, $ICOM_ = 5mA$ | | 3 | | % |
| Switch Symmetry | Symm | AC measured, 100Ω Resistive load NO and GND. Transmit bipolar low frequency pulse $\pm 80V$, $f = 0.5MHz$ Compare positive and negative output level on NO Symmetry = $[V_{OP} - V_{ON}] / [0.5 \times (V_{OP} + V_{ON})]$ | | ± 1 | | % |
| Analog Switch Peak Current | I_{PEAK} | $V(NO) = GND$, $V(COM)$ HV pulse 100ns duration | | 2.7 | | A |
| COM to GND Leakage Current Switch OFF | I_{COMOFF} | $V(COM) = \pm 100mV$ | -1 | | +1 | μA |
| COM to GND Equivalent Resistor. Switch ON | R_{COMON} | $V(COM) = 100mV$ | 60 | 82 | 104 | $K\Omega$ |
| NO to GND Equivalent Resistor. Switch OFF | R_{NOOFF} | $V(NO) = 100mV$ | 35 | 52 | 65 | $K\Omega$ |
| NO to GND Equivalent Resistor Switch ON | R_{NOON} | $V(NO) = 100mV$ | 60 | 82 | 104 | $K\Omega$ |
| Switch-Off DC Offset COM Pin | V_{OFF1} | Ref. Test Circuit $R = 100K\Omega$ | -5 | | +6 | mV |
| Switch-Off DC Offset NO Pin | V_{OFF2} | Ref. Test Circuit $R = 100K\Omega$ | -5 | | +6 | mV |
| Switch-On DC Offset | V_{OFF3} | Ref. Test Circuit $R = 100K\Omega$ | -5 | | +9 | mV |
| SWITCH DYNAMIC CHARACTERISTICS | | | | | | |
| Turn-On Time | t_{ON} | Ref. Test Circuit. $VCOM_ = +1V$, $R_L = 50\Omega$, from switch ON digital command to 90% of the transition completed | | | 4 | μs |
| Turn-Off Time | t_{OFF} | Ref. Test Circuit $VCOM_ = +1V$, $R_L = 50\Omega$ from switch OFF digital command to 90% of the transition completed | | | 4 | μs |
| Off-Isolation in Transmission (TX) | V_{ISOTX} | Ref. Test Circuit | | -75 | | dB |

Electrical Characteristics (continued)

($V_{CC} = 5V \pm 5\%$, $V_{DD} = 1.7V$ to $5.5V$. Typical values are $V_{DD} = +2.5V$, $V_{CC} = 5V$, $T_A = +25^\circ C$. Limits are 100% tested at $T_A = +85^\circ C$ and are guaranteed by design in the entire temperature range)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---------------|---|-----|------|-----|--------|
| Off-Isolation in Reception (RX) | V_{ISORX} | Ref. Test Circuit. $Z_L = 50\Omega$ | | -80 | | dB |
| | | Ref. Test Circuit. $Z_L = 1k\Omega // 15pF$ | | -60 | | |
| Crosstalk | V_{CT} | Ref Test Circuit. RX and TX with switches open or closed | | -62 | | dB |
| SW_ Off-Capacitance Small-Signal - NO Pin | C_{SW_OFF} | $f = 5MHz$, $100mV_{PK}$ on NO pin | | 7.7 | | pF |
| SW_ On-Capacitance Small-Signal | C_{SW_ON} | $f = 5MHz$, $100mV_{PK}$ | | 33 | | pF |
| SW_ Off-Capacitance Small-Signal - COM Pin | C_{SW_OFF} | $f = 5MHz$, $100mV_{PK}$ on COM pin | | 11 | | pF |
| SW_ Off-Capacitance Large-Signal - COM Pin | C_{SW_OFF} | $f = 5MHz$, $100V_{PK}$ on COM pin | | 11 | | pF |
| SW_ On-Capacitance Large-Signal | C_{SW_ON} | $f = 5MHz$, $100V_{PK}$ | | 16 | | pF |
| Charge Injection | QCH | Ref. Test Circuit | | <100 | | pC |
| Output Voltage Spike | V_{SPK} | Ref. Test Circuit | | 65 | | mVpkpk |
| Large-signal Analog Bandwidth (-3dB) | f_{BW_L} | $C_{LOAD} = 200pF$, 60V amplitude sinusoidal burst, 1% duty cycle | | >50 | | MHz |
| Small-signal Analog Bandwidth (-3dB) | f_{BW_S} | $C_{LOAD} = 200pF$, 100mV amplitude sinusoidal signal | | 80 | | MHz |
| TIMING CHARACTERISTICS | | | | | | |
| 2nd Harmonic Distortion HV | THD2 | $f_{OUT} = 5MHz$, Transmit amplitude $200V_{PKPK}$ square wave (20 cycles), NO Load: $100\Omega // 100pF$ | | -45 | | dBc |
| Pulse Cancellation 1 Fundamental | PC1 | $f_{OUT_} = 1MHz - 5MHz$, Transmit amplitude $200V_{PKPK}$, 2 cycles. Strength ratio of the strongest spurious signal of the sum function in the $f_0 \pm f_0/2$ bandwidth to the fundamental signal. NO Load: $100\Omega // 100pF$ | | -40 | | dBc |
| Pulse Cancellation 2 Second Harmonic | PC2 | $f_{OUT_} = 1MHz - 5MHz$, Transmit Amplitude $200V_{PKPK}$, 2 cycles. Strength ratio of the strongest spurious signal of the sum function in the $2 \times f_0 \pm f_0/2$ bandwidth to the fundamental signal. NO Load: $100\Omega // 100pF$ | | -40 | | dBc |

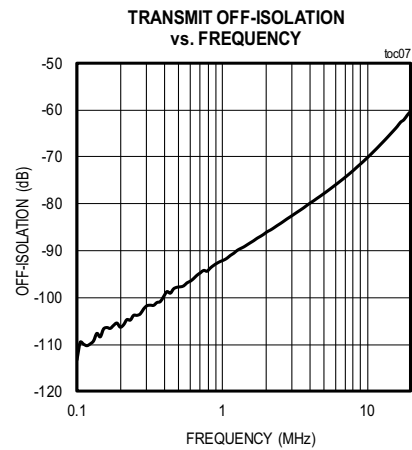
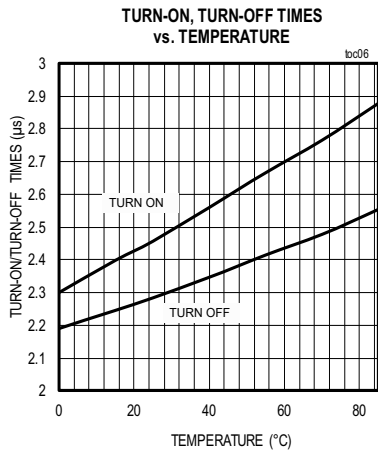
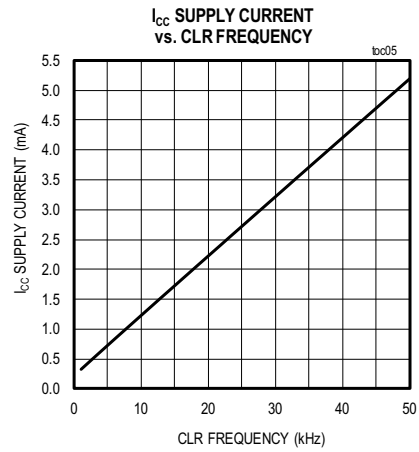
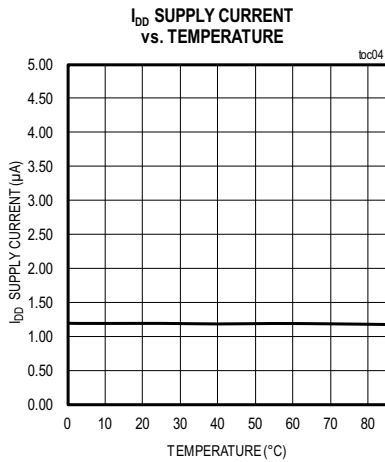
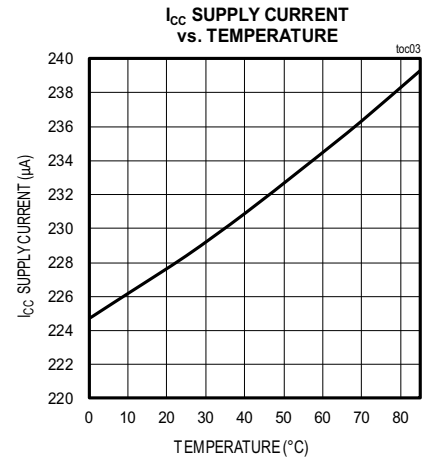
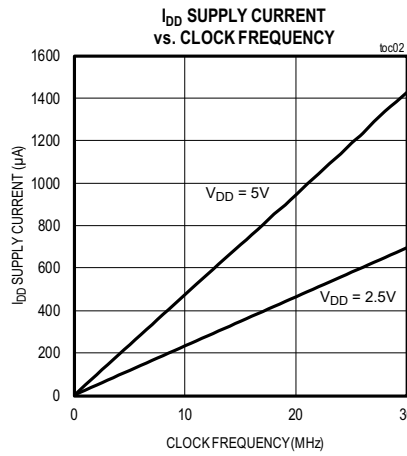
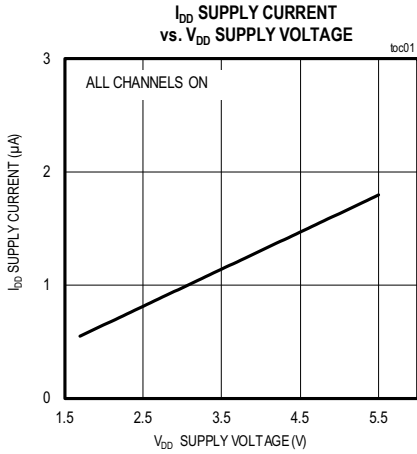
Electrical Characteristics (continued)

($V_{CC} = 5V \pm 5\%$, $V_{DD} = 1.7V$ to $5.5V$. Typical values are $V_{DD} = +2.5V$, $V_{CC} = 5V$, $T_A = +25^\circ C$. Limits are 100% tested at $T_A = +85^\circ C$ and are guaranteed by design in the entire temperature range)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|------------|---|-----|-----|-----|-------|
| TIMING CHARACTERISTICS/SPI TIMINGS | | | | | | |
| CLK Frequency | f_{CLK} | | | | 30 | MHz |
| DIN to CLK Setup Time | t_{DS} | | 3 | | | ns |
| DIN to CLK Hold Time | t_{DH} | | 3 | | | ns |
| CLK to \overline{LE} Setup Time | t_{CS} | | 3 | | | ns |
| \overline{LE} Low Pulse Width | t_{WL} | | 5 | | | ns |
| CLR High Pulse Width | t_{WC} | | 115 | | | ns |
| SET High Pulse Width | t_{WS} | | 115 | | | ns |
| CLK Rise and Fall Times | t_R, t_F | | | | 50 | ns |
| CLK to DOUT Delay | t_{DO} | V_{DD} from 2.5V - 5% to 5V + 5%, CDOUT = 15pF | 5 | | 20 | ns |
| | | $V_{DD} = +1.8V \pm 5\%$, CDOUT = 15pF | 5 | | 30 | |

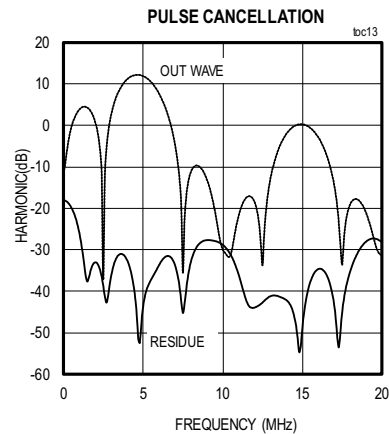
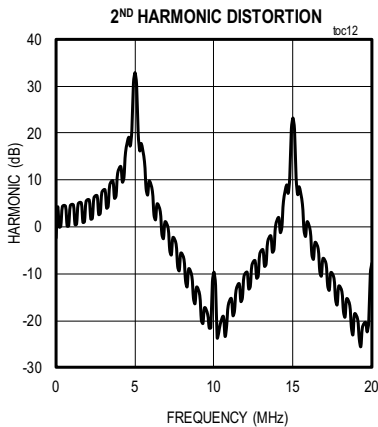
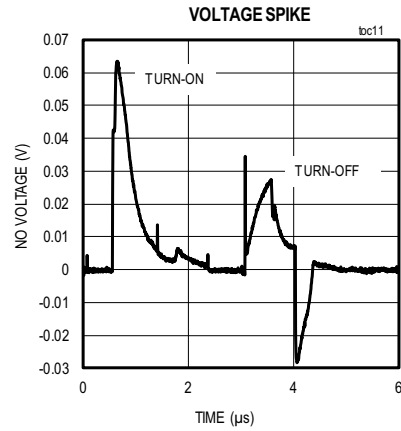
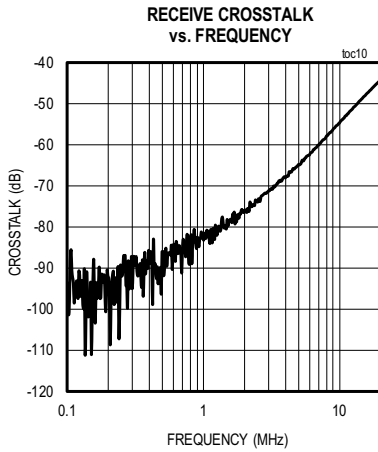
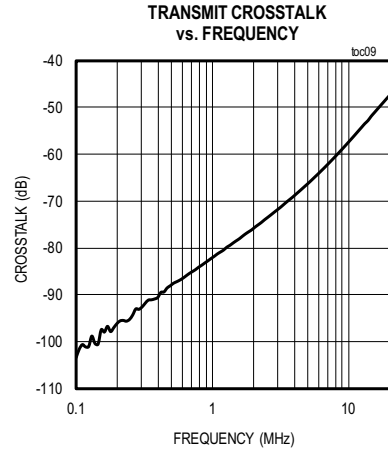
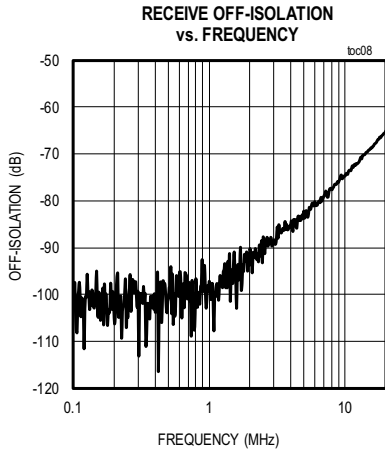
Typical Operating Characteristics

$V_{DD} = 3V$, $V_{CC} = 5V$, $T_A = 25^\circ C$, unless otherwise noted.

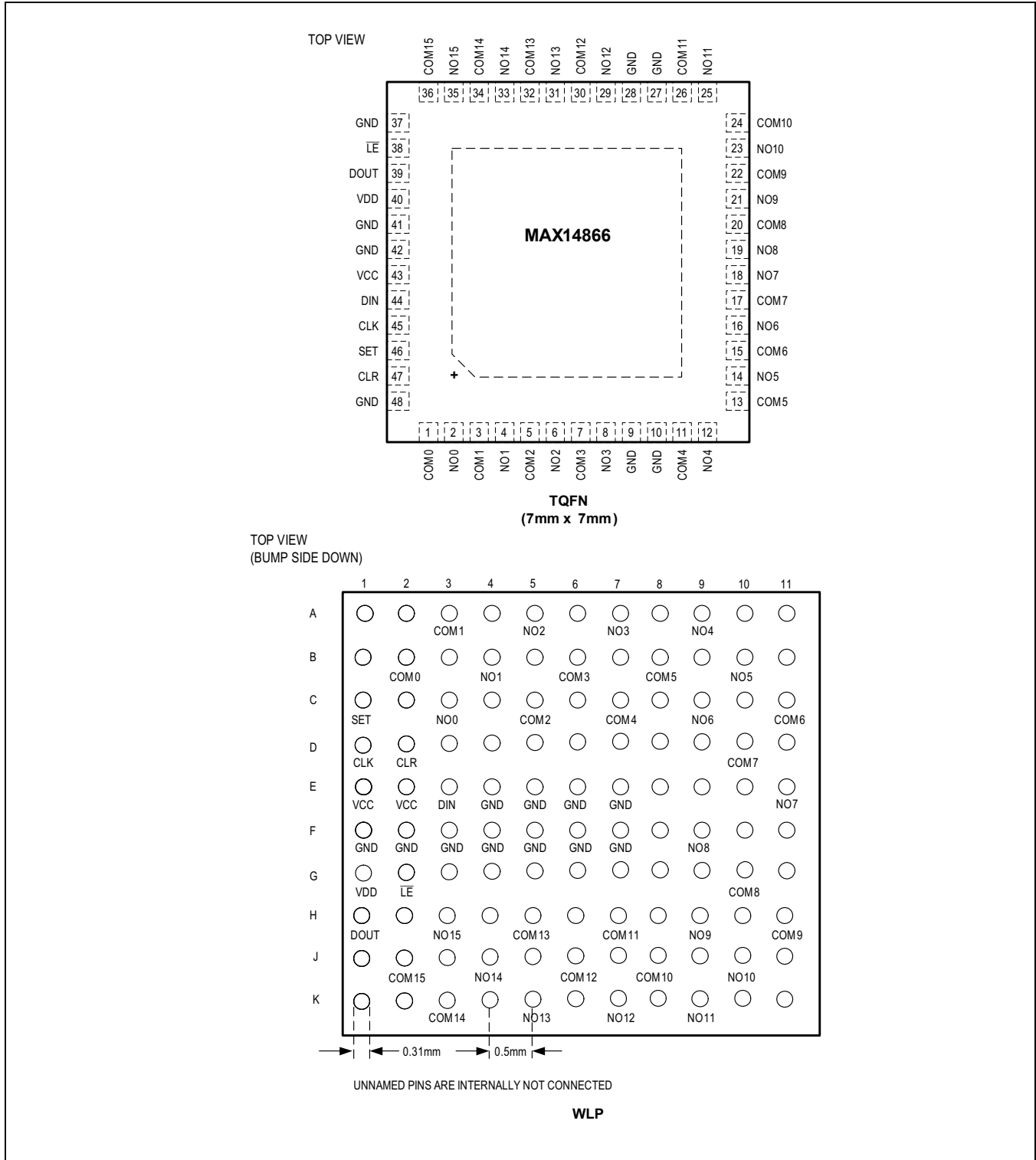


Typical Operating Characteristics (continued)

V_{DD} = 3V, V_{CC} = 5V, T_A = 25°C, unless otherwise noted.



Pin Configurations



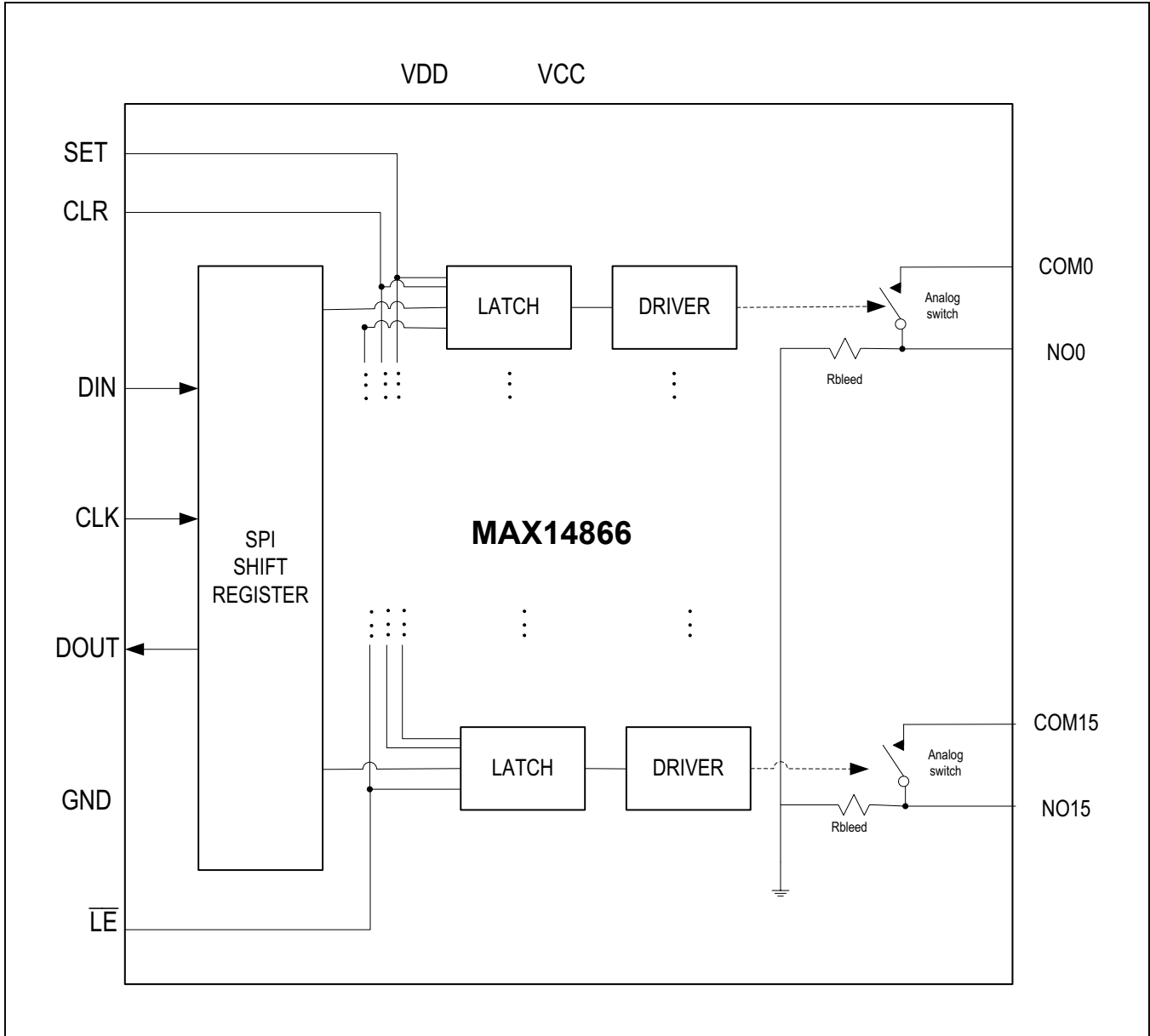
Pin Description

| PIN | | NAME | FUNCTION |
|--------------|---------------|-------|-----------------------------|
| MAX14866 WLP | MAX14866 TQFN | | |
| B2 | 1 | COM0 | Analog Switch 0 - Terminal |
| C3 | 2 | NO0 | Analog Switch 0 - Terminal |
| A3 | 3 | COM1 | Analog Switch 1 - Terminal |
| B4 | 4 | NO1 | Analog Switch 1 - Terminal |
| C5 | 5 | COM2 | Analog Switch 2 - Terminal |
| A5 | 6 | NO2 | Analog Switch 2 - Terminal |
| B6 | 7 | COM3 | Analog Switch 3 - Terminal |
| A7 | 8 | NO3 | Analog Switch 3 - Terminal |
| E4–E7 | 9 | GND | Ground |
| F1–F7 | 10 | GND | Ground |
| C7 | 11 | COM4 | Analog Switch 4 - Terminal |
| A9 | 12 | NO4 | Analog Switch 4 - Terminal |
| B8 | 13 | COM5 | Analog Switch 5 - Terminal |
| B10 | 14 | NO5 | Analog Switch 5 - Terminal |
| C11 | 15 | COM6 | Analog Switch 6 - Terminal |
| C9 | 16 | NO6 | Analog Switch 6 - Terminal |
| D10 | 17 | COM7 | Analog Switch 7 - Terminal |
| E11 | 18 | NO7 | Analog Switch 7 - Terminal |
| F9 | 19 | NO8 | Analog Switch 8 - Terminal |
| G10 | 20 | COM8 | Analog Switch 8 - Terminal |
| H9 | 21 | NO9 | Analog Switch 9 - Terminal |
| H11 | 22 | COM9 | Analog Switch 9 - Terminal |
| J10 | 23 | NO10 | Analog Switch 10 - Terminal |
| J8 | 24 | COM10 | Analog Switch 10 - Terminal |
| K9 | 25 | NO11 | Analog Switch 11 - Terminal |
| H7 | 26 | COM11 | Analog Switch 11 - Terminal |
| | 27 | GND | Ground |
| | 28 | GND | Ground |
| K7 | 29 | NO12 | Analog Switch 12 - Terminal |
| J6 | 30 | COM12 | Analog Switch 12 - Terminal |
| K5 | 31 | NO13 | Analog Switch 13 - Terminal |
| H5 | 32 | COM13 | Analog Switch 13 - Terminal |
| J4 | 33 | NO14 | Analog Switch 14 - Terminal |

Pin Description (continued)

| PIN | | NAME | FUNCTION |
|--|---------------|-----------------|---|
| MAX14866 WLP | MAX14866 TQFN | | |
| K3 | 34 | COM14 | Analog Switch 14 - Terminal |
| H3 | 35 | NO15 | Analog Switch 15 - Terminal |
| J2 | 36 | COM15 | Analog Switch 15 - Terminal |
| | 37 | GND | Ground |
| G2 | 38 | \overline{LE} | CMOS Digital Logic Input. Active-Low Latch Enable Input |
| H1 | 39 | DOUT | CMOS Digital Logic Output - SPI Data Output |
| G1 | 40 | VDD | Positive LV supply input for digital I/O (from 1.7V to 5.5V). Bypass VDD to GND with a 0.1 μ F or greater ceramic capacitor |
| | 41 | GND | Ground |
| | 42 | GND | Ground |
| E1, E2 | 43 | VCC | Positive LV Supply Input (+5V). Bypass VCC to GND with a 0.1 μ F or greater ceramic capacitor |
| E3 | 44 | DIN | CMOS Digital Logic Input - SPI Data Input |
| D1 | 45 | CLK | CMOS Digital Logic Input - SPI Clock Input |
| C1 | 46 | SET | CMOS Digital Logic Input - Asynchronous Set Input |
| D2 | 47 | CLR | CMOS Digital Logic Input - Asynchronous Clear Input |
| | 48 | GND | Ground |
| — | EP | | Exposed PAD (Thermal PAD). Connet EP to GND |
| A1, A2, A4, A6, A8, A10, A11, B1, B3, B5, B7, B9, B11, C2, C4, C6, C8, C10, D3-D9, D11, E8-E10, F8, F10, F11, G3-G9, G11, H2, H4, H6, H8, H10, J1, J3, J5, J7, J9, J11, K1, K2, K4, K6, K8, K10, K11 | — | N.C. | Not internally connected |

Functional (or Block) Diagram



Detailed Description

The MAX14866 is a 16-channel, high-voltage (HV), Analog SPST switch primarily intended for HV multiplexing in ultrasound applications.

The MAX14866 operates from one only low voltage supply (+5V) and does not require dedicated HV supplies resulting in cost saving and system simplification. Moreover, for in-probe applications, HV supplies do not need to be associated with the MAX14866 in the probe/transducer head, resulting in greater safety and easier compliance to safety regulations.

The MAX14866 features best-in-class performances in terms of bandwidth (up to 50MHz), charge injection (<100pC) and linear transmit input range (up to 210V_{PKPK}). The low signal switch R_{DSON} is typically about 7 Ω around 0V and remains flat in the entire input range ensuring extremely good linearity.

The latch-up free SOI (Silicon-on-Insulator) technology and the wide analog range results in extremely high robustness during undershoots and overshoots which occur in ultrasound systems due to the resonant nature of the load.

The status of the switches can be individually controlled through a high speed SPI interface (up to 30MHz). Daisy-chain architecture is supported.

Alternatively, switches can also be controlled with global control signal (SET and CLR) for bank selections or relay replacement applications.

The MAX14866 is offered in two different packages: wafer-level package (WLP) and Thin-QFN (TQFN). The 110-Bump WLP size is only 5.53 x 5.47mm, resulting in less than 1.9mm²/channel footprint and allowing for very high levels of integration which is beneficial especially for in-probe applications.

The size of the TQFN package is an industry standard 48-pin 7mm x 7mm package.

Analog Switches

The MAX14866 can transmit undistorted analog signals up to 210V_{P-P}. For reliable operation, the maximum drop between input and output of the switch (pins COM and NO) must be less than 110V (refer to the absolute maximum rating in the [Electrical Characteristics](#) table)

It is required that the input signal is set at GND prior to HV transmission. The minimum guaranteed transmit frequency is 500KHz. The switch is not symmetrical. Transducer elements must be connected to pin named NO_x (x = 0..15) while the transmit/receive front end circuits must be connected to the pin named COM_x (x = 0..15). Refer to the [Typical Application Circuit](#) for further details.

Voltage Supply

The MAX14866 operates from a low voltage supply $V_{CC} = +5V \pm 5\%$, and a logic supply V_{DD} (from +1.7V to +5.5V). In particular, if the logic high level of the control input signals (SPI, CLR, SET) is +5V, the two supply voltage inputs V_{DD} and V_{CC} can be connected together and the part can operate from one single +5V supply.

Local bypassing on supply voltage inputs is required ($C > 100nF$).

Bleed Resistors

The MAX14866 features integrated bleed resistors. Bleed resistors are intended to fully discharge the transducers and eliminate any voltage built up. The bleed resistor values depends on the status of the switch. Refer to the [Electrical Characteristics](#) table and to [Figure 1](#) for further details.

Heading RST

The MAX14866 Equivalent Electrical Circuit is shown in [Figure 1](#) under different conditions depending on the status of the switch (on/off) and on the level of the signal (small-signal/large-signal).

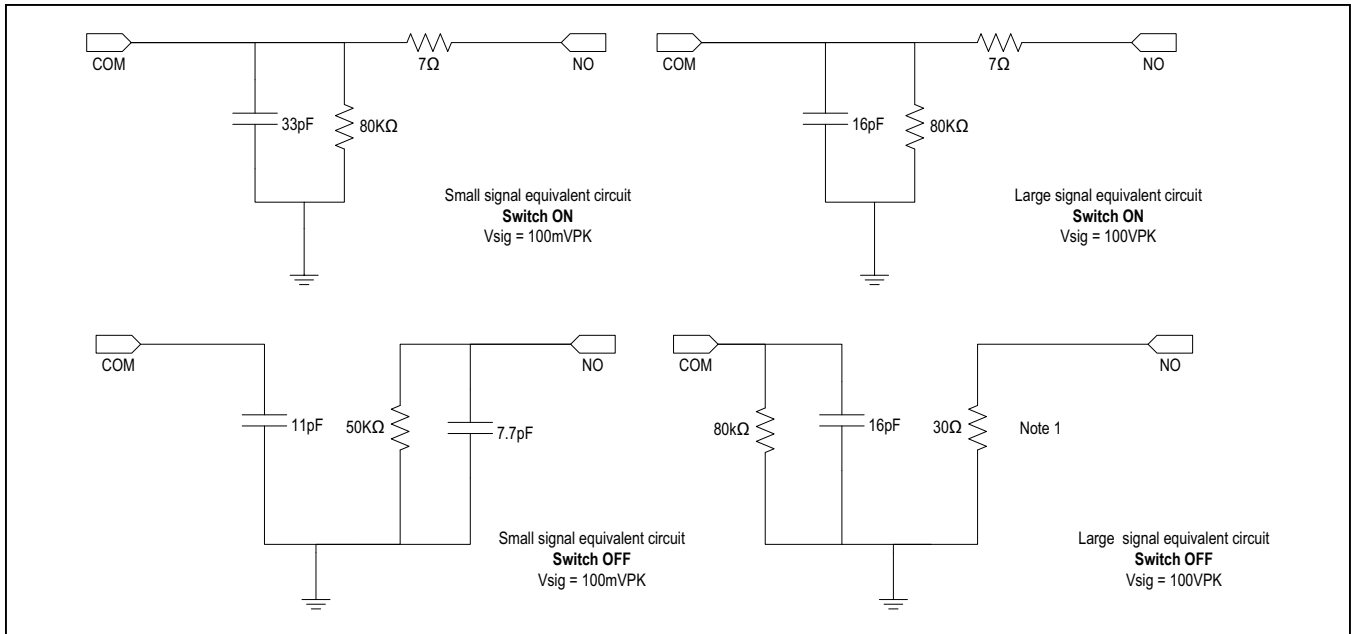


Figure 1. Electrical Equivalent Circuit

Note 3: The large-signal NO equivalent input impedance (30Ω typical) is shown for completeness only. It is intended that the High Voltage excitation signals are applied to terminal COM only so that no any HV transmit burst will hit terminal NO whenever the switch is programmed off.

Note 4: Resistances and capacitances values are typical.

Transmit Operations: High-Voltage Bursts (Voltage Amplitude Greater Than 20V_{PKPK})

The MAX14866 is capable of transmitting long High Voltage Bipolar Bursts (from 40V_{PKPK} to 210V_{PKPK}) with excellent linearity and stability. When transmitting Bipolar HV bursts (amplitude greater than 20V_{PK}) the device is not sensitive to the DC content of the signal.

In particular, the MAX14866 supports long burst excitation modes like the ones commonly used in Elastography. The user must ensure that the total dissipated power can be handled by the package.

Unipolar transmission is supported up to 100V_{pk-to-pk} only.

For reliability reasons, it is requested that both the switch input and output (COM and NO pins) are set at ground before the transmission is initiated.

Transmit Operations: Continuous Wave

Bipolar Continuous Wave Operation (CW) is supported for transmit voltages less than 20V_{PKPK} (amplitude less than 10V). It is required that the DC content (offset) of the CW transmit waveform is less than ±1V. Larger DC

offsets during CW operation results in signal degradation and can affect the device reliability. In particular, unipolar CW operation is not supported.

Serial Interface

The MAX14866 is controlled by a serial interface with a 16-bit serial shift register and transparent latch. Each of the 16 data bits controls a single analog switch (see Table 1). Data on DIN is clocked with the most significant bit (MSB) first into the shift register on the rising edge of CLK. Data is clocked out of the shift register onto DOUT on the rising edge of CLK. DOUT reflects the status of DIN, delayed by 16 clock cycles (see Figure 2 and Figure 3).

Changing the switch status (from on to off or vice-versa) during the transmission of the analog signal is not permitted and can result in reliability issues. The user must ensure that the analog input is kept quiet at GND before any SPI programming session and during the entire settling time of the switches (T_{ON}, T_{OFF}). Similarly the user must ensure that the analog input is quiet at GND before asserting either the CLR or the SET signal and during the entire settling time of the switches (T_{ON}, T_{OFF}).

Table 1. SPI Programming and Logic Table

| DATA BITS | | | | | | | | CONTROL BITS | | | | | | | | FUNCTION | | |
|-----------|----|----|----|----|----|----|----|-----------------|-----|-----|-----|-----|-----|-----|-----|----------|-----|-----|
| D0 (LSB) | D1 | D2 | D3 | D4 | D5 | D6 | D7 | \overline{LE} | CLR | SET | SW0 | SW1 | SW2 | SW3 | SW4 | SW5 | SW6 | SW7 |
| L | | | | | | | | L | L | L | OFF | | | | | | | |
| H | | | | | | | | L | L | L | ON | | | | | | | |
| | L | | | | | | | L | L | L | | OFF | | | | | | |
| | H | | | | | | | L | L | L | | ON | | | | | | |
| | | L | | | | | | L | L | L | | | OFF | | | | | |
| | | H | | | | | | L | L | L | | | ON | | | | | |
| | | | L | | | | | L | L | L | | | | OFF | | | | |
| | | | H | | | | | L | L | L | | | | ON | | | | |
| | | | | L | | | | L | L | L | | | | | OFF | | | |
| | | | | H | | | | L | L | L | | | | | ON | | | |
| | | | | | L | | | L | L | L | | | | | | OFF | | |
| | | | | | H | | | L | L | L | | | | | | ON | | |
| | | | | | | L | | L | L | L | | | | | | | | OFF |
| | | | | | | H | | L | L | L | | | | | | | | ON |
| X | X | X | X | X | X | X | X | H | L | L | | | | | | | | |
| X | X | X | X | X | X | X | X | X | H | X | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF |
| X | X | X | X | X | X | X | X | X | L | H | ON | ON | ON | ON | ON | ON | ON | ON |

| DATA BITS | | | | | | | | CONTROL BITS | | | | | | | | FUNCTION | | |
|-----------|----|-----|-----|-----|-----|-----|-----------|-----------------|-----|-----|-----|-----|------|------|------|----------|------|------|
| D8 | D9 | D10 | D11 | D12 | D13 | D14 | D15 (MSB) | \overline{LE} | CLR | SET | SW8 | SW9 | SW10 | SW11 | SW12 | SW13 | SW14 | SW15 |
| L | | | | | | | | L | L | L | OFF | | | | | | | |
| H | | | | | | | | L | L | L | ON | | | | | | | |
| | L | | | | | | | L | L | L | | OFF | | | | | | |
| | H | | | | | | | L | L | L | | ON | | | | | | |
| | | L | | | | | | L | L | L | | | OFF | | | | | |
| | | H | | | | | | L | L | L | | | ON | | | | | |
| | | | L | | | | | L | L | L | | | | OFF | | | | |
| | | | H | | | | | L | L | L | | | | ON | | | | |
| | | | | L | | | | L | L | L | | | | | OFF | | | |
| | | | | H | | | | L | L | L | | | | | ON | | | |
| | | | | | L | | | L | L | L | | | | | | OFF | | |
| | | | | | H | | | L | L | L | | | | | | ON | | |

Table 1. SPI Programming and Logic Table (continued)

| DATA BITS | | | | | | | | CONTROL BITS | | | | | | | | FUNCTION | | | |
|-----------|----|-----|-----|-----|-----|-----|-----------|-----------------|-----|-----|---------------------|-----|------|------|------|----------|------|------|--|
| D8 | D9 | D10 | D11 | D12 | D13 | D14 | D15 (MSB) | \overline{LE} | CLR | SET | SW8 | SW9 | SW10 | SW11 | SW12 | SW13 | SW14 | SW15 | |
| | | | | | | L | | L | L | L | | | | | | | OFF | | |
| | | | | | | H | | L | L | L | | | | | | | ON | | |
| | | | | | | | L | L | L | L | | | | | | | | OFF | |
| | | | | | | | H | L | L | L | | | | | | | | ON | |
| X | X | X | X | X | X | X | X | H | L | L | HOLD PREVIOUS STATE | | | | | | | | |
| X | X | X | X | X | X | X | X | X | H | X | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | |
| X | X | X | X | X | X | X | X | X | L | H | ON | ON | ON | ON | ON | ON | ON | ON | |

Note 5: The 16 switches operate independently.

Note 6: Serial data is clocked in on the rising edge of CLK.

Note 7: The switches go to a state retaining their present condition on the rising edge of \overline{LE} . When \overline{LE} is low, the shift register data flows through the latch.

Note 8: D_{OUT} is the data output pin of the 16 bits shift register. It always reflects the status of DIN delayed by 16 clock cycles.

Note 9: Shift register clocking has no effect on the switch states if \overline{LE} is high.

Note 10: The CLR input overrides all other inputs.

SPI Programming Inhibition During Transmit

The MAX14866 cannot be programmed during the transmission of HV bursts. The device features a transmit detector circuit. If a transmit input signal greater than $\pm 2V$ is detected, any SPI programming is inhibited for 4.5 μ s max. During such an interval any attempts of programming the part via the SPI is ignored and the previous device status is hold. This function prevents faults caused by false programming of the logic due to the large switching noise occurring during HV transmit.

\overline{LE} description

Drive \overline{LE} logic-low to change the contents of the latch and update the state of the high-voltage switches (Figure 3). Drive \overline{LE} logic-high to freeze the contents of the latch and prevent changes to the switch states. To reduce noise due to clock feedthrough, drive \overline{LE} logic-high while data is clocked into the shift register. After the data shift register is loaded with valid data, pulse \overline{LE} logic-low to load the contents of the shift register into the latch.

CLR description

The MAX14866 features a latch clear input. Drive CLR logic-high to reset the contents of the latch to zero and open all switches. CLR does not affect the contents of the data shift register. Pulse \overline{LE} logic-low to reload the contents of the shift register into the latch.

SET description

The MAX14866 features a latch set input. Drive SET logic-high to set the contents of the latch to logic-high and close all switches. SET does not affect the contents of the data shift register. Pulse \overline{LE} logic-low to reload the contents of the shift register into the latch. CLR is dominant with respect to SET.

Power-On reset

The MAX14866 features a power-on-reset circuit to ensure all switches are open at power-on. The internal 16-bit serial shift register and latch are set to zero on power-up.

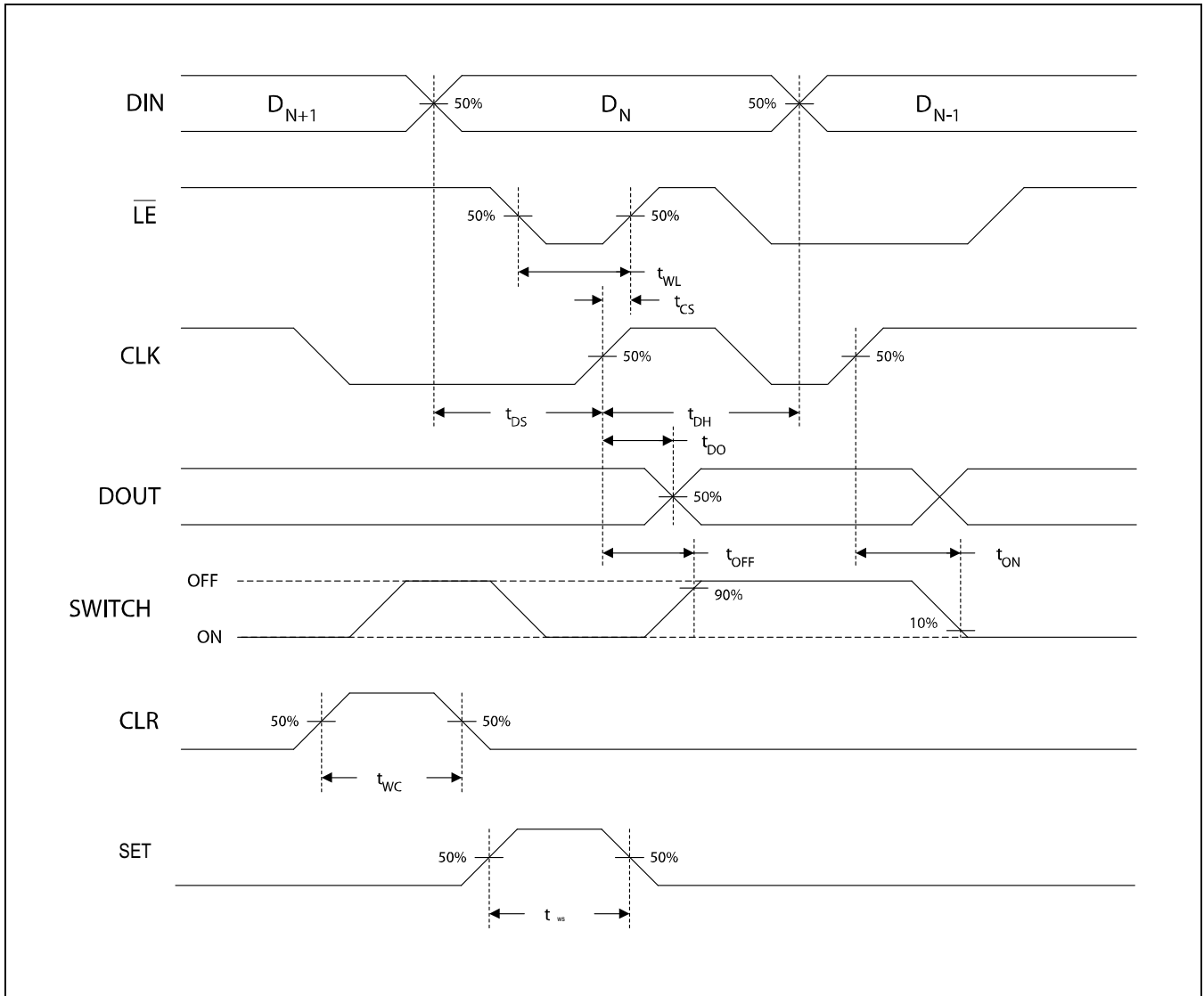


Figure 2. Timings

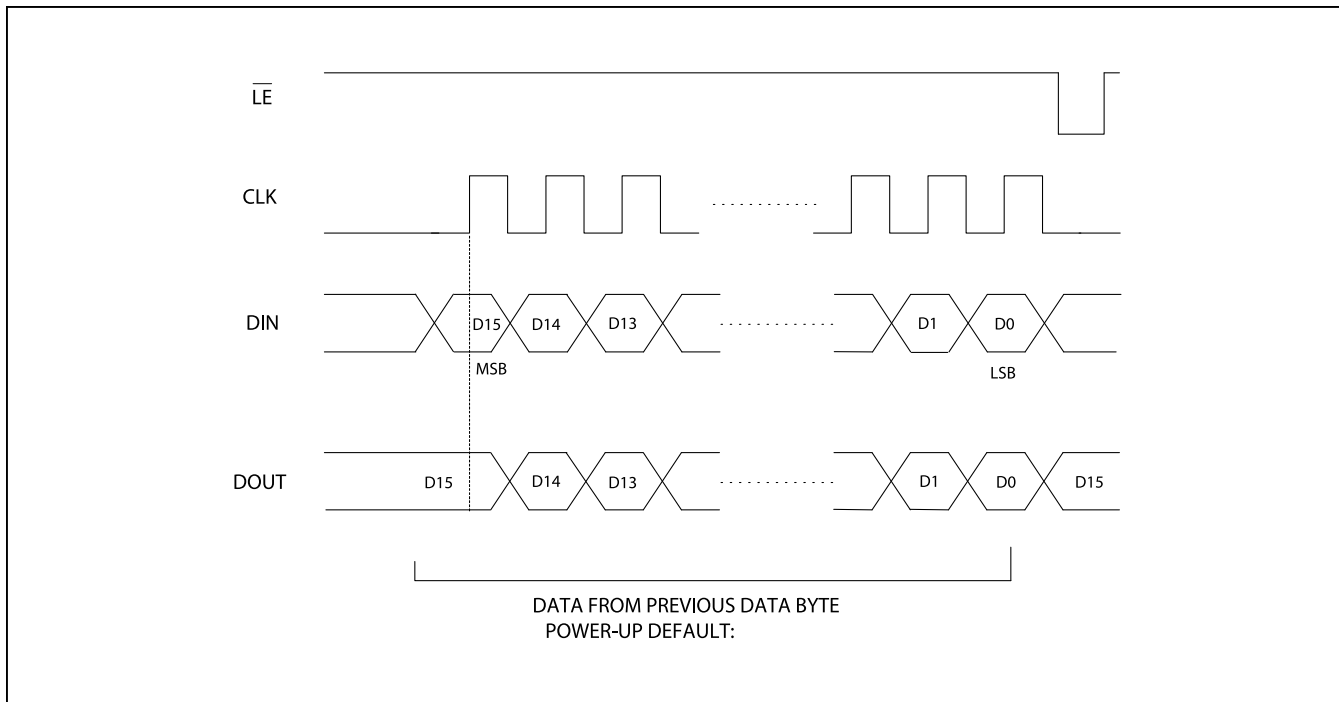
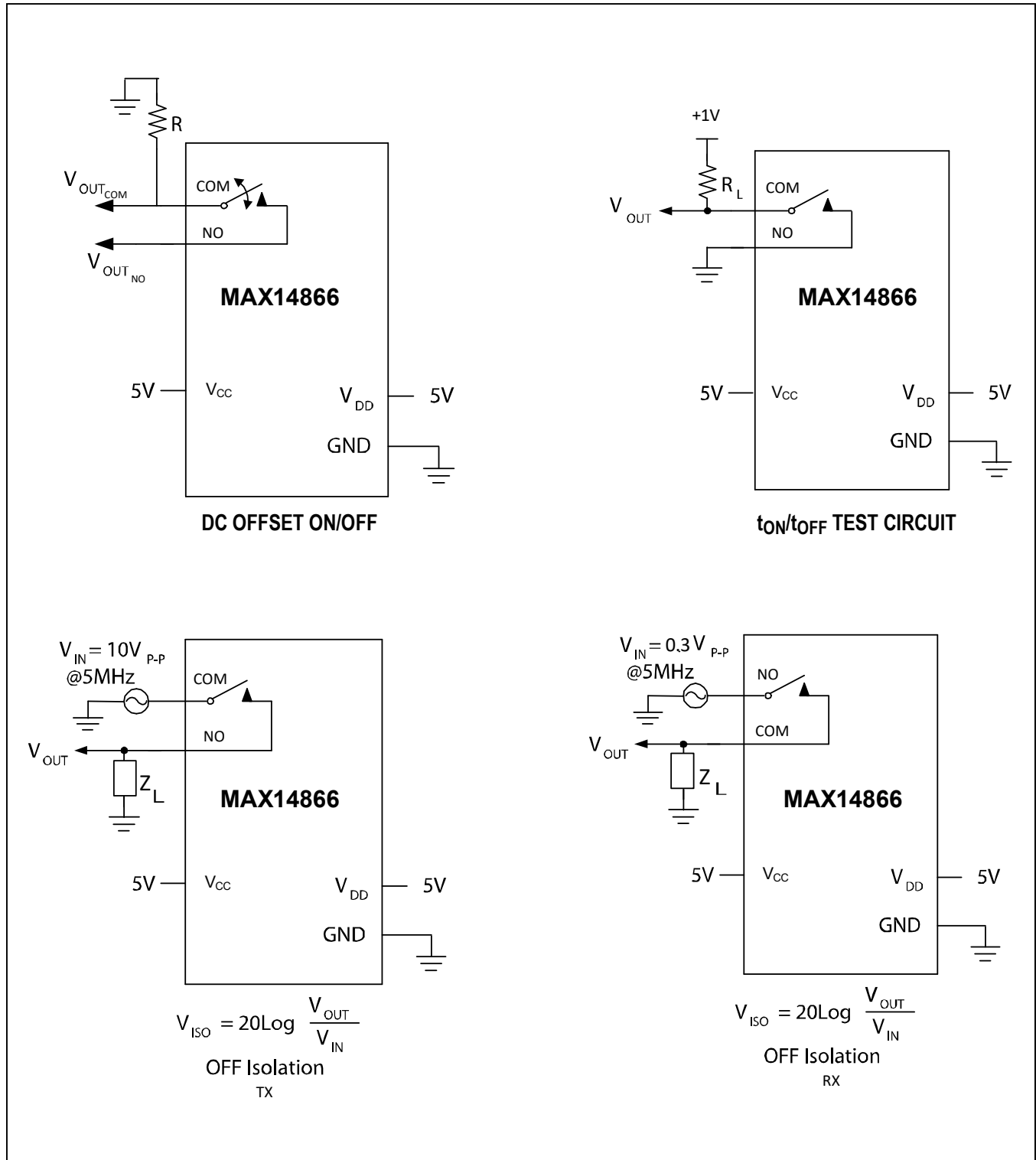
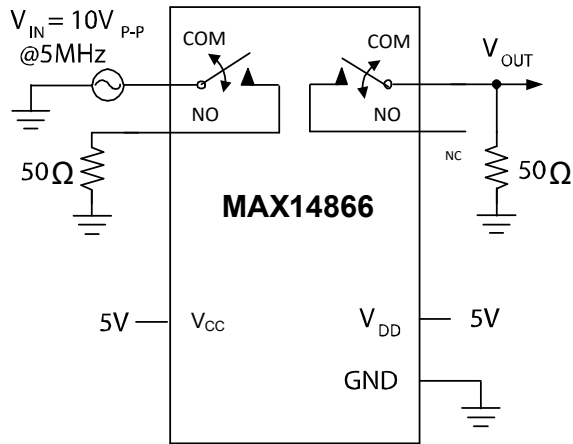


Figure 3. SPI Programming

Test Circuits 1



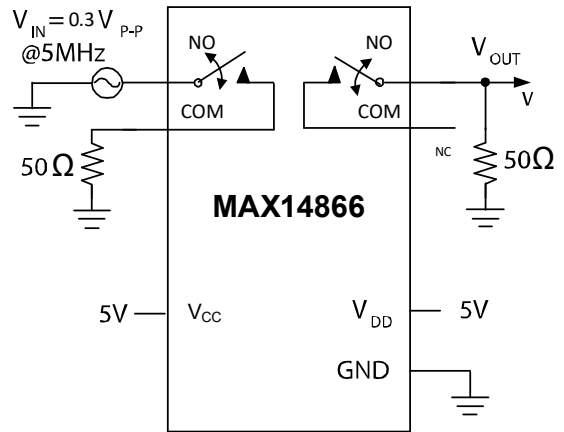
Test Circuits 2



$$V_{CT} = 20 \text{Log} \frac{V_{OUT}}{V_{IN}}$$

Crosstalk TX

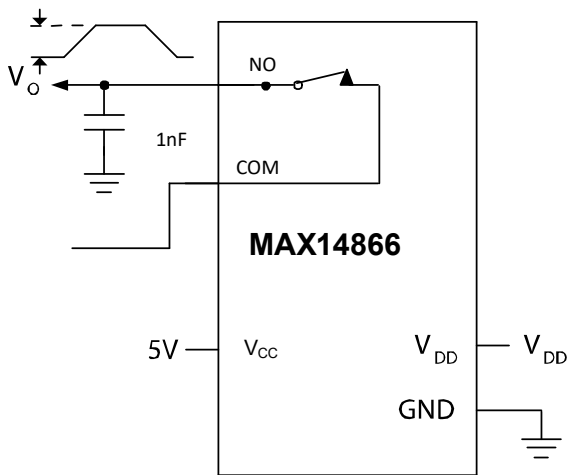
SWITCHES ON OR OFF



$$V_{CT} = 20 \text{Log} \frac{V_{OUT}}{V_{IN}}$$

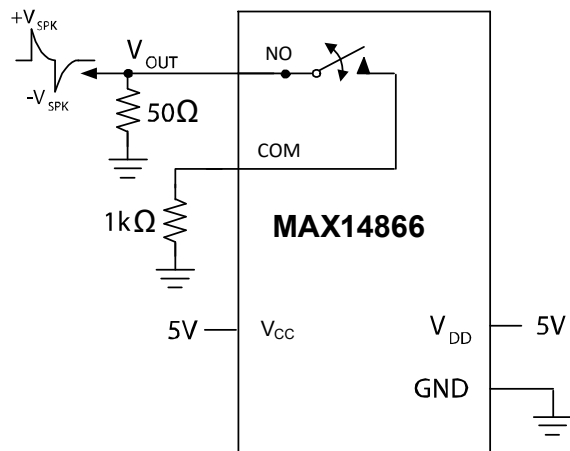
Crosstalk RX

SWITCHES ON OR OFF



$$Q = 1\text{nF} * V_{OUT}$$

CHARGE INJECTION



OUTPUT VOLTAGE SPIKE

Applications Information

Power Supply

The MAX14866 does not require dedicated high-voltage supplies; at a minimum, the device operates from a single LV supply only ($V_{CC} = V_{DD} = +5V$).

V_{DD} (supply voltage input for CMOS logic input) can be set at a lower voltage than V_{CC} and can vary from +1.8V to +5V depending on the voltage level of CMOS logic signals.

Logic Inputs

The MAX14866 digital interface inputs CLK, DIN, \overline{LE} , CLR, SET operate on the V_{DD} logic supply voltage.

Daisy Chain

Digital output DOUT is provided to allow the programming of multiple MAX14866 devices in daisy-chain configuration (Figure 4). Connect each DOUT to the DIN of the subsequent device in the chain. Connect CLK, \overline{LE} , CLR, and SET inputs of all devices, and drive \overline{LE} logic-low to update all devices simultaneously. Drive CLR high to open all the switches simultaneously.

Banks-Switching Applications

For relay replacement applications or any application in which the user needs to control the status of all the switches simultaneously so that independent control is not needed (bank selection, bi-plane or triplane probes, multidimensional array etc ..), CLR and SET command can be used to control the status of all the switches simultaneously. Notice that the CLR logic input is dominant with respect to the SET logic input so that CLR = SET = High corresponds to a Clear command (see Table 1). Therefore, in these applications, one only control signal is required since the the user can toggle the CLR signal only while the SET input can be tied to V_{DD} . Whenever the SPI is not used, connect DIN and CLK to GND and \overline{LE} to V_{DD} and leave DOUT unconnected.

Power Sequencing and Bypassing

The MAX14866 does not require special sequencing of the V_{DD} , V_{CC} supply voltages. Bypass V_{DD} , V_{CC} to GND with greater than 0.1 μ F ceramic capacitor as close as possible to the device.

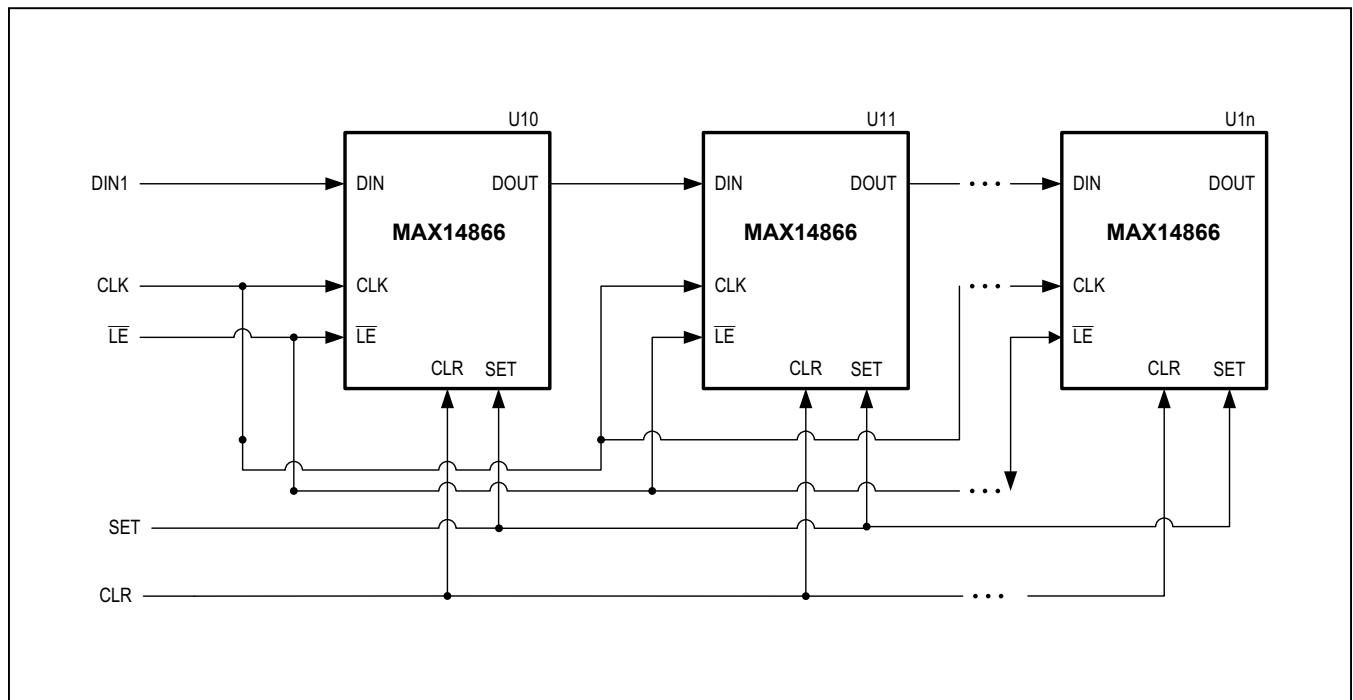


Figure 4. Daisy-Chain Connection

Typical Application Circuit

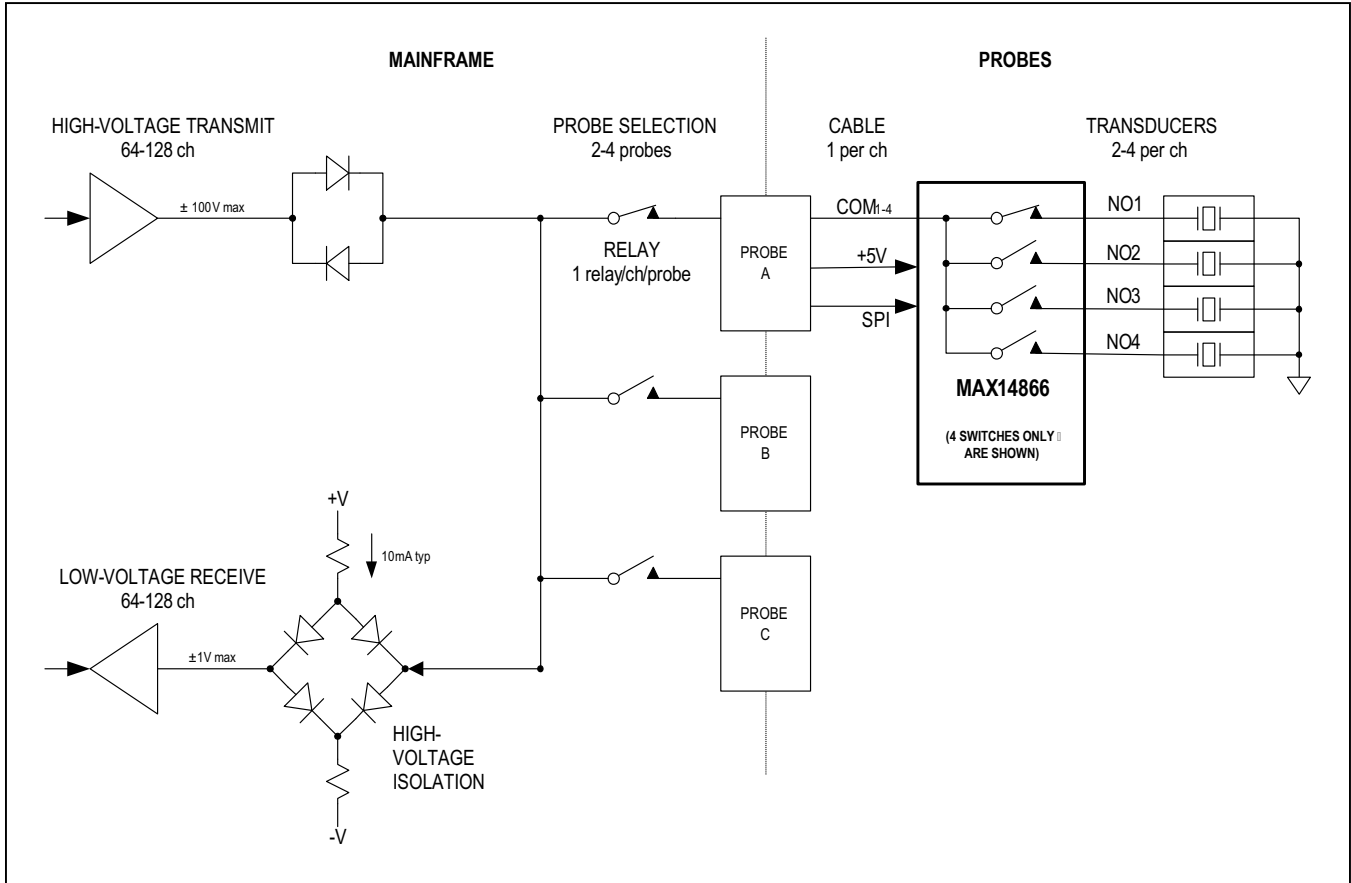


Figure 5. Application Diagram

MAX14866

16-Channel, High-Voltage Analog Switch without High-Voltage Supply Requirement

Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|--------------|-------------|------------------------------|
| MAX14866UWZ+ | 0°C to 85°C | 110 WLP (5.47mm x 5.53mm) |
| MAX14866UTM+ | 0°C to 85°C | 48 TQFN (7mm x 7mm) |

+Denotes a lead (Pb)-free package/RoHS-compliant package

Chip Information

PROCESS: DiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|--------------|--------------|-----------------------------|--|
| 110 Bump WLP | W1105C5+1 | 21-11001051 | Refer to Application Note 1891 |
| 48 Pin TQFN | T4877+6 | 90-0130 | Refer to Application Note 1891 |

MAX14866

16-Channel, High-Voltage Analog Switch
without High-Voltage Supply Requirement

Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|-----------------|---------------|--------------------------------------|---------------|
| 0 | 7/17 | Initial release | — |
| 1 | 4/18 | Updated <i>Pin Description</i> table | 10 |

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

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