ADP4100

Product Preview

Programmable Multi-Phase Synchronous Buck Converter

The ADP4100 is an integrated power control IC for VR11.1 applications. The ADP4100 can be programmed for 1−, 2−, 3−, 4−, 5− or 6−phase operation, allowing for the construction of up to six complementary buck switching stages. The ADP4100 supports $\overline{\text{PSI}}$, which is a power state indicator and can be used to reduce number of operating phases at light loads.

The ADP4100 is optimized for converting a 12 V main supply into the core supply voltage required by high performance Intel processors. It uses an internal 8−bit DAC to read the voltage identification (VID) code directly from the processor, which is used to set the output voltage between 0.375 V and 1.6 V.

Features

- Supports Both VR11 and VR11.1 Specifications
- Digitally Programmable 0.375 V to 1.6 V Output
- Selectable 1−, 2−, 3−, 4−, 5− or 6−Phase Operation
- Fast−Enhanced PWM FlexMode™
- TRDET to Improve Load Release
- Active Current Balancing Between All Output Phases
- Supports On−The−Fly (OTF) VID Code Changes
- Supports $\overline{\text{PSI}}$ − Power Saving Mode
- Short Circuit Protection with Latchoff Delay
- This is a Pb−Free Device

Typical Applications

- Servers
- Desktop PC's
- POLs (Memory)

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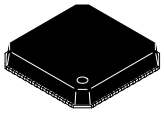
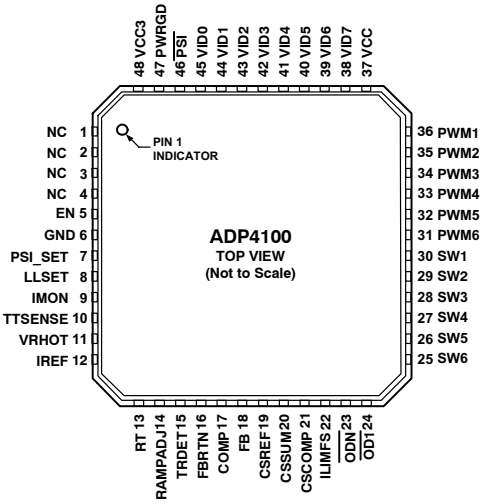
LFCSP48
CASE 932AD



MARKING DIAGRAM

xx = Device Code
# = Pb−Free Package
YYWW = Date Code
XXX = Assembly Lot
CCC = Country of Origin

PIN ASSIGNMENT



ORDERING INFORMATION

Device*	Package	Shipping†
ADP4100JCPZ−REEL	LFCSP48	2500/Tape & Reel
ADP4100JCPZ−RL7	LFCSP48	750/Tape & Reel

*The "Z' suffix indicates Pb−Free package.
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

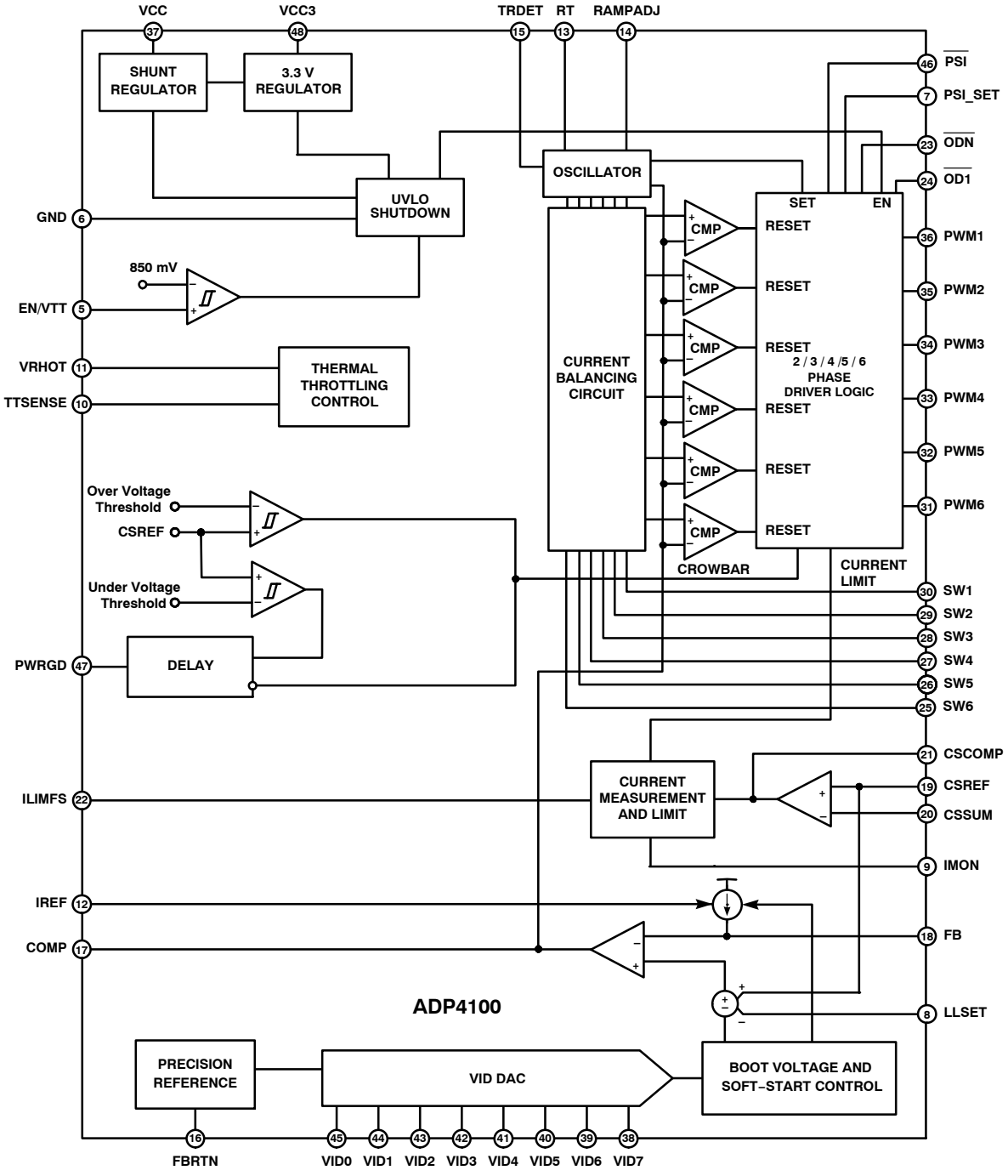


Figure 1. Simplified Block Diagram

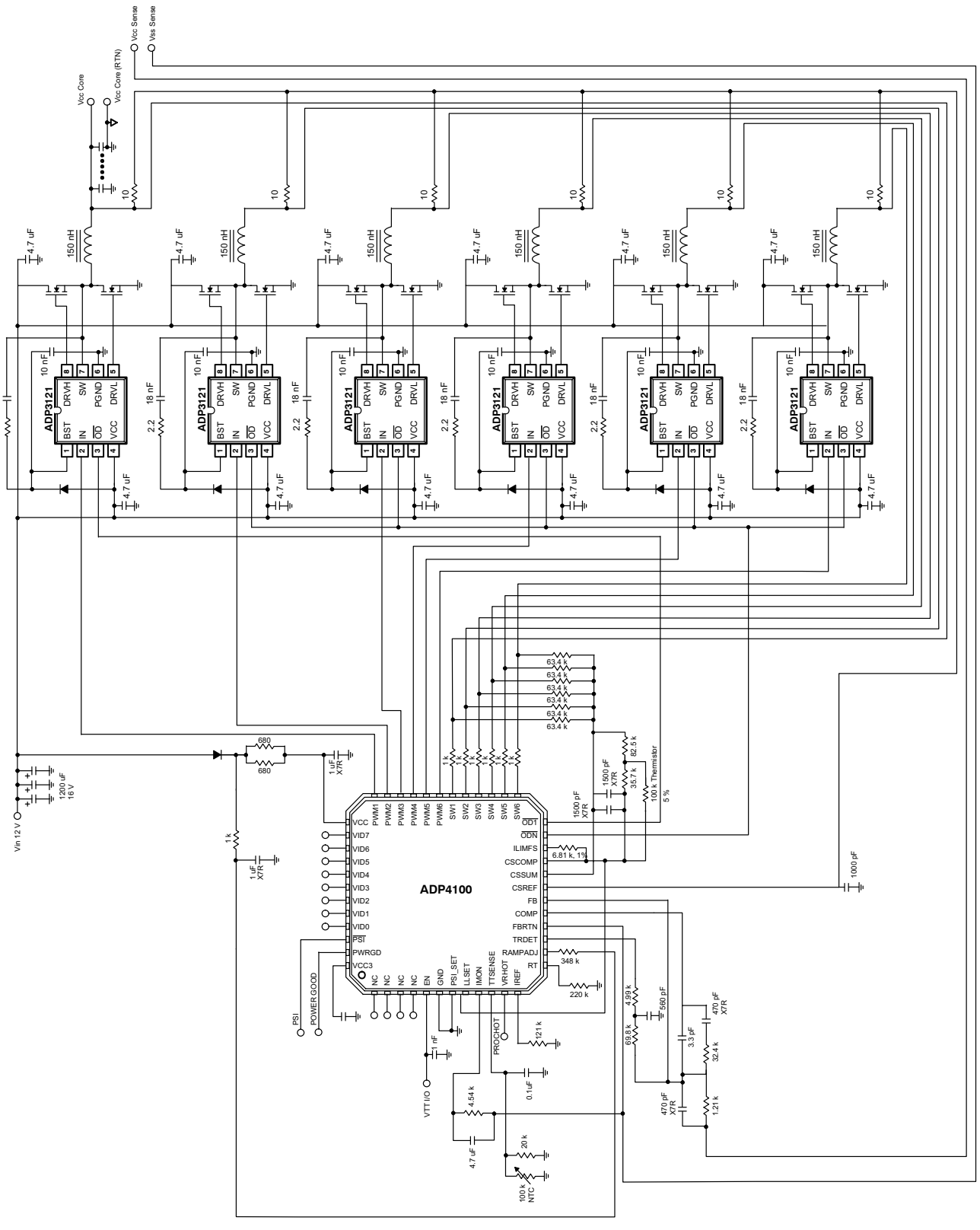


Figure 2. Application Schematic

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage Range (Note 1)	V_{IN}	−0.3 to 6	V
FBRTN	V_{FBRTN}	−0.3 to + 0.3 V	V
PWM2 to PWM6, Rampadj		−0.3 to V_{IN} + 0.3	V
SW1 to SW6		−5 to +25 V	V
SW1 to SW6 (<200 ns|)		−10 to +25 V	V
All other Inputs and Outputs		−0.3 to V_{IN} + 0.3	V
Storage Temperature Range	TSTG	−65 to 150	°C
Operating Ambient Temperature Range		0 to 85	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2	kV
ESD Capability, Machine Model (Note 2)	ESD_{MM}	100	V
Moisture Sensitivity Level	MSL	3	–
Lead Temperature Soldering Reflow (SMD Styles Only), Pb−Free Versions (Note 3)	T_{SLD}	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Refer to Electrical Characteristics and Application Information for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latchup Current Maximum Rating: ≤150 mA per JEDEC standard: JESD78
3. For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Characteristics, LFCSP, 7mm * 7mm (Note 1) Thermal Resistance, Junction−to−Air (Note 4) Thermal Resistance, Junction−to−Lead 2 (Note 4)	 $R_{\theta JA}$ $R_{\Psi JL}$	 24 10	°C/W

4. Values based on copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate.

OPERATING RANGES (Note 1)

Characteristic	Symbol	Min	Max	Unit
Output Voltage (Note 5)	V_{OUT}	0.375	1.6	V
Ambient Temperature	T_A	0	85	°C

5. Maximum limit for $V_{OUT} = V_{OUT(NOM)}$ − 10%.

PIN ASSIGNMENT

Pin No.	Pin Name	Description
1	NC	No Connect
2	NC	No Connect
3	NC	No Connect
4	NC	No Connect
5	EN	Power Supply Enable Input. Pulling this pin to GND disables the PWM outputs and pulls the PWRGD output low.
6	GND	Ground. All internal biasing and the logic output signals of the device are referenced to this ground.
7	PSI_SET	This input sets the number of phases enabled during $\overline{\text{PSI}}$. Pulling this input high means that two phases, Phases 1 and Phase 4 (when 6 phases are enabled during normal operation), are enabled during $\overline{\text{PSI}}$. Grounding this pin means only Phase 1 is enabled during $\overline{\text{PSI}}$.
8	LLSET	Output Loadline Programming Input. This pin can be connected directly to CSCOMP or it can be connected to the centerpoint of a resistor divider between CSCOMP and CSREF. Connecting LLSET to CSREF disables the loadline.
9	IMON	Total Current Output Pin.
10	TTSENSE	VR Temperature Sense Input. An NTC thermistor between this pin and GND is used to remotely sense the temperature at the desired thermal monitoring point.
11	VRHOT	VR HOT Output. Open drain output that signals when the temperature at the monitoring point connected to TTSENSE exceeds the VRHOT temperature threshold.
12	IREF	Current Reference Input. An external resistor from this pin to ground sets the reference current for I_{FB}, IILIMFS, and ITH(X).
13	RT	Frequency Setting Resistor Input. An external resistor connected between this pin and GND sets the oscillator frequency of the device.
14	RAMPADJ	PWM Ramp Current Input. An external resistor from the converter input voltage to this pin sets the internal PWM ramp.
15	TRDET	Transient Detect. This output is asserted low whenever a load release is detected
16	FBRTN	Feedback Return. VID DAC and error amplifier reference for remote sensing of the output voltage.
17	COMP	Error Amplifier Output and Compensation Point.
18	FB	Feedback Input. Error amplifier input for remote sensing of the output voltage. An external resistor between this pin and the output voltage sets the no load offset point.
19	CSREF	Current Sense Reference Voltage Input. The voltage on this pin is used as the reference for the current sense amplifier and the power−good and crowbar functions. This pin should be connected to the common point of the output inductors.
20	CSSUM	Current Sense Summing Node. External resistors from each switch node to this pin sum the average inductor currents together to measure the total output current.
21	CSCOMP	Current Sense Compensation Point. A resistor and capacitor from this pin to CSSUM determines the gain of the current sense amplifier and the positioning loop response time.
22	ILIMFS	Current Sense and Limit Scaling Pin. An external resistor from this pin to CSCOMP sets the internal current sensing signal for current−limit and IMON.
23	$\overline{\text{ODN}}$	Output Disable Logic Output for $\overline{\text{PSI}}$ operation. This pin is actively pulled low when $\overline{\text{PSI}}$ is low, otherwise it functions in the same way as $\overline{\text{OD1}}$.
24	$\overline{\text{OD1}}$	Output Disable Logic Output. This pin is actively pulled low when the EN input is low or when V_{CC} is below its UVLO threshold to signal to the Driver IC that the driver high−side and low−side outputs should go low.
25 to 30	SW6 to SW1	Current Balance Inputs. Inputs for measuring the current level in each phase. The SW pins of unused phases should be left open.
31 to 36	PWM6 to PWM1	Logic−Level PWM Outputs. Each output is connected to the input of an external MOSFET driver such as the ADP3121. Connecting PWM6 to V_{CC} disables PWM6, connecting PWM5 to V_{CC} disables PWM5 and PWM6, etc. This means the ADP4100 can be setup to operate as a 1− 2−, 3−, 4−, 5−, or 6−phase controller.
37	V_{CC}	Supply Voltage for the Device. A 340 Ω resistor should be placed between the 12 V system supply and the V_{CC} pin. The internal shunt regulator maintains V_{CC} = 5.0 V.
38 to 45	VID7 to VID0	Voltage Identification DAC Inputs. These eight pins are pulled down to GND, providing a logic zero if left open. When in normal operation mode, the DAC output programs the FB regulation voltage from 0.375 V to 1.6 V.
46	$\overline{\text{PSI}}$	Power State Indicator. Pulling this pin low places the controller in lower power state operation.
47	PWRGD	Power−Good Output. Open−drain output that signals when the output voltage is outside of the proper operating range.
48	VCC3	3.3 V Power Supply Output. A capacitor from this pin to ground provided decoupling for the interval 3.3V LDO.

ELECTRICAL CHARACTERISTICS

V_{in} = (5.0 V) FBRTN − GND, for typical values T_A = 25°C, for min/max values T_A = 0°C to 85°C; unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Reference Current						
Reference Bias Voltage		V_{IREF}	1.75	1.8	1.85	V
Reference Bias Current	R_{IREF} = 121 kΩ	I_{IREF}		15		μA
Error Amplifier						
Output Voltage Range (Note 6)		V_{COMP}	0		4.4	V
Accuracy	Relative to nominal DAC output, referenced to FBRTN (see Figure 4) In startup	V_{FB} $V_{FB(BOOT)}$	7 1.093	 1.1	7 1.107	mV V
Load Line Positioning Accuracy			−77	−80	−83	mV
LLSET Input Voltage Range			−250		250	mV
LLSET Input Bias Current			−10		10	nA
Differential Non−linearity			−1.0		+1.0	LSB
Input Bias Current	R_{IREF} = 121 kΩ	I_{FB}	14.2	16	17.7	μA
FBRTN Current		I_{FBRTN}		100	200	μA
Output Current	FB forced to V_{OUT} −3%	I_{COMP}		500		μA
Gain Bandwidth Product	COMP = FB	$GBW_{(ERR)}$		20		MHz
Slew Rate	COMP = FB			25		V/μs
BOOT Voltage Hold Time	Internal Timer	t_{BOOT}		2.0		ms
VID Inputs						
Input Low Voltage	VID(X)	$V_{IL(VID)}$			0.3	V
Input High Voltage	VID(X)	$V_{IH(VID)}$	0.8			V
Input Current		$I_{IN(VID)}$		−5.0		μA
VID Transition Delay Time (Note 6)	VID code change to FB change		200			ns
No CPU Detection Turn−Off Delay Time (Note 6)	VID code change to PWM going low		5.0			μs
Oscillator						
Frequency Range (Note 6)		f_{OSC}	0.25		9.0	MHz
Frequency Variation	T_A = 25°C, R_T = 270 kΩ, 6−phase T_A = 25°C, R_T = 130 kΩ, 6−phase T_A = 25°C, R_T = 68 kΩ, 6−phase	f_{PHASE}	225	245 500 850	265	kHz
Output Voltage	RT = 500 kΩ to GND	V_{RT}	1.93	2.03	2.13	V
RAMPADJ Output Voltage	RAMPADJ − FB, V_{FB} = 1V, IRAMPADJ = −60 μA	$V_{RAMPADJ}$	−50		+50	mV
RAMPADJ Input Current Range		$I_{RAMPADJ}$	5.0		60	μA
Current Sense Amplifier						
Offset Voltage	CSSUM − CSREF (see Figure 5)	$V_{OS(CSA)}$	−1.0		+1.0	mV
Input Bias Current, CSREF	CSREF = 1.0 V	$I_{BIAS(CSREF)}$	−20		+20	μA
Input Bias Current, CSSUM	CSREF = 1.0 V	$I_{BIAS(CSSUM)}$	−10		+10	nA
Gain Bandwidth Product	CSSUM = CSCOMP	$GBW_{(CSA)}$		10		MHz
Slew Rate	C_{CSCOMP} = 10pF			10		V/μs
Input Common−Mode Range	CSSUM and CSREF		0		3.0	V
Output Voltage Range			0.05		3.0	V
Output Current		I_{CSCOMP}		500		μA
Current−Limit Latchoff Delay time	Internal Timer			8.0		ms

6. Guaranteed by design or bench characterization, not tested in production.

ELECTRICAL CHARACTERISTICS

V_{in} = (5.0 V) FBRTN − GND, for typical values T_A = 25°C, for min/max values T_A = 0°C to 85°C; unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
$\overline{PSI}$						
Input Low Voltage					0.3	V
Input High Voltage			0.8			V
Input Current				−5		μA
Assertion Timing	Fsw = 300kHz			3.3		μs
Deassertion Timing	Fsw = 300kHz			825		ns
TRDET						
Output Low Voltage	I_{OUT} = −6mA	V_{OL}		150	300	mV
IMON						
Clamp Voltage			1.0		1.15	V
Accuracy	10 x (CSREF − CSCOMP)/R_{ILIM}		−3.0		3.0	%
Output Current					800	μA
Offset			−5.5		5.5	mV
Current−Limit Comparator						
I_{LIM} Bias Current	CSREF − CSCOMP)/R_{ILIM}, (CSREF − CSCOMP) = 150 mV, R_{ILIM} = 7.5 kΩ	I_{LIM}		22		μA
Current−Limit Threshold Current	4/3 x I_{IREF}	I_{CL}		22		μA
Current Balance Amplifier						
Common−Mode Range		$V_{SW(X)CM}$	−600		+200	mV
Input Resistance	SW(X) = 0 V	$R_{SW(X)}$	12	18	21	kΩ
Input Current	SW(X) = 0 V	$I_{SW(X)}$	8.0	12	18	μA
Input Current Matching	SW(X) = 0 V	$\Delta I_{SW(X)}$	−6.0		+6.0	%
Delay Timer						
Internal Timer				2.0		ms
Soft−Start						
Internal Timer				0.5		V/ms
DVID Slew Rate						
Internal Timer				12.2		V/ms
Enable Input						
Input Low Voltage		$V_{IL(EN)}$			0.3	V
Input High Voltage		$V_{IH(EN)}$	0.8			V
Input Current		$I_{IN(EN)}$		−1.0		μA
Delay Time	EN > 0.8 V, Internal Delay	$t_{DELAY(EN)}$		2.0		ms
$\overline{ODN}$ and $\overline{OD1}$ Outputs						
Output Low Voltage	$I_{OD(SINK)}$ = −400 μA	$V_{OL(\overline{ODN/1})}$		160	500	mV
Output High Voltage	$I_{OD(SOURCE)}$ = 400 μA	$V_{OL(\overline{ODN/1})}$	4.0	5.0		V
$\overline{ODN}$ / $\overline{OD1}$ Pulldown Resistor				60		kΩ
Power−Good Comparator						
Undervoltage Threshold	Relative to Nominal DAC Output	$V_{PWRGD(UV)}$	−600	−500	−400	mV
Overvoltage Threshold	Relative to DAC Output, PWRGD_Hi = 00	$V_{PWRGD(OV)}$	200	300	400	mV
Output Low Voltage	$I_{PWRGD(SINK)}$ = −4 mA	$V_{OL(PWRGD)}$		150	300	mV

6. Guaranteed by design or bench characterization, not tested in production.

ELECTRICAL CHARACTERISTICS

V_{in} = (5.0 V) FBRTN − GND, for typical values T_A = 25°C, for min/max values T_A = 0°C to 85°C; unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Power Good Delay Time						
During Soft−Start (Note 6)	Internal Timer			2.0		ms
Power−Good Comparator						
VID Code Changing			100	250		μs
VID Code Static				200		ns
Crowbar Trip Point	Relative to DAC Output, PWRGD_Hi = 00	$V_{CROWBAR}$	200	300	400	mV
Crowbar Reset Point	Relative to FBRTN		250	300	350	mV
Crowbar Delay Time	Overvoltage to PWM going low	$t_{CROWBAR}$				
VID Code Changing			100	250		μs
VID Code Static				400		ns
PWM Outputs						
Output Low Voltage	$I_{PWM(SINK)}$ = −400 μA	$V_{OL(PWM)}$		160	500	mV
Output High Voltage	$I_{PWM(SOURCE)}$ = 400 μA	$V_{OH(PWM)}$	4.0	5.0		V
VRHOT Output						
Output Low Voltage	$I_{VRHOT(SINK)}$ = −6 mA	$V_{OL(VRHOT)}$		160	500	mV
Output High Leakage Current	V_{OH} = 5.0 V	$I_{OH(VRHOT)}$			1.0	μA
TTSENSE Inputs						
TTSENSE Voltage Range	Internally Limited		0		2	V
Source Current	R_{IREF} = 121 kΩ	I_{TH}	−110	−125	−140	μA
VRHOT Voltage Threshold			780	810	840	mV
VRHOT Hysteresis				55		mV
VRHOT Output Low Voltage	$I_{VRHOT(SINK)}$ = −4mA			150	300	mV
Supply						
V_{CC} (Note 6)	V_{CC}		4.7	5.25	5.75	V
DC Supply Current (see Figure 2)	V_{SYSTEM} = 13.2 V, R_{SHUNT} = 340 Ω	I_{VCC}		20	25	mA
UVLO Turn−On Current				6.5	11	mA
UVLO Threshold Voltage	V_{CC} Rising	V_{UVLO}	9.5			V
UVLO Turn−Off Voltage	V_{CC} Falling			4.1		V
VCC3 Output Voltage	I_{VCC3} = 1 mA	VCC3	3.0	3.3	3.6	V

6. Guaranteed by design or bench characterization, not tested in production.

TYPICAL CHARACTERISTICS

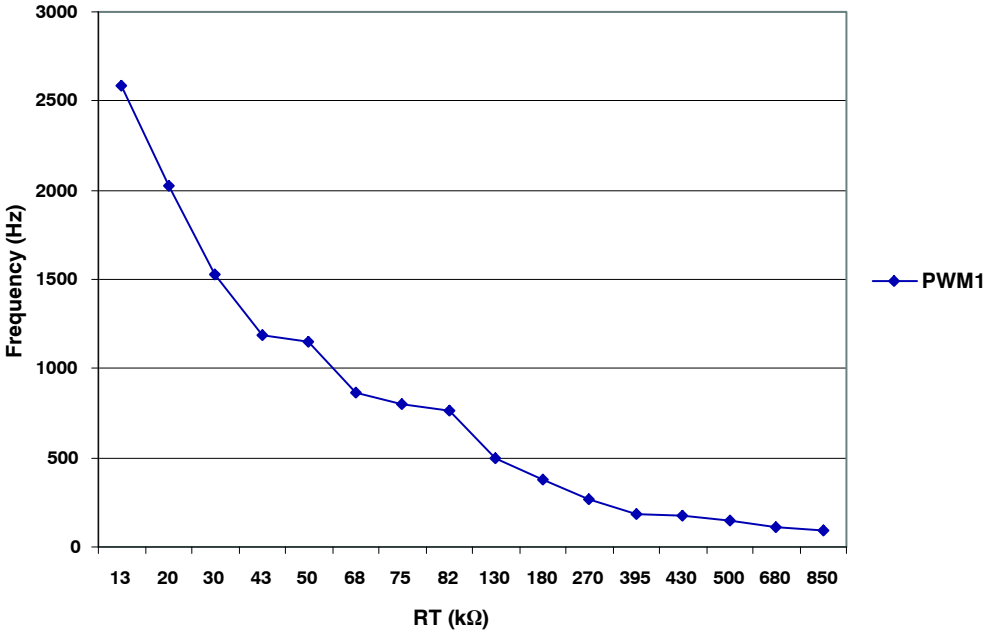


Figure 3. ADP4100 RT vs Frequency

TEST CIRCUITS

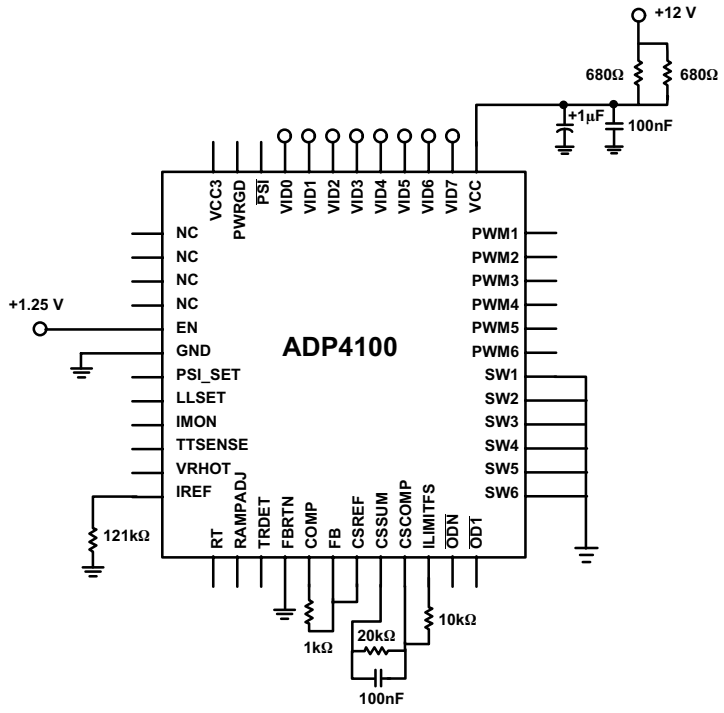


Figure 4. Closed−Loop Output Voltage Accuracy

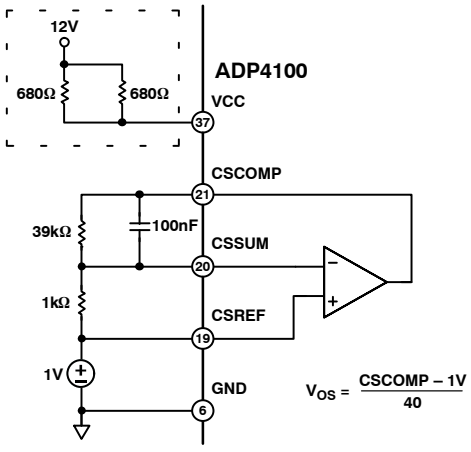


Figure 5. Current Sense Amplifier V_{OS}

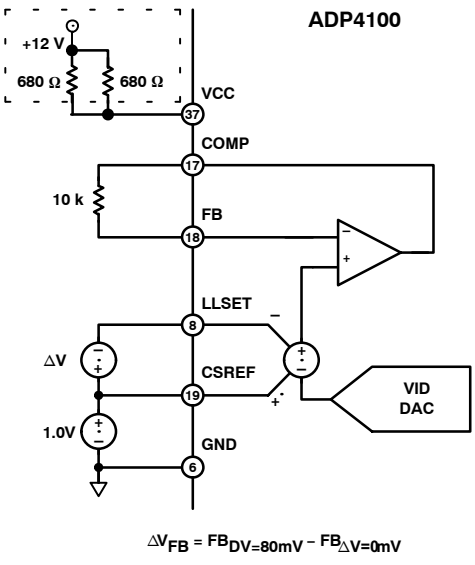


Figure 6. Positioning Accuracy

Theory of Operation

The ADP4100 is a 6−Phase VR11.1 regulator. A typical application circuits is shown in Figure 2.

Startup Sequence

The ADP4100 follows the VR11 startup sequence shown in Figure 7. After both the EN and UVLO conditions are met, an internal timer goes through one delay cycle TD1 (= 2ms). The first six clock cycles of TD2 are blanked from the PWM outputs and used for phase detection as explained in the following section. Then the internal soft−start ramp is enabled (TD2) and the output comes up to the boot voltage of 1.1V. The voltage is held at 1.1V for the 2 ms, also known as the Boot Hold time or TD3. During TD3 the processor VID pins settle to the required VID code. When TD3 is over, the ADP4100 reads the VID inputs and soft−starts either up or down to the final VID voltage (TD4). After TD4 has been completed and the PWRGD masking time (equal to VID on the fly masking) is finished, a third cycle of the internal timer sets the PWRGD blanking (TD5).

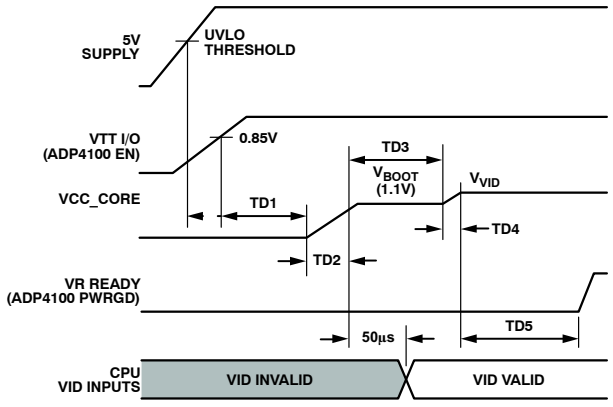


Figure 7. System Startup Sequence for VR11

Figure 8 shows typical startup waveforms for the ADP4100.

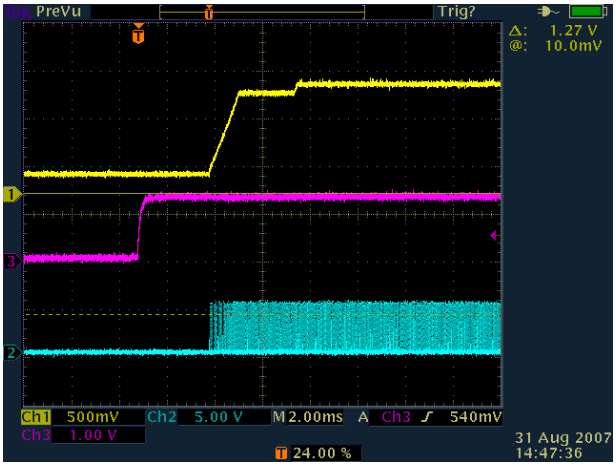


Figure 8. Shows Typical Startup Waveforms for the ADP4100

Figure 8 typical startup waveforms:
Channel 1: CSREF
Channel 2: PWM1
Channel 3 : Enable

Phase Detection

During startup, the number of operational phases and their phase relationship is determined by the internal circuitry that monitors the PWM outputs. Normally, the ADP4100 operates as a 6−Phase PWM controller.

To operate as a 5−Phase Controller connect PWM6 to V_{CC}.

To operate as a 4−Phase Controller connect PWM5 and PWM6 to V_{CC}.

To operate as a 3−Phase Controller connect PWM4, PWM5 and PWM6 to V_{CC}.

To operate as a 2−Phase Controller connect PWM3, PWM4, PWM5 and PWM6 to V_{CC}.

To operate as a single phase controller connect PMW2, PWM3, PWM4, PWM5 and PWM6 to V_{CC}.

Prior to soft−start, while EN is high the PWM6, PWM5, PWM4 PWM3 and PWM2 pins sink approximately 100 µA each. An internal comparator checks each pin's voltage vs. a threshold of 3.0 V. If the pin is tied to V_{CC}, it is above the threshold. Otherwise, an internal current sink pulls the pin to GND, which is below the threshold. PWM1 is low during the phase detection interval that occurs during the first six clock cycles of TD2. After this time, if the remaining PWM outputs are not pulled to V_{CC}, the 100 µA current sink is removed, and they function as normal PWM outputs. If they are pulled to V_{CC}, the 100 µA current source is removed, and the outputs are put into a high impedance state.

The PWM outputs are logic−level devices intended for driving fast response external gate drivers such as the ADP3121. Because each phase is monitored independently, operation approaching 100% duty cycle is possible. In addition, more than one output can be on at the same time to allow overlapping phases.

Master Clock Frequency

The clock frequency of the ADP4100 is set with an external resistor connected from the RT pin to ground. The frequency follows the graph in Figure 3. To determine the frequency per phase, the clock is divided by the number of phases in use. If all phases are in use, divide by 6. If 4 phases are in use then divide by 4.

$$R_T = \frac{1}{n \times f_{sw} \times C_r} - R_{TO} \qquad \text{(eq. 1)}$$

Where: CT = 2.2 pF and RTO = 21 K

Output Voltage Differential Sensing

The ADP4100 combines differential sensing with a high accuracy VID DAC and reference, and a low offset error amplifier. This maintains a worst−case specification of ±7 mV differential sensing error over its full operating output voltage and temperature range. The output voltage is sensed between the FB pin and FBRTN pin. FB is connected

through a resistor, R_B, to the regulation point, usually the remote sense pin of the microprocessor. FBRTN is connected directly to the remote sense ground point. The internal VID DAC and precision reference are referenced to FBRTN, which has a minimal current of 100 μA to allow accurate remote sensing. The internal error amplifier compares the output of the DAC to the FB pin to regulate the output voltage.

Output Current Sensing

The ADP4100 provides a dedicated Current−Sense Amplifier (CSA) to monitor the total output current for proper voltage positioning vs. load current, for the IMON output and for current−limit detection. Sensing the load current at the output gives the total real time current being delivered to the load, which is an inherently more accurate method than peak current detection or sampling the current across a sense element such as the low−side MOSFET. This amplifier can be configured several ways, depending on the objectives of the system, as follows:

- Output inductor DCR sensing without a thermistor for lowest cost.
- Output inductor DCR sensing with a thermistor for improved accuracy with tracking of inductor temperature.
- Sense resistors for highest accuracy measurements.

The positive input of the CSA is connected to the CSREF pin, which is connected to the average output voltage. The inputs to the amplifier are summed together through resistors from the sensing element, such as the switch node side of the output inductors, to the inverting input CSSUM. The feedback resistor between CSCOMP and CSSUM sets the gain of the amplifier and a filter capacitor is placed in parallel with this resistor. The gain of the amplifier is programmable by adjusting the feedback resistor. This difference signal is used internally to offset the VID DAC for voltage positioning.

The difference between CSREF and CSCOMP is used as a differential input for the current−limit comparator.

To provide the best accuracy for sensing current, the CSA is designed to have a low offset input voltage. Also, the sensing gain is determined by external resistors to make it extremely accurate.

Current−Limit Setpoint

The current limit threshold on the ADP4100 is programmed by a resistor between the I_{LIMFS} pin and the CSCOMP pin. The I_{LIMFS} current, I_{ILIMFS}, is compared with an internal current reference of 22 μA. If I_{ILIMFS} exceeds 22 μA then the output current has exceeded the limit and the current limit protection is tripped.

$$I_{ILIMFS} = \frac{V_{ILIMFS} - V_{CSCOMP}}{R_{ILIMFS}} \quad \text{(eq. 2)}$$

Where: $V_{ILIMFS} = V_{CSREF}$

$$I_{ILIMFS} = \frac{V_{CSREF} - V_{CSCOMP}}{R_{ILIMFS}} \quad \text{(eq. 3)}$$

$$V_{CSREF} - V_{CSCOMP} = \frac{R_{CS}}{R_{PH}} \times R_L \times I_{LOAD}$$

Where: R_L = DCR of the Inductor

Assuming that:

$$\frac{R_{CS}}{R_{PH}} \times R_L = 1\ m\Omega \quad \text{(eq. 4)}$$

i.e. the external circuit is set up for a 1 mΩ Loadline then the R_{ILIMFS} is calculated as follows:

$$I_{ILIMFS} = \frac{1\ m\Omega \times I_{LOAD}}{R_{LIMITS}} \quad \text{(eq. 5)}$$

Assuming we want a current limit of 150 A that means that I_{LIMFS} must equal 22 μA at that load.

$$22\ \mu A = \frac{1\ m\Omega \times 150\ A}{R_{LIMITFS}} \quad \text{(eq. 6)}$$

Solving this equation for $R_{LIMITFS}$ we get 6.8 kΩ. Closest 1% resistor is 6.81 kΩ.

Current−Limit, Short−Circuit and Latchoff Protection

If the current limit is reached and TD5 has completed, an internal latchoff delay time will start, and the controller will shut down if the fault is not removed. This delay is four times longer than the delay time during the startup sequence. The current limit delay time only starts after the TD5 has completed. If there is a current limit during startup, the ADP4100 will go through TD1 to TD5, and then start the latchoff time. Because the controller continues to cycle the phases during the latchoff delay time, if the short is removed before the timer is complete, the controller can return to normal operation.

The latchoff function can be reset by either removing and reapplying the supply voltage to the ADP4100, or by toggling the EN pin low for a short time.

During startup when the output voltage is below 200 mV, a secondary current limit is active. This is necessary because the voltage swing of CSCOMP cannot go below ground. This secondary current limit limits the internal COMP voltage to the PWM comparators to 1.5 V. This limits the voltage drop across the low−side MOSFETs through the current balance circuitry. Typical overcurrent latchoff waveforms are shown in Figure 9).

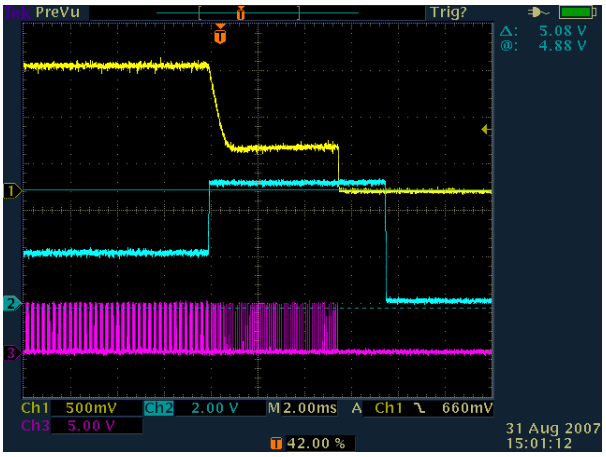


Figure 9. Overcurrent Latchoff Waveforms Channel 1: CSREF, Channel 2: COMP, Channel 3: PWM1

An inherent per phase current limit protects individual phases if one or more phases stops functioning because of a faulty component. This limit is based on the maximum normal mode COMP voltage.

Output Current Monitor

IMON is an analog output from the ADP4100 representing the total current being delivered to the load. It outputs an accurate current that is directly proportional to the current set by the ILIMFS resistor.

$$I_{IMON} = 10 \times I_{SW} \times I_{LIMFS} \quad \text{(eq. 7)}$$

The current is then run through a parallel RC connected from the I_{MON} pin to the FBRTN pin to generate an accurately scaled and filtered voltage as per the VR11.1 specification. The size of the resistor is used to set the I_{MON} scaling.

The scaling is set such that I_{MON} = 900 mV at the TDC current of the processor. This means that the RIMON resistor should be chosen as follows.

From the Current−Limit Setpoint paragraph we know the following:

$$I_{ILIMFS} = \frac{1\ m\Omega \times I_{LOAD}}{R_{LIMFS}} \quad \text{(eq. 8)}$$

$$I_{IMON} = 10 \times \frac{1\ m\Omega \times I_{LOAD}}{R_{LIMFS}}$$

For a 150 A current limit R_{LIMFS} = 6.81 kΩ. Assuming the TDC = 135 A then V_{MON} should equal 900 mV when I_{LOAD} = 135 A.

When I_{LOAD} = 135 A, I_{MON} equals:

$$I_{MON} = 10 \times \frac{1\ m\Omega \times 135\ A}{6.81\ k\Omega} = 198\mu A \quad \text{(eq. 9)}$$

$$V_{IMON} = 900\ mV = 198\ \mu A \times R_{MON}$$

This gives a value of 4.54 kΩ for RMON.

If the TDC and OCP limit for the processor have to be changed then it may be necessary to change the ILIMITFS resistor only. This is because the ILIMITFS resistor sets up both the current limit and also the current out of the IMON pin, as explained earlier.

The I_{MON} pin also includes an active clamp to limit the IMON voltage to 1.15 V MAX while maintaining accuracy at 900 mV full scale.

Active Impedance Control Mode

For controlling the dynamic output voltage droop as a function of output current, the CSA gain and load line programming can be scaled to be equal to the droop impedance of the regulator times the output current. This droop voltage is then used to set the input control voltage to the system. The droop voltage is subtracted from the DAC reference input voltage directly to tell the error amplifier where the output voltage should be. This allows enhanced feed−forward response.

Load Line Setting

For load line values greater than 1 mΩ, R_{CSA} can be set equal to R_O, and the LLSET pin can be directly connected to the CSCOMP pin. When the load line value needs to be less than 1 mΩ, two additional resistors are required. Figure 10 shows the placement of these resistors.

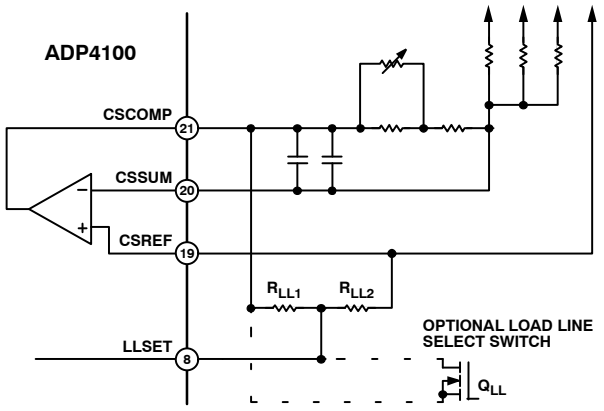


Figure 10. Load Line Setting Resistors

The two resistors R_{LL1} and R_{LL2} set up a divider between the CSCOMP pin and CSREF pin. This resistor divider is input into the LLSET pin to set the load line slope R_O of the V_R according to the following equation:

$$R_O = \frac{R_{LL2}}{R_{LL1} + R_{LL2}} \times R_{CSA} \quad \text{(eq. 10)}$$

The resistor values for R_{LL1} and R_{LL2} are limited by two factors.

- The minimum value is based upon the loading of the CSCOMP pin. This pin's drive capability is 500 μA and the majority of this should be allocated to the CSA feedback. If the current through R_{LL1} and R_{LL2} is limited to 10% of this (50 μA), the following limit can be placed for the minimum value for R_{LL1} and R_{LL2}:

$$R_{LL1} + R_{LL2} \geq \frac{I_{LIM} \times R_{CSA}}{50 \times 10^{-6}} \quad \text{(eq. 11)}$$

Here, I_{LIM} is the current−limit current, which is the maximum signal level that the CSA responds to.

- The maximum value is based upon minimizing induced dc offset errors based on the bias current of the LLSET pin. To keep the induced dc error less than 1 mV, which makes this error statistically negligible, place the following limit of the parallel combination of R_{LL1} and R_{LL2}:

It is best to select the resistor values to minimize their values to reduce the noise and parasitic susceptibility of the feedback path.

$$\frac{R_{LL1} \times R_{LL2}}{R_{LL1} + R_{LL2}} \leq \frac{1 \times 10^{-3}}{120 \times 10^{-9}} = 8.33\ k\Omega \quad \text{(eq. 12)}$$

By combining Equation 10 with Equation 12 and selecting minimum values for the resistors, the following equations result:

$$R_{LL2} = \frac{I_{LIM} \times R_O}{50\ \mu A} \quad \text{(eq. 13)}$$

$$R_{LL1} = \left(\frac{R_{CSA}}{R_O} - 1\right) \times R_{LL2} \quad \text{(eq. 14)}$$

Therefore, both R_{LL1} and R_{LL2} need to be in parallel and less than 8.33 kΩ.

Another useful feature for some VR applications is the ability to select different load lines. Figure 10 shows an optional MOSFET switch that allows this feature. Here, design for $R_{CSA} = R_{O(MAX)}$ (selected with Q_{LL} on) and then use Equation 10 to set $R_O = R_{O(MIN)}$ (selected with Q_{LL} off).

For this design, $R_{CSA} = R_O = 1\ m\Omega$. As a result, connect LLSET directly to CSCOMP; the R_{LL1}.

Current Control Mode and Thermal Balance

The ADP4100 has individual inputs (SW1 to SW6) for each phase that are used for monitoring the current of each phase. This information is combined with an internal ramp to create a current balancing feedback system that has been optimized for initial current balance accuracy and dynamic thermal balancing during operation. This current balance information is independent of the average output current information used for positioning.

The magnitude of the internal ramp can be set to optimize the transient response of the system. It also monitors the supply voltage for feed−forward control for changes in the supply. A resistor connected from the power input voltage to the RAMPADJ pin determines the slope of the internal PWM ramp.

Voltage Control Mode

A high gain, high bandwidth, voltage mode error amplifier is used for the voltage mode control loop. The control input voltage to the positive input is set via the VID logic according to the voltages listed in VID Code Table. The VID code is set using the VID Input pins.

This voltage is also offset by the droop voltage for active positioning of the output voltage as a function of current, commonly known as active voltage positioning. The output of the amplifier is the COMP pin, which sets the termination voltage for the internal PWM ramps.

The negative input (FB) is tied to the output sense location with Resistor R_B and is used for sensing and controlling the output voltage at this point. A current source (equal to 16 μA) from the FB pin flowing through R_B is used for setting the no load offset voltage from the VID voltage. The no load voltage is negative with respect to the VID DAC for Intel CPU's.

The value of R_B can be found using the following equation:

$$R_B = \frac{V_{VID} - V_{ONL}}{I_{FB}} \quad \text{(eq. 15)}$$

RAMPADJ Input Current

The resistor connected to the Rampadj pin sets the internal PWM ramp. The value for this resistor is chosen to provide the combination of thermal balance, stability and transient response.

$$R_R = \frac{A_R \times L}{3 \times A_D \times R_{DS} \times C_R} \quad \text{(eq. 16)}$$

Where
A_R is the internal ramp amplifier gain (= 0.5)
A_D is the current balancing amplifier gain (= 5)
R_{DS} is the total low side MOSFET on resistance
C_R is the internal ramp capacitor value (= 5pF).

The internal ramp voltage can be calculated as follows:

$$V_R = \frac{A_R \times (1 - D) \times V_{VID}}{R_R \times C_R \times f_{SW}} \quad \text{(eq. 17)}$$

The size of the internal ramp can be made larger or smaller. If it is made larger, stability and noise rejection improves but the transient performance decreases. If the ramp is made smaller then the transient response improves however noise rejection and stability degrades.

COMP Pin Ramp

There is a ramp signal on the COMP signal, which is due to the droop voltage and the output voltage ramps. This ramp adds to the internal ramp to produce the following ramp signal at the PWM input.

$$V_{RT} = \frac{V_R}{\left(1 - \frac{2 \times (1 - n \times D)}{n \times f_{SW} \times C_X \times R_O}\right)} \quad \text{(eq. 18)}$$

Where Cx = bulk capacitance
R_O = Droop
n = number of phases
f_{SW} = switching frequency per phase
D = duty cycle
V_R = Internal Ramp Voltage (calculated in Rampadj section of this data sheet)

This ramp voltage should be set to at least 0.5 V for noise immunity reasons. If it is less than 0.5 V then decrease the ramp resistor.

Dynamic VID

The ADP4100 has the ability to respond to dynamically changing VID inputs while the controller is running. This allows the output voltage to change while the supply is running and supplying current to the load. This is commonly referred to as Dynamic VID (DVID). A DVID can occur under either light or heavy load conditions. The processor signals the controller by changing the VID inputs in a single or multiple steps from the start code to the finish code. This change can be positive or negative.

When a VID bit changes state, the ADP4100 detects the change and ignores the DAC inputs for a minimum of 200 ns. This time prevents a false code due to logic skew while the VID inputs are changing. Additionally, the first VID change initiates the PWRGD and CROWBAR blanking functions for a minimum of 100 μs to prevent a false PWRGD or CROWBAR event. Each VID change resets the internal timer.

If a VID off code is detected the ADP4100 will wait for 5 μsec to ensure that the code is correct before initiating a shutdown of the controller.

Enhanced Transients Mode

The ADP4100 incorporates enhanced transient response for both load step up and load release. For load step up it senses the output of the error amp to determine if a load step up has occurred and then sequences on the appropriate number of phases to ramp up the output current.

For load release, it also senses the output of the error amp and uses the load release information to trigger the TRDET pin, which is then used to adjust the error amp feedback for optimal positioning. This is especially important during high frequency load steps.

Additional information is used during load transients to ensure proper sequencing and balancing of phases during high frequency load steps as well as minimizing the stress on components such as the input filter and MOSFETs.

TRDET and Phase Shuffling

The ADP4100 senses the error amp output and triggers the TRDET pin when a load release takes place. The TRDET circuit, as shown in Figure 2, adjusts the feedback for optimal positioning especially during high frequency load steps. TRDET is also used to trigger phase shuffling. If repeated transients take place at the switching frequency then its possible for one phase to carry most of the currrent. To prevent this from happening the ADP4100 will shuffle the phases whenever a load release happens, i.e. it will randomize the phase sequence.

Reference Current

The IREF pin is used to set an internal current reference. This reference current sets I_{FB} and $I_{TTSENSE}$. A resistor to ground programs the current based on the 1.8 V output.

$$I_{REF} = \frac{1.8\ V}{R_{IREF}} \qquad \text{(eq. 19)}$$

Typically, R_{IREF} is set to 121 kΩ to program IREF = 15 μA. The following currents are then equal to:

$$I_{FB} = I_{REF} = 15\ \mu A$$

$$I_{TTSENSE} = -8\ (I_{IREF}) = -120\ \mu A \qquad \text{(eq. 20)}$$

Power Good Monitoring

The power good comparator monitors the output voltage via the CSREF pin. The PWRGD pin is an open−drain output whose high level (when connected to a pullup resistor) indicates that the output voltage is within the nominal limits specified in the specifications above based on the VID voltage setting. PWRGD goes low if the output voltage is outside of this specified range, if the VID DAC inputs are in no CPU mode, or whenever the EN pin is pulled low. PWRGD is blanked during a DVID event for a period of 100 μs to prevent false signals during the time the output is charging.

The PWRGD circuitry also incorporates an initial turn−on delay time (TD5). Prior to the SS voltage reaching the programmed VID DAC voltage and the PWRGD masking time finishing, the PWRGD pin is held low. Once the SS circuit reaches the programmed DAC voltage, the internal timer operates.

The range for the PWRGD comparator is +300 mV and −500 mV.

Power State Indicator

The $\overline{\text{PSI}}$ pin is an input used to determine the operating state of the load. If this input is pulled low, the load is in a low power state and the controller asserts the $\overline{\text{ODN}}$ pin low, which can be used to disable phases and maintain better efficiency at lighter loads.

The sequencing into and out of low power operation is maintained to minimize output deviations as well as providing full power load transients immediately after exiting a low power state.

The user can program if one or two phases are enabled during $\overline{\text{PSI}}$ using the PSI_SET pin. If this pin is pulled low then 1 phase is enabled (always phase 1). If it is pulled high then two phases are enabled (phase 1 and phase 4 in a 6−phase or 5−phase system, phase 1 and phase 3 in a 4−phase system. Extreme care should be taken to ensure that $\overline{\text{ODI}}$ is connected to all phases enabled during $\overline{\text{PSI}}$.

$\overline{\text{PSI}}$ Set Table

# of Phases Normally	$\overline{\text{PSI}}$ Set	Phases on During $\overline{\text{PSI}}$
6	High Low	Phase 1 and 4 Phase 1
5	High Low	Phase 1 and 4 Phase 1
4	High Low	Phase 1 and 3 Phase 1
3	High Low	Phase 1 Phase 1
2	High Low	Phase 1 Phase 1
1	High Low	Phase 1 Phase 1

Output Crowbar

As part of the protection for the load and output components of the supply, the PWM outputs are driven low (turning on the low−side MOSFETs) when the output voltage exceeds the upper crowbar threshold. This crowbar action stops once the output voltage falls below the release threshold of approximately 300 mV.

The value for the crowbar limit follows the PWRGD high limit.

Turning on the low−side MOSFETs pulls down the output as the reverse current builds up in the inductors. If the output overvoltage is due to a short in the high−side MOSFET, this action current−limits the input supply or blows its fuse, protecting the microprocessor from being destroyed.

Output Enable and UVLO

For the ADP4100 to begin switching, the input supply current to the controller must be higher than the UVLO threshold and the EN pin must be higher than its 0.8 V threshold. This initiates a system startup sequence. If either UVLO or EN is less than their respective thresholds, the ADP4100 is disabled. This holds the PWM outputs at ground and forces PWRGD, $\overline{\text{ODN}}$ and $\overline{\text{OD1}}$ signals low.

In the application circuit (see Figure 2), the $\overline{\text{OD1}}$ pin should be connected to the $\overline{\text{OD}}$ inputs of the external drivers for the phases that are always on. The $\overline{\text{ODN}}$ pin should be connected to the $\overline{\text{OD}}$ inputs of the external drivers on the phases that are shutdown during low power operation. Grounding the driver $\overline{\text{OD}}$ inputs disables the drivers such that both DRVH and DRVL are grounded. This feature is important in preventing the discharge of the output capacitors when the controller is shut off. If the driver outputs are not disabled, a negative voltage can be generated during output due to the high current discharge of the output capacitors through the inductors.

Thermal Monitoring

The ADP4100 includes a thermal monitoring channel using a thermistor.

The VR thermal monitoring circuits require an NTC thermistor to be placed from TTSENSE to GND. For best accuracy, the thermistors can be linearized using resistors. A fixed current of 8 times I_{REF} (normally giving 120 μA) is sourced out of the TTSENSE pin into the thermistor. The resulting voltage is compared with the VRHOT Threshold (0.81 V). When the meaured voltage goes below the threshold (i.e. using this thermistor and resistor combination, when the temperature has exceeded approximately 85 °C) the VRHOT signal asserts high. VRHOT is low when the temperature is below the limit (i.e. the volatge is higher than the threshold).

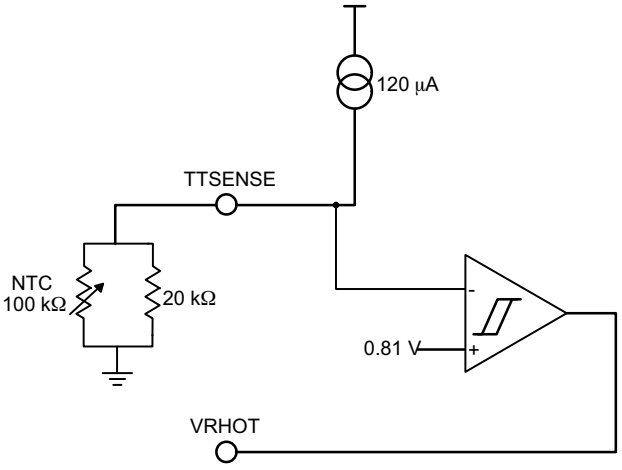


Figure 11. TTSENSE Diagram

Shunt Resistor

The ADP4100 uses a shunt to generate 5.0 V from the 12 V supply range. A trade−off can be made between the power dissipated in the shunt resistor and the UVLO threshold. Figure 12 shows the typical resistor value needed to realize certain UVLO voltages. It also gives the maximum power dissipated in the shunt resistor for these UVLO voltages.

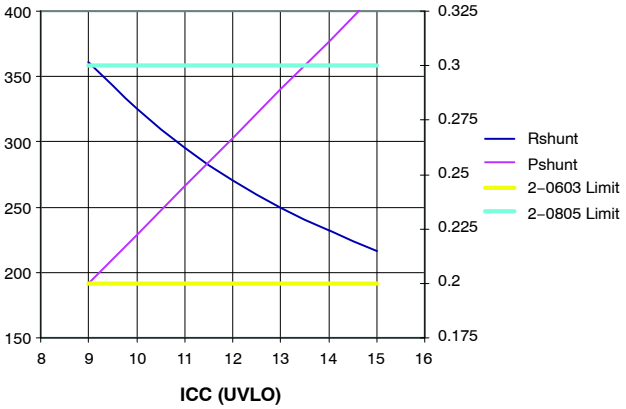


Figure 12. Typical Shunt Resistor Value and Power Dissipation for Different UVLO Voltage

The maximum power dissipated is calculated using Equation 21.

$$P_{MAX} = \frac{\left(V_{IN(MAX)} - V_{CC(MIN)}\right)^2}{R_{SHUNT}} \quad \text{(eq. 21)}$$

where:

$V_{IN(MAX)}$ is the maximum voltage from the 12 V input supply (if the 12 V input supply is 12 V ± 5%, $V_{IN(MAX)}$ = 12.6 V; if the 12 V input supply is 12 V ± 10%, $V_{IN(MAX)}$ = 13.2 V).

$V_{CC(MIN)}$ is the minimum V_{CC} voltage of the ADP4100. This is specified as 4.7 V.

R_{SHUNT} is the shunt resistor value.

The CECC standard specification for power rating in surface−mount resistors is: 0603 = 0.1 W, 0805 = 0.125 W, 1206 = 0.25 W.

VCC3

The ADP4100 has an internal 3.3 V LDO to supply the internal circuits on the ADP4100. A 1 μF X7R capacitor should be placed between this pin and AGND. This should not be loaded by an external circuitry.

Driver Connections

Each driver in the external circuit is connected to one PWM signal from the controller. The PWM signal controls when the driver turns on and off both the high and low side FET's.

Each driver is also connected to either the $\overline{OD1}$ or $\overline{ODN}$ signal from the controller. This signal is used to disable the driver, i.e. both high side and low side FET's are disabled. Drivers are disabled when $\overline{OD}$ pins are low and switching when the $\overline{OD}$ pin is high. Phases which are enabled during PSI should be connected to $\overline{OD1}$. Phases which are disabled during PSI should be connected to $\overline{ODN}$. Extreme care should be taken to ensure that the controller configuration (set by the PSI_Set pin) matches the $\overline{OD1}$ and $\overline{ODN}$ connections on the board.

VID Inputs

The ADP4100 has seven VID Input pins which are used to set the target output voltage. The VID codes are decoded using the following VR11.1 Table. An input voltage of less than 0.3 V is decoded as logic low. An input voltage of greater than 0.8 V is decoded as logic high. If the pins are left open then an internal pulldown will pull the pin low.

VR11 VID CODES for the ADP4100

OUTPUT	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
OFF	0	0	0	0	0	0	0	0
OFF	0	0	0	0	0	0	0	1
1.60000	0	0	0	0	0	0	1	0
1.59375	0	0	0	0	0	0	1	1
1.58750	0	0	0	0	0	1	0	0
1.58125	0	0	0	0	0	1	0	1
1.57500	0	0	0	0	0	1	1	0
1.56875	0	0	0	0	0	1	1	1
1.56250	0	0	0	0	1	0	0	0
1.55625	0	0	0	0	1	0	0	1
1.55000	0	0	0	0	1	0	1	0
1.54375	0	0	0	0	1	0	1	1
1.53750	0	0	0	0	1	1	0	0
1.53125	0	0	0	0	1	1	0	1
1.52500	0	0	0	0	1	1	1	0
1.51875	0	0	0	0	1	1	1	1
1.51250	0	0	0	1	0	0	0	0
1.50625	0	0	0	1	0	0	0	1
1.50000	0	0	0	1	0	0	1	0
1.49375	0	0	0	1	0	0	1	1
1.48750	0	0	0	1	0	1	0	0
1.48125	0	0	0	1	0	1	0	1
1.47500	0	0	0	1	0	1	1	0
1.46875	0	0	0	1	0	1	1	1
1.46250	0	0	0	1	1	0	0	0
1.45625	0	0	0	1	1	0	0	1
1.45000	0	0	0	1	1	0	1	0
1.44375	0	0	0	1	1	0	1	1
1.43750	0	0	0	1	1	1	0	0
1.43125	0	0	0	1	1	1	0	1
1.42500	0	0	0	1	1	1	1	0
1.41875	0	0	0	1	1	1	1	1
1.41250	0	0	1	0	0	0	0	0
1.40625	0	0	1	0	0	0	0	1
1.40000	0	0	1	0	0	0	1	0
1.39375	0	0	1	0	0	0	1	1
1.38750	0	0	1	0	0	1	0	0
1.38125	0	0	1	0	0	1	0	1
1.37500	0	0	1	0	0	1	1	0
1.36875	0	0	1	0	0	1	1	1
1.36250	0	0	1	0	1	0	0	0
1.35625	0	0	1	0	1	0	0	1
1.35000	0	0	1	0	1	0	1	0
1.34375	0	0	1	0	1	0	1	1
1.33750	0	0	1	0	1	1	0	0
1.33125	0	0	1	0	1	1	0	1

VR11 VID CODES for the ADP4100

OUTPUT	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
1.32500	0	0	1	0	1	1	1	0
1.31875	0	0	1	0	1	1	1	1
1.31250	0	0	1	1	0	0	0	0
1.30625	0	0	1	1	0	0	0	1
1.30000	0	0	1	1	0	0	1	0
1.29375	0	0	1	1	0	0	1	1
1.28750	0	0	1	1	0	1	0	0
1.28125	0	0	1	1	0	1	0	1
1.27500	0	0	1	1	0	1	1	0
1.26875	0	0	1	1	0	1	1	1
1.26250	0	0	1	1	1	0	0	0
1.25625	0	0	1	1	1	0	0	1
1.25000	0	0	1	1	1	0	1	0
1.24375	0	0	1	1	1	0	1	1
1.23750	0	0	1	1	1	1	0	0
1.23125	0	0	1	1	1	1	0	1
1.22500	0	0	1	1	1	1	1	0
1.21875	0	0	1	1	1	1	1	1
1.21250	0	1	0	0	0	0	0	0
1.20625	0	1	0	0	0	0	0	1
1.20000	0	1	0	0	0	0	1	0
1.19375	0	1	0	0	0	0	1	1
1.18750	0	1	0	0	0	1	0	0
1.18125	0	1	0	0	0	1	0	1
1.17500	0	1	0	0	0	1	1	0
1.16875	0	1	0	0	0	1	1	1
1.16250	0	1	0	0	1	0	0	0
1.15625	0	1	0	0	1	0	0	1
1.15000	0	1	0	0	1	0	1	0
1.14375	0	1	0	0	1	0	1	1
1.13750	0	1	0	0	1	1	0	0
1.13125	0	1	0	0	1	1	0	1
1.12500	0	1	0	0	1	1	1	0
1.11875	0	1	0	0	1	1	1	1
1.11250	0	1	0	1	0	0	0	0
1.10625	0	1	0	1	0	0	0	1
1.10000	0	1	0	1	0	0	1	0
1.09375	0	1	0	1	0	0	1	1
1.08750	0	1	0	1	0	1	0	0
1.08125	0	1	0	1	0	1	0	1
1.07500	0	1	0	1	0	1	1	0
1.06875	0	1	0	1	0	1	1	1
1.06250	0	1	0	1	1	0	0	0
1.05625	0	1	0	1	1	0	0	1
1.05000	0	1	0	1	1	0	1	0
1.04375	0	1	0	1	1	0	1	1

VR11 VID CODES for the ADP4100

OUTPUT	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
1.03750	0	1	0	1	1	1	0	0
1.03125	0	1	0	1	1	1	0	1
1.02500	0	1	0	1	1	1	1	0
1.01875	0	1	0	1	1	1	1	1
1.01250	0	1	1	0	0	0	0	0
1.00625	0	1	1	0	0	0	0	1
1.00000	0	1	1	0	0	0	1	0
0.99375	0	1	1	0	0	0	1	1
0.98750	0	1	1	0	0	1	0	0
0.98125	0	1	1	0	0	1	0	1
0.97500	0	1	1	0	0	1	1	0
0.96875	0	1	1	0	0	1	1	1
0.96250	0	1	1	0	1	0	0	0
0.95625	0	1	1	0	1	0	0	1
0.95000	0	1	1	0	1	0	1	0
0.94375	0	1	1	0	1	0	1	1
0.93750	0	1	1	0	1	1	0	0
0.93125	0	1	1	0	1	1	0	1
0.92500	0	1	1	0	1	1	1	0
0.91875	0	1	1	0	1	1	1	1
0.91250	0	1	1	1	0	0	0	0
0.90625	0	1	1	1	0	0	0	1
0.90000	0	1	1	1	0	0	1	0
0.89375	0	1	1	1	0	0	1	1
0.88750	0	1	1	1	0	1	0	0
0.88125	0	1	1	1	0	1	0	1
0.87500	0	1	1	1	0	1	1	0
0.86875	0	1	1	1	0	1	1	1
0.86250	0	1	1	1	1	0	0	0
0.85625	0	1	1	1	1	0	0	1
0.85000	0	1	1	1	1	0	1	0
0.84375	0	1	1	1	1	0	1	1
0.83750	0	1	1	1	1	1	0	0
0.83125	0	1	1	1	1	1	0	1
0.82500	0	1	1	1	1	1	1	0
0.81875	0	1	1	1	1	1	1	1
0.81250	1	0	0	0	0	0	0	0
0.80625	1	0	0	0	0	0	0	1
0.80000	1	0	0	0	0	0	1	0
0.79375	1	0	0	0	0	0	1	1
0.78750	1	0	0	0	0	1	0	0
0.78125	1	0	0	0	0	1	0	1
0.77500	1	0	0	0	0	1	1	0
0.76875	1	0	0	0	0	1	1	1
0.76250	1	0	0	0	1	0	0	0
0.75625	1	0	0	0	1	0	0	1

VR11 VID CODES for the ADP4100

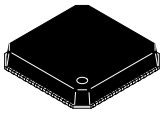
OUTPUT	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
0.75000	1	0	0	0	1	0	1	0
0.74375	1	0	0	0	1	0	1	1
0.73750	1	0	0	0	1	1	0	0
0.73125	1	0	0	0	1	1	0	1
0.72500	1	0	0	0	1	1	1	0
0.71875	1	0	0	0	1	1	1	1
0.71250	1	0	0	1	0	0	0	0
0.70625	1	0	0	1	0	0	0	1
0.70000	1	0	0	1	0	0	1	0
0.69375	1	0	0	1	0	0	1	1
0.68750	1	0	0	1	0	1	0	0
0.68125	1	0	0	1	0	1	0	1
0.67500	1	0	0	1	0	1	1	0
0.66875	1	0	0	1	0	1	1	1
0.66250	1	0	0	1	1	0	0	0
0.65625	1	0	0	1	1	0	0	1
0.65000	1	0	0	1	1	0	1	0
0.64375	1	0	0	1	1	0	1	1
0.63750	1	0	0	1	1	1	0	0
0.63125	1	0	0	1	1	1	0	1
0.62500	1	0	0	1	1	1	1	0
0.61875	1	0	0	1	1	1	1	1
0.61250	1	0	1	0	0	0	0	0
0.60625	1	0	1	0	0	0	0	1
0.60000	1	0	1	0	0	0	1	0
0.59375	1	0	1	0	0	0	1	1
0.58750	1	0	1	0	0	1	0	0
0.58125	1	0	1	0	0	1	0	1
0.57500	1	0	1	0	0	1	1	0
0.56875	1	0	1	0	0	1	1	1
0.56250	1	0	1	0	1	0	0	0
0.55625	1	0	1	0	1	0	0	1
0.55000	1	0	1	0	1	0	1	0
0.54375	1	0	1	0	1	0	1	1
0.53750	1	0	1	0	1	1	0	0
0.53125	1	0	1	0	1	1	0	1
0.52500	1	0	1	0	1	1	1	0
0.51875	1	0	1	0	1	1	1	1
0.51250	1	0	1	1	0	0	0	0
0.50625	1	0	1	1	0	0	0	1
0.50000	1	0	1	1	0	0	1	0
OFF	1	1	1	1	1	1	1	0
OFF	1	1	1	1	1	1	1	1

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

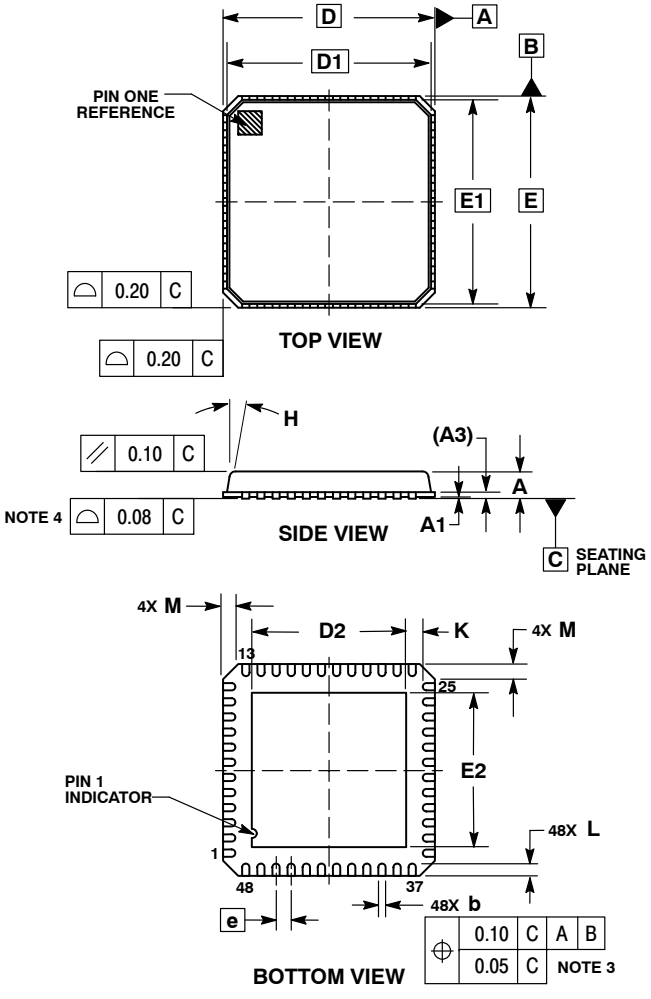
ON Semiconductor®

LFCSP48 7x7, 0.5P
CASE 932AD−01
ISSUE A

DATE 23 JAN 2009



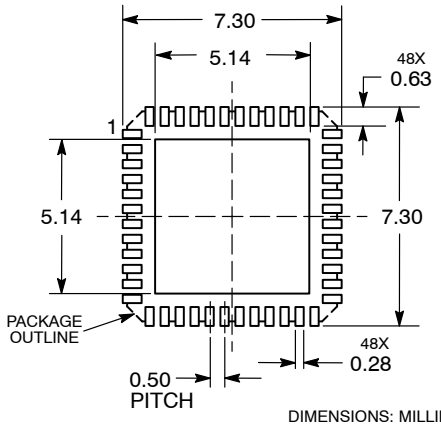
SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	7.00 BSC	
D1	6.75 BSC	
D2	4.95	5.25
E	7.00 BSC	
E1	6.75 BSC	
E2	4.95	5.25
e	0.50 BSC	
H	---	12°
K	0.20	---
L	0.30	0.50
M	---	0.60

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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