ON Semiconductor®

FPF2290
Over-Voltage Protection Load Switch

Features

- Surge Protection
  - IEC 61000-4-5: ±100 V
- Selectable Over-Voltage Protection (OVP) with OV1 and OV2 Logic inputs
  - 5.9 V ±100 mV
  - 10 V ±100 mV
  - 14 V ±280 mV
  - 23 V ±460 mV
- Over-Temperature Protection (OTP)
- Ultra-Low On-Resistance: Typ. 33 mΩ
- ESD Protection
  - Human Body Model (HBM): > 2 kV
  - Charged Device Model (CDM): > 1 kV
  - IEC 61000-4-2 Air Discharge: > 15 kV

Applications

- Mobile Handsets and Tablets
- Portable Media Players
- MP3 Players

Description

The FPF2290 features a low-R_{ON} internal FET and an operating voltage range of 2.5 V to 23 V. An internal clamping circuit is capable of shunting surge voltages of ±100 V, protecting downstream components and enhancing system robustness. The FPF2290 features over-voltage protection that powers down the internal FET if the input voltage exceeds the OVP threshold. The OVP threshold is selectable via Logic select pins (OV1 and OV2). Over-temperature protection also powers down the device at 130°C (typical).

The FPF2290 is available in a fully “green” compliant 1.3 mm × 1.8 mm Wafer-Level Chip-Scale Package (WLCSP) with backside laminate.

Ordering Information

Part Number	Operating Temperature Range	Top Mark	Package	Packing Method
FPF2290BUCX-F130	-40°C – +85°C	HR	12-Ball, 0.4 mm Pitch WLCSP	Tape & Reel

September-2017, Rev. 2

Publication Order Number:
FPF2290BUCX-F130/D

Block Diagram

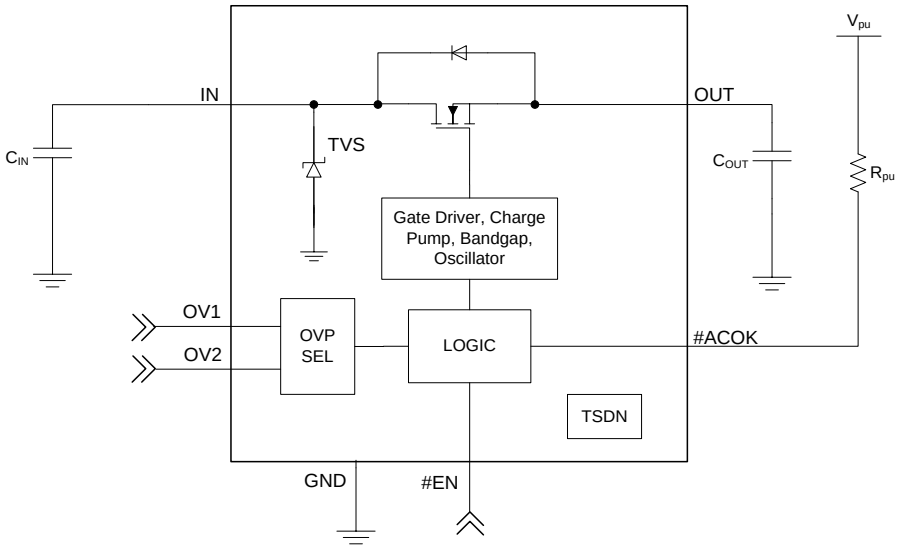
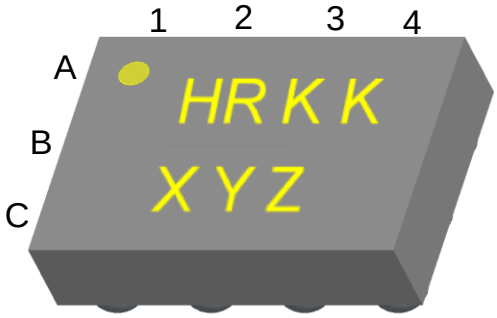


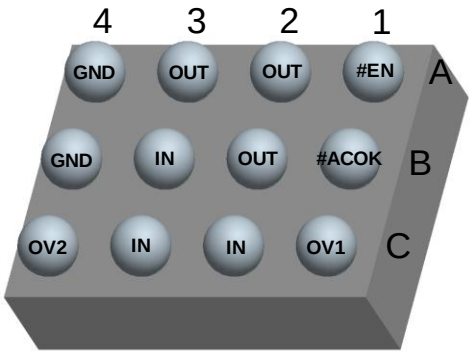
Figure 1. Functional Block Diagram

Note:

1. Setting OV1 and OV2 logic level are recommended before IN is applied.

Pin Configuration





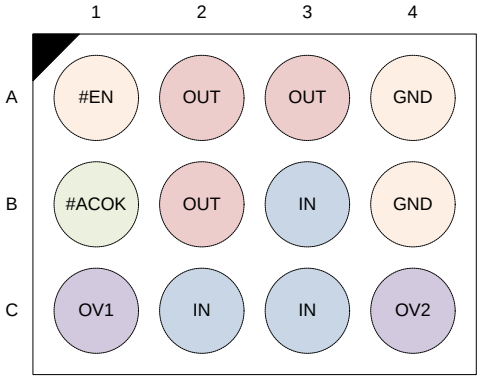


Figure 2. Pin Configuration (Top View)

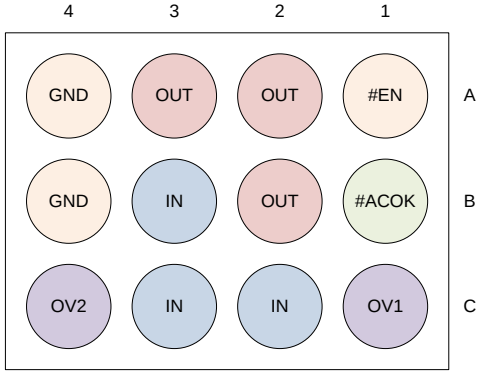


Figure 3. Pin Configuration (Bottom View)

Pin Definitions

Name	Bump	Type	Description		
IN	B3, C2, C3	Input/Supply	Switch Input and Device Supply		
OUT	A2, A3, B2	Output	Switch Output to Load		
#ACOK	B1	Output	Power Good (Open-Drain Output)	1	Hi-Z: $V_{IN} < V_{IN\_MIN}$ OR $V_{IN} > V_{OVLO}$
				0	LOW: Voltage Stable
#EN	A1	Input	Device Enable (Active LOW)		
OV1/2	C1, C4	Input	OVLO Selection Input (*see Table 1*) Note: Appy OV1 and OV2 Logic levels before VIN is applied.		
GND	A4, B4	Supply	Device Ground		

Table 1. OVLO Selection

OV1	OV2	OVP Trip Level
LOW	LOW	5.9 V ±100 mV
HIGH	LOW	10 V ±100 mV
LOW	HIGH	14 V ±280 mV
HIGH	HIGH	23 V ±460 mV

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{IN}	V_IN to GND & V_IN to V_OUT = GND or Float		-0.3	29.0	V
V_{OUT}	V_OUT to GND		-0.3	V_{IN} + 0.3	V
V_{OVn}	OV1 and OV2 to GND		-0.3	6.0	V
V_{EN_ACOK}	Maximum DC Voltage Allowed on #EN or #ACOK Pin			6	V
I_{IN}	Switch I/O Current (Continuous)			4.5	A
t_{PD}	Total Power Dissipation at T_A = 25°C			1.48	W
T_{STG}	Storage Temperature Range		-65	+150	°C
T_J	Maximum Junction Temperature			+150	°C
T_L	Lead Temperature (Soldering, 10 Seconds)			+260	°C
Θ_{JA}	Thermal Resistance, Junction-to-Ambient(2) (1-in.^{2} Pad of 2-oz. Copper)			84.1	°C/W
ESD	IEC 61000-4-2 System Level ESD	Air Discharge	15		kV
		Contact Discharge	8		
	Human Body Model, ANSI/ESDA/JEDEC JS-001-2012	All Pins	2		
	Charged Device Model, JESD22-C101	All Pins	1		
Surge	IEC 61000-4-5, Surge Protection	V_{IN}	±100		V

Note:

2. Measured using 2S2P JEDEC std. PCB.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. ON Semiconductor does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{IN}	Supply Voltage	2.5	23.0	V
T_A	Operating Temperature	-40	+85	°C

Electrical Characteristics

T_A = -40°C to 85°C, V_{IN} = 2.5 to 23 V, unless otherwise indicated. Typical values are V_{IN} = 5.0 V, $I_{IN} \leq$ 3 A, C_{IN} = 0.1 µF and T_A = 25°C.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
Basic Operation							
V_{IN_CLAMP}	Input Clamping Voltage	I_{IN} = 10 mA			35		V
I_Q	Input Quiescent Current	V_{IN} = 5 V, #EN = 0 V			80	115	µA
I_{IN_Q}	OVLO Supply Current	OV1 = LOW, OV2 = LOW V_{IN} = 6.5 V, V_{OUT} = 0 V			63	90	µA
V_{IN_OVLO}	Over-Voltage Trip Level	V_{IN} Rising	OV1 = LOW, OV2 = LOW	5.80	5.90	6.00	V
		V_{IN} Falling		5.75			
		V_{IN} Rising	OV1 = HIGH, OV2 = LOW	9.90	10.00	10.10	
		V_{IN} Falling		9.85			
		V_{IN} Rising	OV1 = LOW, OV2 = HIGH	13.72	14.0	14.28	
		V_{IN} Falling		13.52			
		V_{IN} Rising	OV1 = HIGH, OV2 = HIGH	22.54	23.0	23.46	
		V_{IN} Falling		22.34			
R_{ON}	Resistance from V_{IN} to V_{OUT}	V_{IN} = 5 V, I_{OUT} = 1 A, T_A = 25°C			33	40	mΩ
C_{OUT}	OUT Load Capacitance[3]	V_{IN} = 5 V		0.1		1000.0	µF
T_{SDN}	Thermal Shutdown[3]				130		°C
T_{SDN_HYS}	Thermal Shutdown Hysteresis[3]				20		°C
Digital Signals							
V_{OL}	#ACOK Output Low Voltage	I_{SINK} = 1 mA				0.4	V
I_{ACOK}	#ACOK Leakage Current	$V_{I/O}$ = 3.0 V, #ACOK Deasserted				0.5	µA
V_{IH}	Input HIGH Voltage (#EN, OVx)	V_{IN} = 2.5 V to V_{OVLO}		1.2			V
V_{IL}	Input LOW Voltage (#EN, OVx)	V_{IN} = 2.5 V to V_{OVLO}				0.5	V
I_{IN}	Input Leakage Current (#EN, OVx)	V_{IN} = 5.0 V, V_{OUT} = Float				1.0	µA
Timing Characteristics							
t_{DEB}	Debounce Time	Time from 2.5 V < V_{IN} < V_{IN_OVLO} to V_{OUT} = 0.1 × V_{IN}		10	15	20	ms
t_{START}	Soft-Start Time	Time from V_{IN} = V_{IN_min} to 0.2 × #ACOK, V_{IO} = 1.8 V with 10 kΩ Pull-up Resistor		20	30	40	ms
t_{ON}	Switch Turn-On Time	R_L = 100 Ω, C_L = 22 µF, V_{OUT} from 0.1 × V_{IN} to 0.9 × V_{IN}		1	3	5	ms
t_{OFF}	Switch Turn-Off Time[3]	R_L = 100 Ω, C_L = 0 µF, V_{IN} > V_{OVLO} to V_{OUT} = 0.8 × V_{IN}				150	ns

Note:

3. Guaranteed by characterization and design.

Timing Diagrams

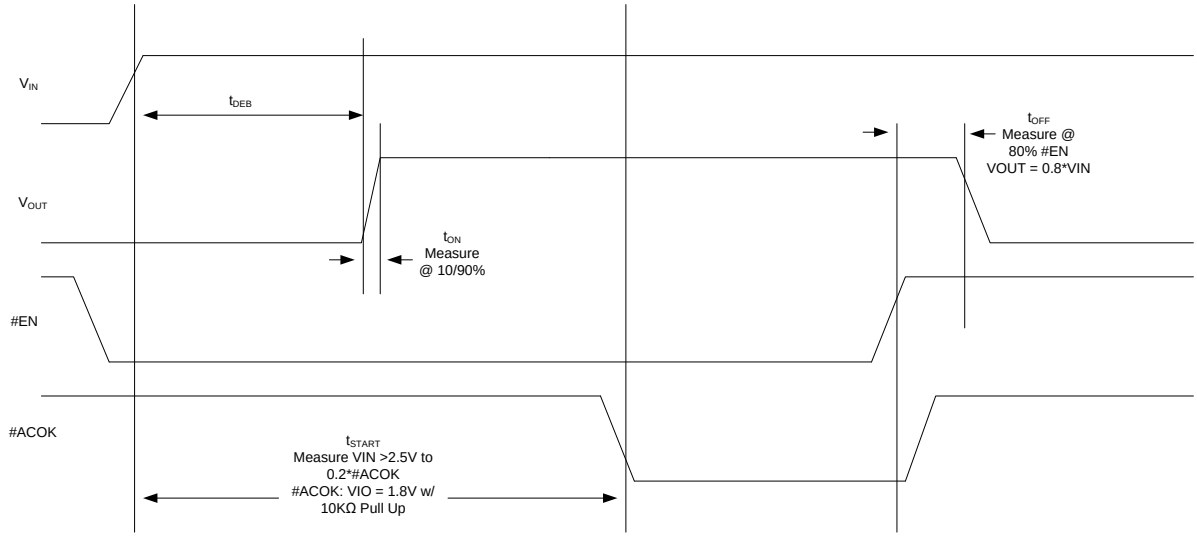


Figure 4. Timing for Power Up and Normal Operation

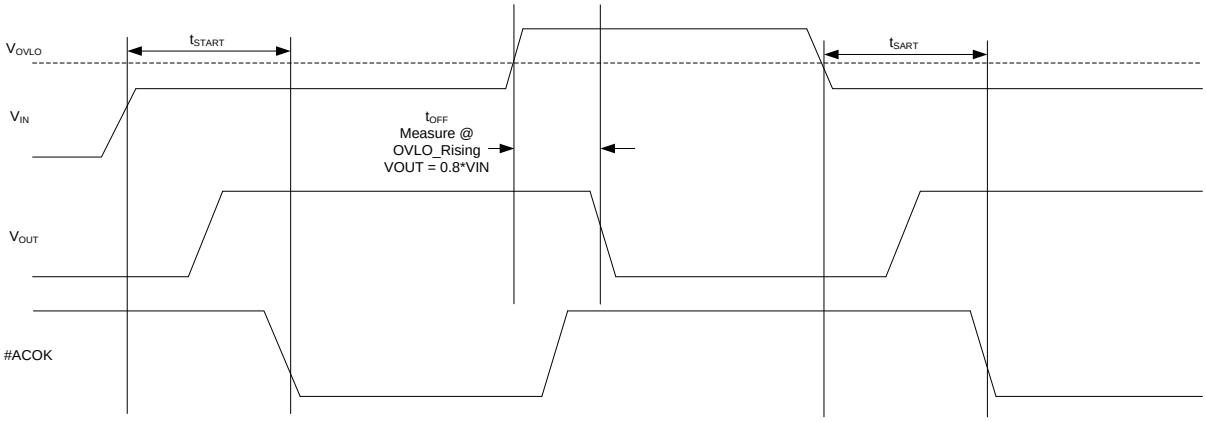
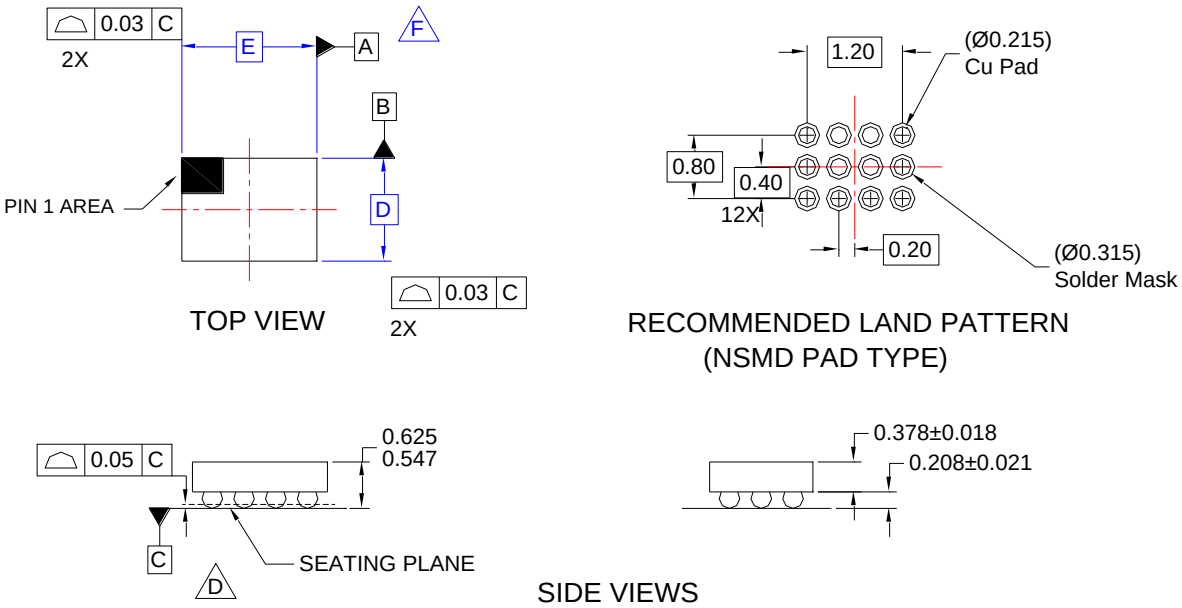


Figure 5. Timing for OVLO Trip

Product-Specific Dimensions

D	E	X	Y
1288 µm ±30 µm	1828 µm ±30 µm	314 µm ±18 µm	244 µm ±18 µm

Physical Dimensions



NOTES:

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE NOMINAL HEIGHT IS 586 MICRONS ±39 MICRONS (547-625 MICRONS).

F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

G. DRAWING FILENAME: MKT-UC012ZCrev2.

H. ON SEMICONDUCTOR RECOMMENDS THAT LANDS IN THE LANDPATTERN ARE AT LEAST .215MM DIAMETER AS MEASURED AT THE BOTTOM OF THE LAND, NOT THE TOP EDGE.

Figure 6. 12-Ball, 3×4 Array, 0.4 mm Pitch, Wafer-Level Chip-Scale Package (WLCSP)

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
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