PCN Number:	20221214000.2	**PCN Date:**	December 16, 2022
Title:	Qualification of TI CDAT as an additional Assembly and Test site for select package devices		
Customer Contact:	PCN Manager	**Dept:**	Quality Services
Proposed 1st Ship Date:	June 16, 2023	**Sample Requests accepted until:**	Jan 16, 2023

*Sample requests received after January 16, 2023 will not be supported.

Change Type:

☒	Assembly Site	☐	Design	☐	Wafer Bump Site
☐	Assembly Process	☐	Data Sheet	☐	Wafer Bump Material
☒	Assembly Materials	☐	Part number change	☐	Wafer Bump Process
☐	Mechanical Specification	☒	Test Site	☐	Wafer Fab Site
☐	Packing/Shipping/Labeling	☐	Test Process	☐	Wafer Fab Materials
				☐	Wafer Fab Process

PCN Details

Description of Change:

Texas Instruments Incorporated is announcing the qualification of TI CDAT as an additional Assembly and Test site for select devices. Material differences between sites are as follows:

	TI Malaysia	TI CDAT
Wire type	1.3mils Au	1.3mils Cu
Mold compound	4208625	4222198

Test coverage, insertions, conditions will remain consistent with current testing.

Reason for Change:

Continuity of Supply

Anticipated impact on Form, Fit, Function, Quality or Reliability (positive / negative):

None

Impact on Environmental Ratings

Checked boxes indicate the status of environmental ratings following implementation of this change. If below boxes are checked, there are no changes to the associated environmental ratings.

RoHS	REACH	Green Status	IEC 62474
☒ No Change	☒ No Change	☒ No Change	☒ No Change

Changes to product identification resulting from this PCN:

Assembly Site	Assembly Site Origin (22L)	Assembly Country Code (23L)	Assembly City
TI Malaysia	MLA	MYS	KUALA LUMPUR
TI CDAT	CDA	CHN	CHENGDU

Sample product shipping label (not actual product label)

OPT:
ITEM: 39
LBL: 5A (L)TO:1750

(1P) SN74LS07NSR
(Q) 2000 (D) 0336
(31T)LOT: 3959047MLA
(4W) TKY(1T) 7523483SI2
(P)
(2P) REV: (V) 0033317
(20L) CSO: SHE (21L) CCO:USA
(22L) ASO: MLA (23L) ACO: MYS

Product Affected:

TPS65310AQCDRVJRQ1	TPS65311QRVJRQ1

Qualification Report

Approve Date 07-Dec-2022

Automotive New Product Qualification Summary
(As per AEC-Q100 and JEDEC Guidelines)

Product Attributes

Attributes	Qual Device: TPS65310AQCDRVJRQ1	Qual Device: TPS65311QRVJRQ1	QBS Reference: TPS7A5401QRGRRQ1	QBS Reference: TPS65300QPWPRQ1
Automotive Grade Level	Grade 1	Grade 1	Grade 1	Grade 1
Operating Temp Range (C)	-40 to 125	-40 to 125	-40 to 125	-40 to 125
Product Function	Power Management	Power Management	Power Management	Power Management
Wafer Fab Supplier	DP1DM5	DP1DM5	RFAB	DP1DM5
Assembly Site	CDAT	CDAT	CDAT	TAI
Package Group	QFN	QFN	QFN	TSSOP
Package Designator	RVJ	RVJ	RGR	PWP
Pin Count	56	56	20	24

- QBS: Qual By Similarity
- Qual Device TPS65310AQCDRVJRQ1 is qualified at MSL3 260C
- Qual Device TPS65311QRVJRQ1 is qualified at MSL3 260C

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: TPS65310AQCDRVJRQ1	Qual Device: TPS65311QRVJRQ1
Test Group A - Accelerated Environment Stress Tests									
PC	A1	JEDEC J- STD-020 JESD22A113	3	77	Preconditioning	MSL3 260C	1 Step	3/0/1[1]	-
PC	A1	JEDEC J- STD-020 JESD22A113	3	77	Preconditioning	MSL2 260C	1 Step	-	-
HAST	A2	JEDEC	3	77	Biased HAST	130C/85%RH	96	3/231/0	-

		JESD22A110					Hours		
AC/UHAST	A3	JEDEC JESD22A102/JEDEC JESD22A118	3	77	Autoclave	121C/15psig	96 Hours	3/231/0	-
AC/UHAST	A3	JEDEC JESD22A102/JEDEC JESD22-A118	3	77	Unbiased HAST	130C/85%RH	96 Hours	-	-
TC	A4	JEDEC JESD22A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	3/231/1[1]	-
PTC	A5	JEDEC JESD22A105	1	45	PTC	-40/125C	1000 Cycles	1/45/1[1]	-
HTSL	A6	JEDEC JESD22A103	1	45	High Temperature Storage Life	150C	1000 Hours	1/45/0	-
HTSL	A6	JEDEC JESD22-A103	1	45	High Temperature Storage Life	175C	500 Hours	-	-
Test Group B - Accelerated Lifetime Simulation Tests									
HTOL	B1	JEDEC JESD22A108	1	77	Life Test	125C	1000 Hours	3/231/0	-
ELFR	B2	AEC Q100008	1	77	Early Life Failure Rate	125C	48 Hours	-	-
Test Group C - Package Assembly Integrity Tests									
WBS	C1	AEC Q100001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0	-
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0	-
SD	C3	JEDEC JESD22-B102	1	15	PB Solderability	>95% Lead Coverage	-	1/15/0	-
SD	C3	JEDEC JESD22-B102	1	15	PB-Free Solderability	>95% Lead Coverage	-	1/15/0	-
PD	C4	JEDEC JESD22B100 and B108	1	10	Physical Dimensions	Cpk>1.67	-	3/30/0	-
Test Group D - Die Fabrication Reliability Tests									

EM	D1	JESD61	-	-	Electromigration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
TDDB	D2	JESD35	-	-	Time Dependent Dielectric Breakdow n	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
HCI	D3	JESD60 & 28	-	-	Hot Carrier Injection	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
NBTI	D4	-	-	-	Negative Bias Temperature Instability	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
SM	D5	-	-	-	Stress Migration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
Test Group E - Electrical Verification Tests									
ESD	E2	AEC Q100002	1	3	ESD HBM	-	750 Volts	1/3/0	-
ESD	E3	AEC Q100011	1	3	ESD CDM	-	2000 Volts	1/3/0	-
LU	E4	AEC Q100004	1	6	Latch-Up	Per AEC Q100-004	-	1/6/0	-
ED	E5	AEC Q100009	3	30	Electrical Distributions	Cpk>1.67 Room, hot, and cold	-	3/90/0	-

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duratio n	QBS Reference: TPS7A5401QRGRRQ1	QBS Reference: TPS65300QPWPRQ1
Test Group A - Accelerated Environment Stress Tests									
PC	A1	JEDEC J- STD-020 JESD22A113	3	77	Preconditioning	MSL3 260C	1 Step	-	-
PC	A1	JEDEC J- STD-020 JESD22A113	3	77	Preconditioning	MSL2 260C	1 Step	3/0/0	-
HAST	A2	JEDEC JESD22A110	3	77	Biased HAST	130C/85%RH	96 Hours	3/231/0	-
AC/UHAST	A3	JEDEC JESD22A102/JEDEC JESD22A118	3	77	Autoclave	121C/15psig	96 Hours	-	-
AC/UHAST	A3	JEDEC	3	77	Unbiased HAST	130C/85%RH	96	1/77/0	-

		JESD22A102/JEDEC JESD22-A118					Hours		
TC	A4	JEDEC JESD22A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	3/231/0	-
PTC	A5	JEDEC JESD22A105	1	45	PTC	-40/125C	1000 Cycles	1/45/0	-
HTSL	A6	JEDEC JESD22A103	1	45	High Temperature Storage Life	150C	1000 Hours	-	-
HTSL	A6	JEDEC JESD22-A103	1	45	High Temperature Storage Life	175C	500 Hours	3/135/0	-
Test Group B - Accelerated Lifetime Simulation Tests									
HTOL	B1	JEDEC JESD22A108	1	77	Life Test	125C	1000 Hours	3/231/0	-
ELFR	B2	AEC Q100008	1	77	Early Life Failure Rate	125C	48 Hours	-	3/2400/0
Test Group C - Package Assembly Integrity Tests									
WBS	C1	AEC Q100001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0	-
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0	-
SD	C3	JEDEC JESD22-B102	1	15	PB Solderability	>95% Lead Coverage	-	1/15/0	-
SD	C3	JEDEC JESD22-B102	1	15	PB-Free Solderability	>95% Lead Coverage	-	1/15/0	-
PD	C4	JEDEC JESD22B100 and B108	1	10	Physical Dimensions	Cpk>1.67	-	3/30/0	-
Test Group D - Die Fabrication Reliability Tests									
EM	D1	JESD61	-	-	Electromigration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
TDDB	D2	JESD35	-	-	Time	-	-	Completed Per	Completed Per

					Dependent Dielectric Breakdown			Process Technology Requirements	Process Technology Requirements
HCI	D3	JESD60 & 28	-	-	Hot Carrier Injection	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
NBTI	D4	-	-	-	Negative Bias Temperature Instability	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
SM	D5	-	-	-	Stress Migration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
Test Group E - Electrical Verification Tests									
ESD	E2	AEC Q100002	1	3	ESD HBM	-	750 Volts	1/3/0	1/3/0
ESD	E3	AEC Q100011	1	3	ESD CDM	-	2000 Volts	1/3/0	-
LU	E4	AEC Q100004	1	6	Latch-Up	Per AEC Q100-004	-	1/6/0	1/6/0
ED	E5	AEC Q100009	3	30	Electrical Distributions	Cpk>1.67 Room, hot, and cold	-	3/90/0	1/30/0

Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable
The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours
The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles
Ambient Operating Temperature by Automotive Grade Level:
Grade 0 (or E): -40C to +150C
Grade 1 (or Q): -40C to +125C
Grade 2 (or T): -40C to +105C
Grade 3 (or I) : -40C to +85C
E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):
Room/Hot/Cold : HTOL, ED
Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU Room : AC/uHAST
Quality and Environmental data is available at TI's external Web site: http://www.ti.com/
[1]-Die fabrication issue. Please contact TI for 8D reports.

Qualification Report

Approve Date 07-Dec-2022

Automotive New Product Qualification Summary
(As per AEC-Q100, AEC-Q006, and JEDEC Guidelines)

Product Attributes

Attributes	Qual Device:	QBS Reference:

	TPS65310AQCDRVJRQ1	TPS7A5401QRGRRQ1
Die Attributes		
Wafer Fab Supplier	DP1DM5	RFAB
Wafer Process	LBC5M	LBC7M
Assembly Site	CDAT	CDAT
Package Group	QFN	QFN
Package Designator	RVJ	RGR
Pin Count	56	20

QBS: Qual By Similarity
Qual Device TPS65310AQCDRVJRQ1 is qualified at MSL3 260C

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: TPS65310AQCDRVJRQ1	QBS Reference: TPS7A5401QRGRRQ1
PC	A1.1	-	3	22	SAM Precon Pre	Review for delamination	1 Step	1/22/0	3/66/0
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL3 260C	1 Step	3/0/1[1]	-
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL2 260C	1 Step	-	3/0/0
PC	A1.2	-	3	22	SAM Precon Post	Review for delamination	1 Step	1/22/0	3/66/0
HAST	A2.1	JEDEC JESD22-A110	3	77	Biased HAST	130C/85%RH	96 Hours	3/231/0	3/231/0
HAST	A2.1.2	-	3	1	Cross Section, post bHAST, 1X	Post stress cross section	Completed	-	3/3/0
HAST	A2.1.3	-	3	30	Wire Bond Shear, post bHAST, 1X	Post stress	Wires	1/30/0	3/90/0
HAST	A2.1.4	-	3	30	Bond Pull over Stitch, post bHAST, 1X	Post stress	Wires	1/30/0	3/90/0
HAST	A2.1.5	-	3	30	Bond Pull over Ball, post bHAST, 1X	Post stress	Wires	1/30/0	3/90/0

HAST	A2.2	JEDEC JESD22-A110	3	77	Biased HAST	130C/85%RH	192 Hours	1/77/0	3/231/0
HAST	A2.2.1	-	3	22	SAM Analysis, post bHAST 2X	Review for delamination	Completed	1/22/0	3/66/0
HAST	A2.2.2	-	3	1	Cross Section, post bHAST, 2X	Post stress cross section	Completed	1/1/0	3/3/0
HAST	A2.2.3	-	3	30	Wire Bond Shear, post bHAST, 2X	Post stress	Wires	1/30/0	3/90/0
HAST	A2.2.4	-	3	30	Bond Pull over Stitch, post bHAST, 2X	Post stress	Wires	1/30/0	3/90/0
HAST	A2.2.5	-	3	30	Bond Pull over Ball, post bHAST, 2X	Post stress	Wires	1/30/0	3/90/0
TC	A4.1	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	3/231/1[1]	3/231/0
TC	A4.1.1	-	3	22	SAM Analysis, post TC 1X	Review for delamination	Completed	1/22/0	3/66/0
TC	A4.1.2	-	3	1	Cross Section, post TC, 1X	Post stress cross section	Completed	1/1/0	3/3/0
TC	A4.1.3	-	3	30	Wire Bond Shear, post TC, 1X	Post stress	Wires	1/30/0	3/90/0
TC	A4.1.4	-	3	30	Bond Pull over Stitch, post TC, 1X	Post stress	Wires	1/30/0	3/90/0
TC	A4.1.5	-	3	30	Bond Pull over Ball, post TC, 1X	Post stress	Wires	1/30/0	3/90/0
TC	A4.2	JEDEC JESD22A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	1000 Cycles	1/77/0	3/231/0
TC	A4.2.1	-	3	22	SAM Analysis, post TC, 2X	Review for delamination	Completed	1/22/0	3/66/0
TC	A4.2.2	-	3	1	Cross Section, post TC, 2X	Post stress cross section	Completed	1/1/0	3/3/0
TC	A4.2.3	-	3	30	Wire Bond Shear, post TC,	Post stress	Wires	1/30/0	3/90/0

					2X				
TC	A4.2.4	-	3	30	Bond Pull over Stitch, post TC, 2X	Post stress	Wires	1/30/0	3/90/0
TC	A4.2.5	-	3	30	Bond Pull over Ball, post TC, 2X	Post stress	Wires	1/30/0	3/90/0
PTC	A5.1	JEDEC JESD22-A105	1	45	PTC	-40/125C	1000 Cycles	1/45/1[1]	1/45/0
PTC	A5.2	JEDEC JESD22A105	1	45	PTC	-40/125C	2000 Cycles	1/44/0	-
HTSL	A6.1	JEDEC JESD22-A103	3	45	High Temperature Storage Life	150C	1000 Hours	1/45/0	-
HTSL	A6.1	JEDEC JESD22-A103	3	45	High Temperature Storage Life	175C	500 Hours	-	3/135/0
HTSL	A6.1.1	-	3	1	Cross Section, post HTSL, 1X	Post stress cross section	Completed	1/1/0	3/3/0
HTSL	A6.2	JEDEC JESD22A103	3	45	High Temperature Storage Life	150C	2000 Hours	1/45/0	-
HTSL	A6.2	JEDEC JESD22A103	3	45	High Temperature Storage Life	175C	1000 Hours	-	3/135/0
HTSL	A6.2.1	-	3	1	Cross Section, post HTSL, 2X	Post stress cross section	Completed	1/1/0	3/3/0

Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable
The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours
The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours
The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles

Ambient Operating Temperature by Automotive Grade Level:
Grade 0 (or E): -40C to +150C
Grade 1 (or Q): -40C to +125C
Grade 2 (or T): -40C to +105C
Grade 3 (or I) : -40C to +85C

E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):
Room/Hot/Cold : HTOL, ED
Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU Room : AC/uHAST
Quality and Environmental data is available at TI's external Web site: http://www.ti.com/
[1]-Die fabrication issue. Please contact TI for 8D reports.

For questions regarding this notice, e-mails can be sent to the contacts shown below or your local Field Sales Representative.

Location	E-Mail
WW Change Management Team	PCN_ww_admin_team@list.ti.com

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.