

# CD40194B Types

## CMOS 4-Bit Bidirectional Universal Shift Register

High-Voltage Types (20 Volt Rating)

■ CD40194B is a universal shift register featuring parallel inputs, parallel outputs SHIFT RIGHT and SHIFT LEFT serial inputs, and a direct overriding clear input. In the parallel-load mode (S0 and S1 are high), data is loaded into the associated flip-flop and appears at the output after the positive transition of the CLOCK input. During loading, serial data flow is inhibited. Shift right and shift left are accomplished synchronously on the positive clock edge with data entered at the SHIFT RIGHT and SHIFT LEFT serial inputs, respectively. Clocking of the register is inhibited when both mode control inputs are low. When low, the RESET input resets all stages and forces all outputs low.

The CD40194B types are supplied in 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

**MAXIMUM RATINGS, Absolute-Maximum Values:**

<b>DC SUPPLY-VOLTAGE RANGE, (V<sub>DD</sub>)</b>	
Voltages referenced to V <sub>SS</sub> Terminal	-0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5V to V <sub>DD</sub> +0.5V
DC INPUT CURRENT, ANY ONE INPUT	±10mA
<b>POWER DISSIPATION PER PACKAGE (P<sub>D</sub>):</b>	
For T <sub>A</sub> = -55°C to +100°C	500mW
For T <sub>A</sub> = +100°C to +125°C	Derate Linearity at 12mW/°C to 200mW
<b>DEVICE DISSIPATION PER OUTPUT TRANSISTOR</b>	
FOR T <sub>A</sub> = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100mW
OPERATING-TEMPERATURE RANGE (T <sub>A</sub> )	-55°C to +125°C
STORAGE TEMPERATURE RANGE (T <sub>stg</sub> )	-65°C to +150°C
<b>LEAD TEMPERATURE (DURING SOLDERING):</b>	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max	+265°C

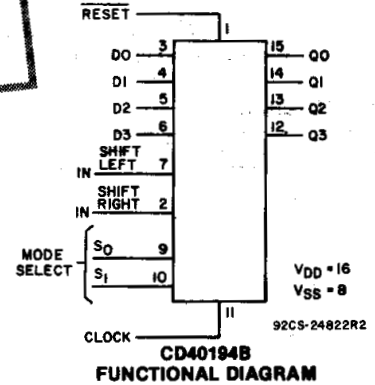
NOT RECOMMENDED FOR NEW DESIGNS

**Features:**

- Medium-speed: f<sub>CL</sub> = 12 MHz (typ.) @ V<sub>DD</sub> = 10 V
- Fully static operation
- Synchronous parallel or serial operation
- Asynchronous master reset
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

**Applications:**

- Arithmetic unit bus registers
- Serial/parallel conversions
- General-purpose register for bus-organized systems
- General-purpose registers



3  
COMMERCIAL CMOS  
HIGH VOLTAGE ICs

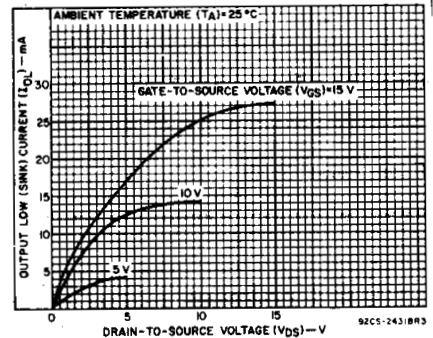


Fig. 1—Typical n-channel output low (sink) current characteristics.

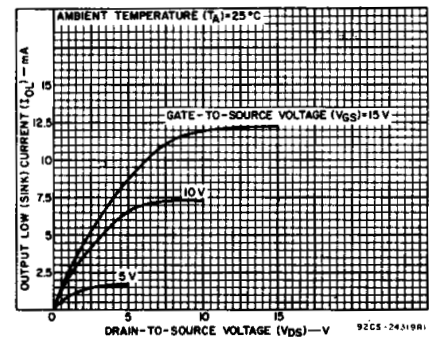


Fig. 2—Minimum n-channel output low (sink) current characteristics.

# CD40194B Types

**RECOMMENDED OPERATING CONDITIONS** at  $T_A = 25^\circ\text{C}$ , Except as Noted.  
 For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	VDD (V)	LIMITS		UNITS
		Min.	Max.	
Supply-Voltage Range (For Package-Temperature Range)		3	18	V
Setup Time, D0, D3, SR <sub>IN</sub> , SL <sub>IN</sub> to clock  SELECT 0, SELECT 1 to clock	5	100	—	ns
	10	70	—	
	15	50	—	
Hold Time, D0, D03, SR <sub>IN</sub> , SL <sub>IN</sub> to clock  SELECT 0, SELECT 1 to clock	5	0	—	ns
	10	0	—	
	15	0	—	
Clock Pulse Width,   Clock Input Frequency	5	180	—	MHz
	10	80	—	
	15	50	—	
Clock Input Rise or Fall Time,  Reset Pulse Width,	5	1000	—	μs
	10	100	—	
	15	100	—	
Clock Input Frequency	5	—	3	MHz
	10	—	6	
	15	—	8	
Clock Input Rise or Fall Time,  Reset Pulse Width,	5	1000	—	μs
	10	100	—	
	15	100	—	
Reset Pulse Width,	5	300	—	ns
	10	200	—	
	15	140	—	

## CONTROL TRUTH TABLE FOR CD40194B SERIES

CLOCK	MODE SELECT		RESET	ACTION
	S <sub>0</sub>	S <sub>1</sub>		
X	0	0	1	No Change
	1	0	1	Shift Right (Q0 toward Q3)
	0	1	1	Shift Left (Q3 toward Q0)
	1	1	1	Parallel Load
X	X	X	0	Reset

1 = High level  
 0 = Low level

X = Don't care  
 ▲ = Level change

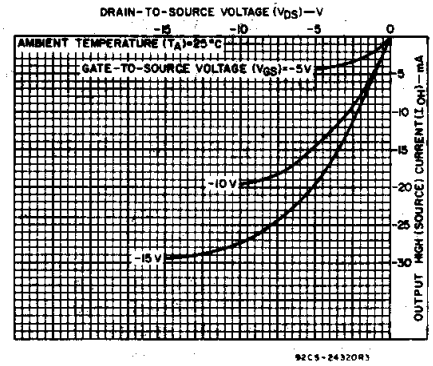


Fig. 3—Typical p-channel output high (source) current characteristics.

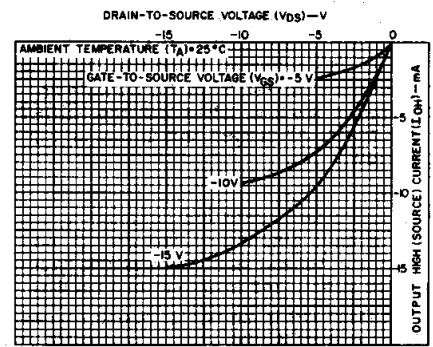


Fig. 4—Minimum p-channel output high (source) current characteristics.

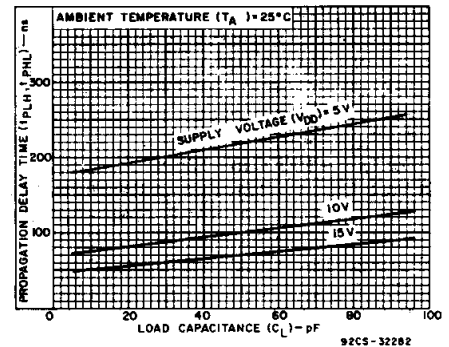


Fig. 5—Typical propagation delay time as a function of load capacitance, (CLOCK to Q).

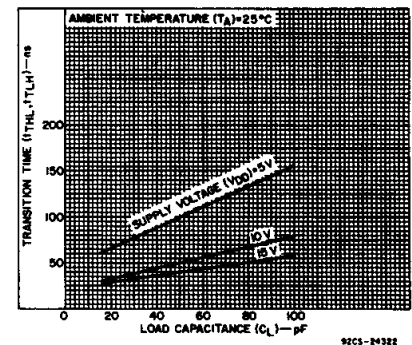


Fig. 6—Typical transition time as a function of load capacitance.

# CD40194B Types

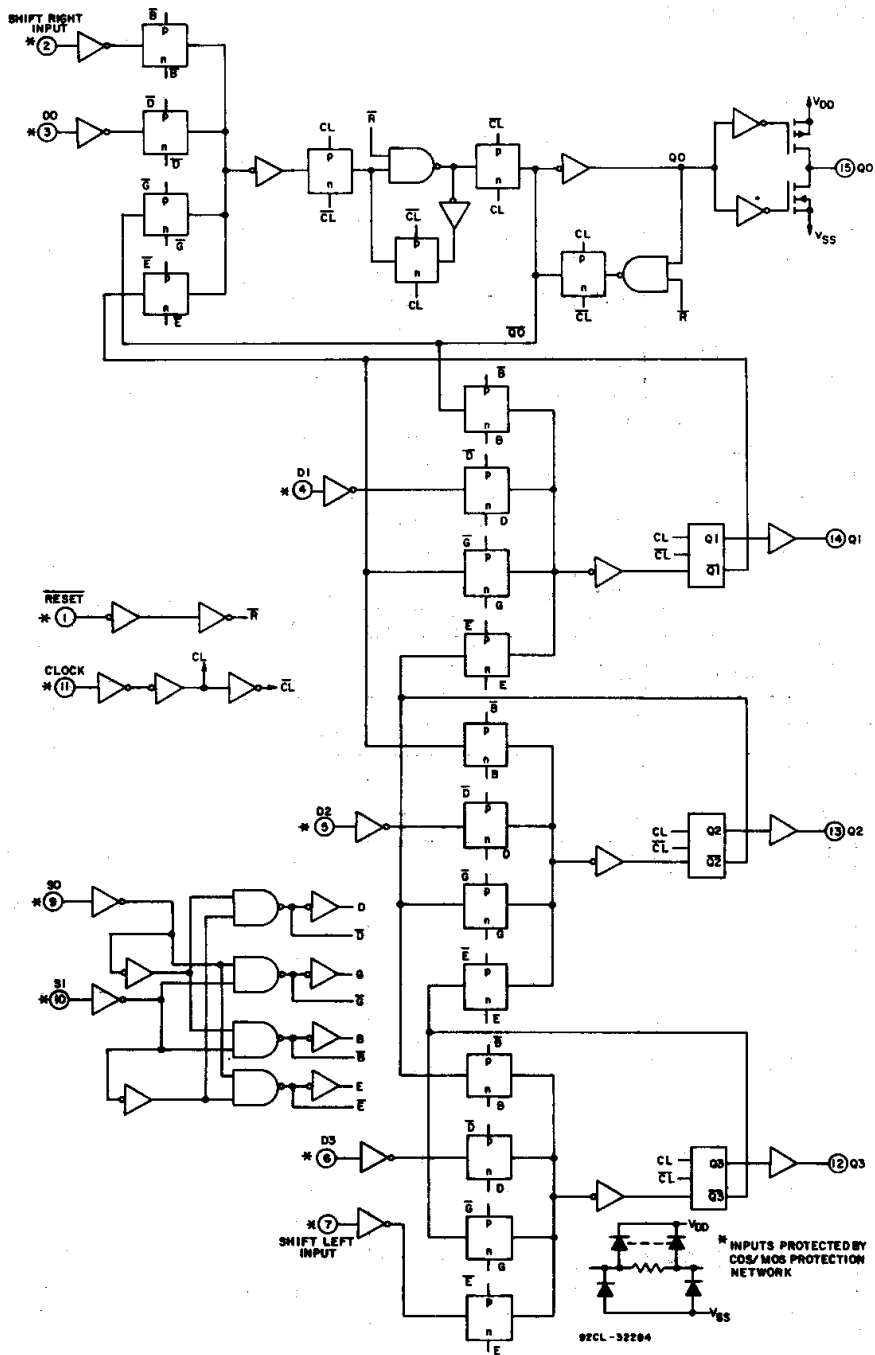


Fig. 8—CD40194B logic diagram.

COMMERCIAL CMOS  
HIGH VOLTAGE ICs

# CD40194B Types

## STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V <sub>O</sub> (V)	V <sub>IN</sub> (V)	V <sub>DD</sub> (V)	-55	-40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I <sub>DD</sub> Max.	—	0,5	5	5	5	150	150	—	0.04	5	μA
	—	0,10	10	10	10	300	300	—	0.04	10	
	—	0,15	15	20	20	600	600	—	0.04	20	
Output Low (Sink) Current, I <sub>OL</sub> Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0,10	10	1.8	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, I <sub>OH</sub> Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	mA
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
Output Voltage: Low-Level, V <sub>OL</sub> Max.	—	0,5	5	0.05				—	0	0.05	V
	—	0,10	10	0.05				—	0	0.05	
	—	0,15	15	0.05				—	0	0.05	
Output Voltage: High-Level, V <sub>OH</sub> Min.	—	0,5	5	4.95				4.95	5	—	V
	—	0,10	10	9.95				9.95	10	—	
	—	0,15	15	14.95				14.95	15	—	
Input Low Voltage, V <sub>IL</sub> Max.	0.5,4.5	—	5	1.5				—	—	1.5	V
	1,9	—	10	3				—	—	3	
	1.5,13.5	—	15	4				—	—	4	
Input High Voltage, V <sub>IH</sub> Min.	0.5,4.5	—	5	3.5				3.5	—	—	V
	1,9	—	10	7				7	—	—	
	1.5,13.5	—	15	11				11	—	—	
Input Current I <sub>IN</sub> Max.	—	0,18	18	±0.1	±0.1	±1	±1	—	±10 <sup>-5</sup>	±0.1	μA
3-State Output Leakage Current, I <sub>OUT</sub> Max.	0,18	0,18	18	±0.4	±0.4	±12	±12	—	±10 <sup>-4</sup>	±0.4	μA

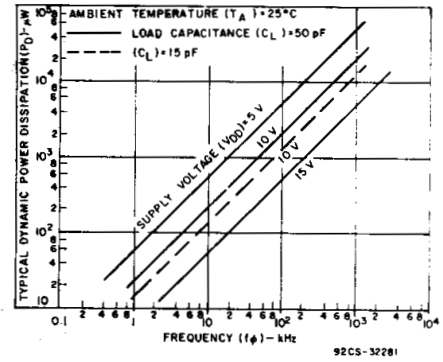


Fig. 9—Typical power dissipation as a function of frequency.

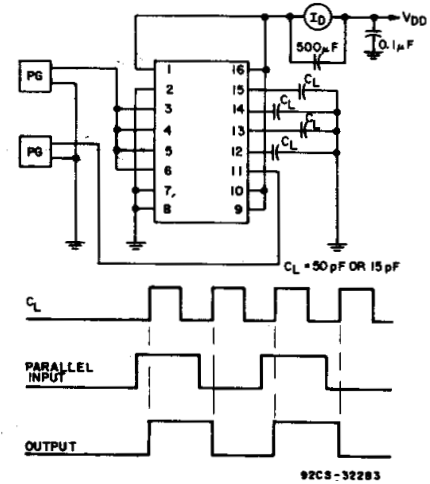


Fig. 10—Dynamic power dissipation test circuit.

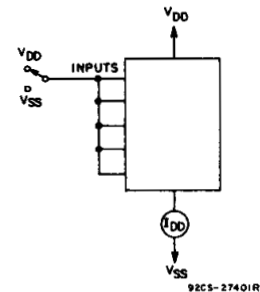


Fig. 11—Quiescent device current test circuit.

# CD40194B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ ,  
 Input  $t_r, t_f = 20 \text{ ns}$ ,  $C_L = 50 \text{ pF}$ ,  $R_L = 200 \text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS	
		VDD V	Min.	Typ.		Max.
Propagation Delay Time: Clock to Q $t_{PHL}, t_{PLH}$		5	—	220	440	ns
		10	—	100	200	
		15	—	70	140	
Output Transition Time $t_{THL}, t_{TLH}$		5	—	100	200	
		10	—	50	100	
		15	—	40	80	
Minimum Setup Time: $t_s$ D0, D3, $SR_{1N}, SL_{1N}$ to Clock		5	—	80	160	
		10	—	35	70	
		15	—	20	50	
SELECT 0, SELECT 1 to Clock		5	—	200	400	
		10	—	110	220	
		15	—	65	130	
Minimum Hold Time: $t_H$ D0, D3, $SR_{1N}, SL_{1N}$ to Clock		5	—	-65	0	
		10	—	-25	0	
		15	—	-15	0	
SELECT 0, SELECT 1 to Clock		5	—	-170	0	
		10	—	-95	0	
		15	—	-55	0	
Minimum Clock Pulse Width $t_w$		5	—	90	180	
		10	—	40	80	
		15	—	25	50	
Maximum Clock Input Frequency $f_{CL}$		5	3	6	—	MHz
		10	6	12	—	
		15	8	15	—	
Maximum Clock Rise or Fall Time $t_{rCL}, t_{fCL}$		5	—	—	1000	$\mu\text{s}$
		10	—	—	100	
		15	—	—	100	
Minimum Reset Pulse Width* $t_{WR}$		5	—	150	300	ns
		10	—	100	200	
		15	—	70	140	
Reset Propagation Delay $t_{PRHL}$		5	—	230	460	
		10	—	90	180	
		15	—	65	130	
Input Capacitance $C_{iN}$	Any Input	—	5	7.5	pF	

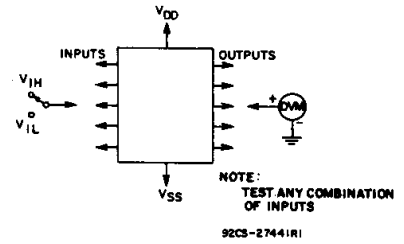


Fig. 12—Input-voltage test circuit.

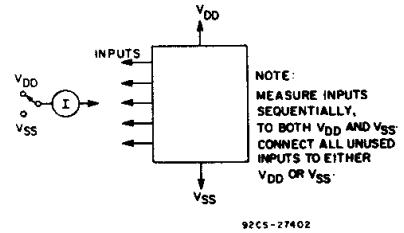
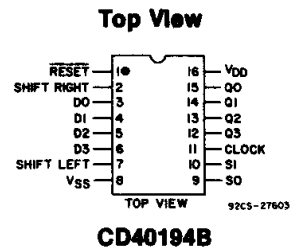


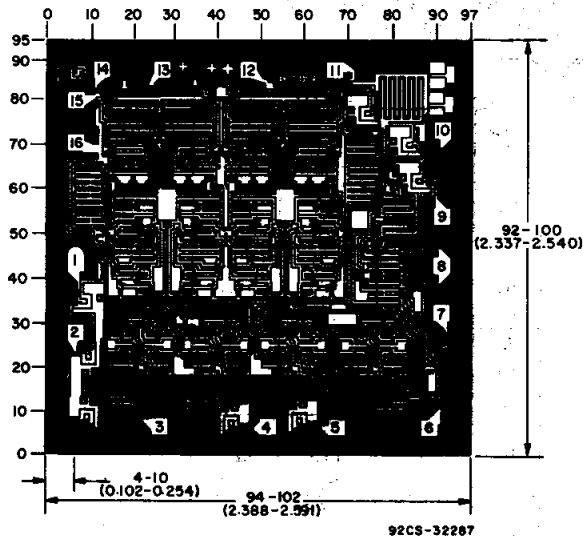
Fig. 13—Input current test circuit.

## TERMINAL DIAGRAM



3  
COMMERCIAL CMOS  
HIGH VOLTAGE ICs

## CD40194B Types



*Dimensions and pad layout for CD40194BH*

*Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).*

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD40194BE	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD40194BE	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.



## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (<https://www.ti.com/legal/termsofsale.html>) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2021, Texas Instruments Incorporated