

MC34163, MC33163

Switching Regulators - Step-Up/Down, Inverting

3.4 A

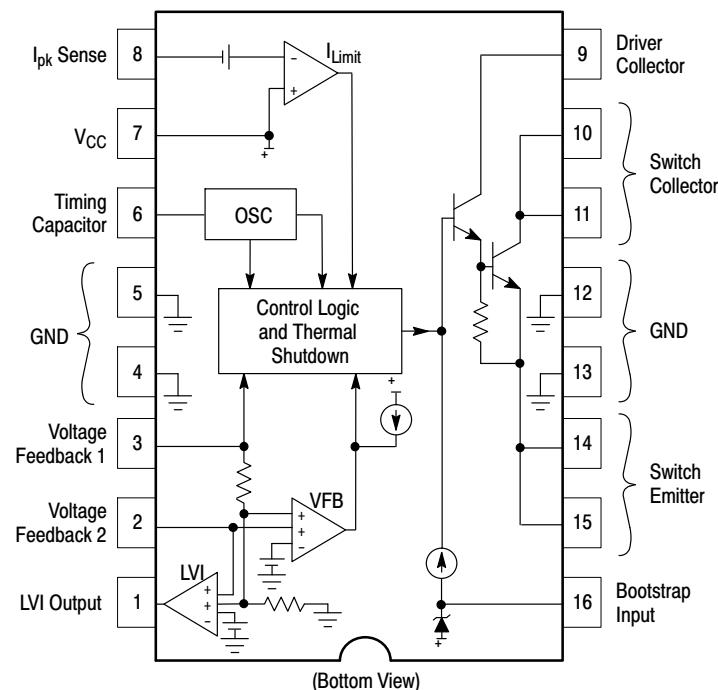
The MC34163 series are monolithic power switching regulators that contain the primary functions required for dc-to-dc converters. This series is specifically designed to be incorporated in step-up, step-down, and voltage-inverting applications with a minimum number of external components.

These devices consist of two high gain voltage feedback comparators, temperature compensated reference, controlled duty cycle oscillator, driver with bootstrap capability for increased efficiency, and a high current output switch. Protective features consist of cycle-by-cycle current limiting, and internal thermal shutdown. Also included is a low voltage indicator output designed to interface with microprocessor based systems.

These devices are contained in a 16 pin dual-in-line heat tab plastic package for improved thermal conduction.

Features

- Output Switch Current in Excess of 3.0 A
- Operation from 2.5 V to 40 V Input
- Low Standby Current
- Precision 2% Reference
- Controlled Duty Cycle Oscillator
- Driver with Bootstrap Capability for Increased Efficiency
- Cycle-by-Cycle Current Limiting
- Internal Thermal Shutdown Protection
- Low Voltage Indicator Output for Direct Microprocessor Interface
- Heat Tab Power Package
- Moisture Sensitivity Level (MSL) Equals 1
- Pb-Free Packages are Available*



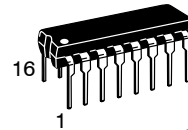
(Bottom View)
This device contains 114 active transistors.
Figure 1. Representative Block Diagram



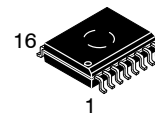
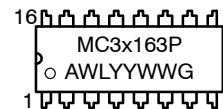
ON Semiconductor®

<http://onsemi.com>

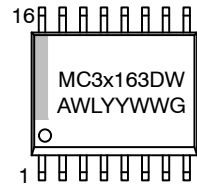
MARKING DIAGRAMS



**PDIP-16
P SUFFIX
CASE 648C**

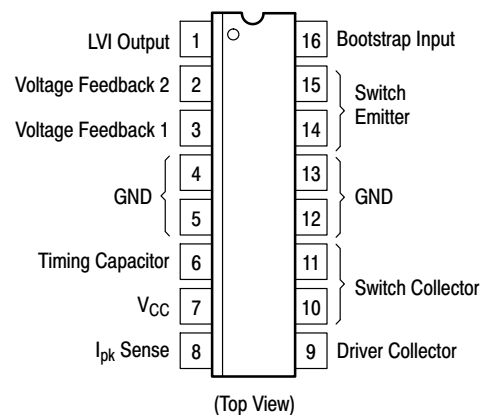


**SOIC-16W
DW SUFFIX
CASE 751G**



- x = 3 or 4
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC34163, MC33163

MAXIMUM RATINGS (Note 1)

| Rating | Symbol | Value | Unit |
|--|-------------------------|----------------------------------|-----------------------------|
| Power Supply Voltage | V_{CC} | 40 | V |
| Switch Collector Voltage Range | $V_{C(\text{switch})}$ | -1.0 to +40 | V |
| Switch Emitter Voltage Range | $V_{E(\text{switch})}$ | -2.0 to $V_{C(\text{switch})}$ | V |
| Switch Collector to Emitter Voltage | $V_{CE(\text{switch})}$ | 40 | V |
| Switch Current (Note 2) | I_{SW} | 3.4 | A |
| Driver Collector Voltage | $V_{C(\text{driver})}$ | -1.0 to +40 | V |
| Driver Collector Current | $I_{C(\text{driver})}$ | 150 | mA |
| Bootstrap Input Current Range (Note 2) | I_{BS} | -100 to +100 | mA |
| Current Sense Input Voltage Range | $V_{Ipk(\text{Sense})}$ | $(V_{CC}-7.0)$ to $(V_{CC}+1.0)$ | V |
| Feedback and Timing Capacitor Input Voltage Range | V_{in} | -1.0 to +7.0 | V |
| Low Voltage Indicator Output Voltage Range | $V_{C(LVI)}$ | -1.0 to +40 | V |
| Low Voltage Indicator Output Sink Current | $I_{C(LVI)}$ | 10 | mA |
| Thermal Characteristics | | | $^{\circ}\text{C}/\text{W}$ |
| P Suffix, Dual-In-Line Case 648C | | | |
| Thermal Resistance, Junction-to-Air | $R_{\theta JA}$ | 80 | |
| Thermal Resistance, Junction-to-Case (Pins 4, 5, 12, 13) | $R_{\theta JC}$ | 15 | |
| DW Suffix, Surface Mount Case 751G | | | |
| Thermal Resistance, Junction-to-Air | $R_{\theta JA}$ | 94 | |
| Thermal Resistance, Junction-to-Case (Pins 4, 5, 12, 13) | $R_{\theta JC}$ | 18 | |
| Operating Junction Temperature | T_J | +150 | $^{\circ}\text{C}$ |
| Operating Ambient Temperature (Note 3) | T_A | | $^{\circ}\text{C}$ |
| MC34163 | | 0 to +70 | |
| MC33163 | | -40 to +85 | |
| Storage Temperature Range | T_{stg} | -65 to +150 | $^{\circ}\text{C}$ |

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. This device series contains ESD protection and exceeds the following tests: Human Body Model 1500 V per MIL-STD-883, Method 3015. Machine Model Method 150 V.
2. Maximum package power dissipation limits must be observed.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

ORDERING INFORMATION

| Device | Package | Shipping [†] |
|--------------|-----------------------|-----------------------|
| MC33163DW | SOIC-16W | 47 Units / Rail |
| MC33163DWG | SOIC-16W (Pb-Free) | 47 Units / Rail |
| MC33163DWR2 | SOIC-16W | 1000 Units / Reel |
| MC33163DWR2G | SOIC-16W (Pb-Free) | 1000 Units / Reel |
| MC33163P | PDIP-16 | 25 Units / Rail |
| MC33163PG | PDIP-16 (Pb-Free) | 25 Units / Rail |
| MC34163DW | SOIC-16W | 47 Units / Rail |
| MC34163DWG | SOIC-16W (Pb-Free) | 47 Units / Rail |
| MC34163DWR2 | SOIC-16W | 1000 Units / Reel |
| MC34163DWR2G | SOIC-16W (Pb-Free) | 1000 Units / Reel |
| MC34163P | PDIP-16 | 25 Units / Rail |
| MC34163PG | PDIP-16 (Pb-Free) | 25 Units / Rail |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MC34163, MC33163

ELECTRICAL CHARACTERISTICS ($V_{CC} = 15\text{ V}$, Pin 16 = V_{CC} , $C_T = 620\text{ pF}$, for typical values $T_A = 25^\circ\text{C}$, for min/max values T_A is the operating ambient temperature range that applies (Note 5), unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|----------------|--------|-----|-----|-----|------|
|----------------|--------|-----|-----|-----|------|

OSCILLATOR

| | | | | | |
|--|----------------------|----------|---------|----------|---------------|
| Frequency $T_A = 25^\circ\text{C}$ Total Variation over $V_{CC} = 2.5\text{ V}$ to 40 V , and Temperature | f_{OSC} | 46 45 | 50 – | 54 55 | kHz |
| Charge Current | I_{chg} | – | 225 | – | μA |
| Discharge Current | I_{dischg} | – | 25 | – | μA |
| Charge to Discharge Current Ratio | I_{chg}/I_{dischg} | 8.0 | 9.0 | 10 | – |
| Sawtooth Peak Voltage | $V_{OSC(P)}$ | – | 1.25 | – | V |
| Sawtooth Valley Voltage | $V_{OSC(V)}$ | – | 0.55 | – | V |

FEEDBACK COMPARATOR 1

| | | | | | |
|--|---------------|------------------|--------------------|---------------------|---------------|
| Threshold Voltage $T_A = 25^\circ\text{C}$ Line Regulation ($V_{CC} = 2.5\text{ V}$ to 40 V , $T_A = 25^\circ\text{C}$) Total Variation over Line, and Temperature | $V_{th(FB1)}$ | 4.9 – 4.85 | 5.05 0.008 – | 5.2 0.03 5.25 | V %/V V |
| Input Bias Current ($V_{FB1} = 5.05\text{ V}$) | $I_{B(FB1)}$ | – | 100 | 200 | μA |

FEEDBACK COMPARATOR 2

| | | | | | |
|--|---------------|---------------------|--------------------|------------------------|---------------|
| Threshold Voltage $T_A = 25^\circ\text{C}$ Line Regulation ($V_{CC} = 2.5\text{ V}$ to 40 V , $T_A = 25^\circ\text{C}$) Total Variation over Line, and Temperature | $V_{th(FB2)}$ | 1.225 – 1.213 | 1.25 0.008 – | 1.275 0.03 1.287 | V %/V V |
| Input Bias Current ($V_{FB2} = 1.25\text{ V}$) | $I_{B(FB2)}$ | – 0.4 | 0 | 0.4 | μA |

CURRENT LIMIT COMPARATOR

| | | | | | |
|--|----------------------|----------|----------|----------|---------------|
| Threshold Voltage $T_A = 25^\circ\text{C}$ Total Variation over $V_{CC} = 2.5\text{ V}$ to 40 V , and Temperature | $V_{th(Ipk\ Sense)}$ | – 230 | 250 – | – 270 | mV |
| Input Bias Current ($V_{Ipk\ (Sense)} = 15\text{ V}$) | $I_{B(sense)}$ | – | 1.0 | 20 | μA |

DRIVER AND OUTPUT SWITCH (Note 4)

| | | | | | |
|---|-------------------|----------------|----------------|----------------|---------------|
| Sink Saturation Voltage ($I_{SW} = 2.5\text{ A}$, Pins 14, 15 grounded) Non-Darlington Connection ($R_{Pin\ 9} = 110\ \Omega$ to V_{CC} , $I_{SW}/I_{DRV} \approx 20$) Darlington Connection (Pins 9, 10, 11 connected) | $V_{CE(sat)}$ | – – | 0.6 1.0 | 1.0 1.4 | V |
| Collector Off-State Leakage Current ($V_{CE} = 40\text{ V}$) | $I_{C(off)}$ | – | 0.02 | 100 | μA |
| Bootstrap Input Current Source ($V_{BS} = V_{CC} + 5.0\text{ V}$) | $I_{source(DRV)}$ | 0.5 | 2.0 | 4.0 | mA |
| Bootstrap Input Zener Clamp Voltage ($I_Z = 25\text{ mA}$) | V_Z | $V_{CC} + 6.0$ | $V_{CC} + 7.0$ | $V_{CC} + 9.0$ | V |

LOW VOLTAGE INDICATOR

| | | | | | |
|---|---------------|------|-------|------|---------------|
| Input Threshold (V_{FB2} Increasing) | V_{th} | 1.07 | 1.125 | 1.18 | V |
| Input Hysteresis (V_{FB2} Decreasing) | V_H | – | 15 | – | mV |
| Output Sink Saturation Voltage ($I_{sink} = 2.0\text{ mA}$) | $V_{OL(LVI)}$ | – | 0.15 | 0.4 | V |
| Output Off-State Leakage Current ($V_{OH} = 15\text{ V}$) | I_{OH} | – | 0.01 | 5.0 | μA |

TOTAL DEVICE

| | | | | | |
|---|----------|---|-----|----|----|
| Standby Supply Current ($V_{CC} = 2.5\text{ V}$ to 40 V , Pin 8 = V_{CC} , Pins 6, 14, 15 = GND, remaining pins open) | I_{CC} | – | 6.0 | 10 | mA |
|---|----------|---|-----|----|----|

- Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
- $T_{low} = 0^\circ\text{C}$ for MC34163
= -40°C for MC33163
- $T_{high} = +70^\circ\text{C}$ for MC34163
= $+85^\circ\text{C}$ for MC33163

MC34163, MC33163

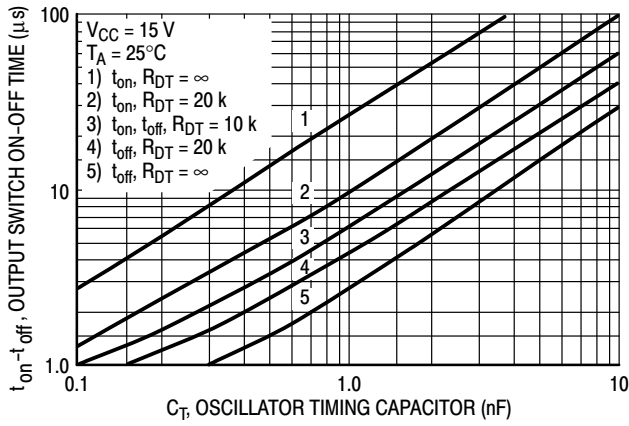


Figure 2. Output Switch On-Off Time versus Oscillator Timing Capacitor

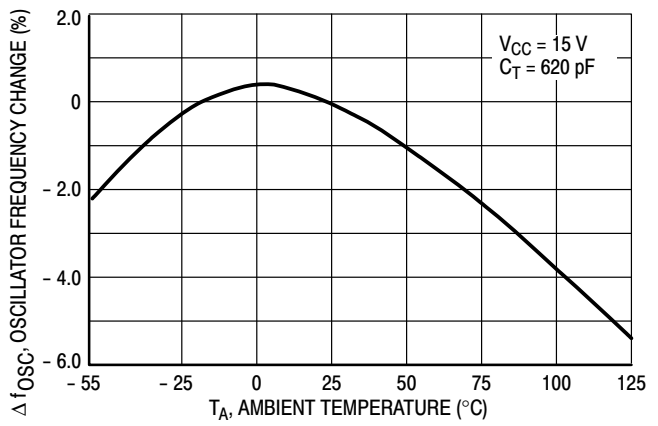


Figure 3. Oscillator Frequency Change versus Temperature

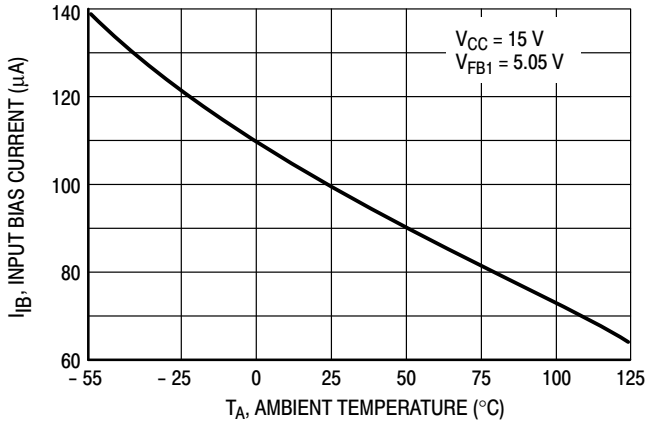


Figure 4. Feedback Comparator 1 Input Bias Current versus Temperature

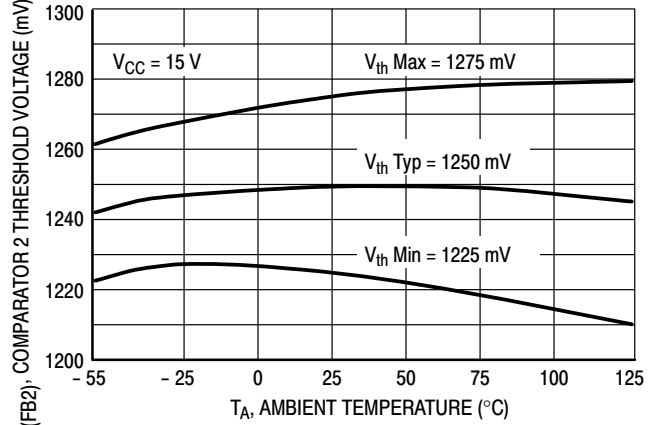


Figure 5. Feedback Comparator 2 Threshold Voltage versus Temperature

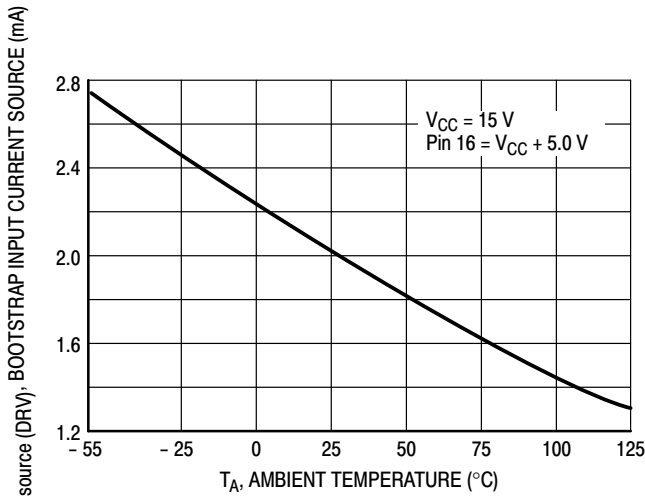


Figure 6. Bootstrap Input Current Source versus Temperature

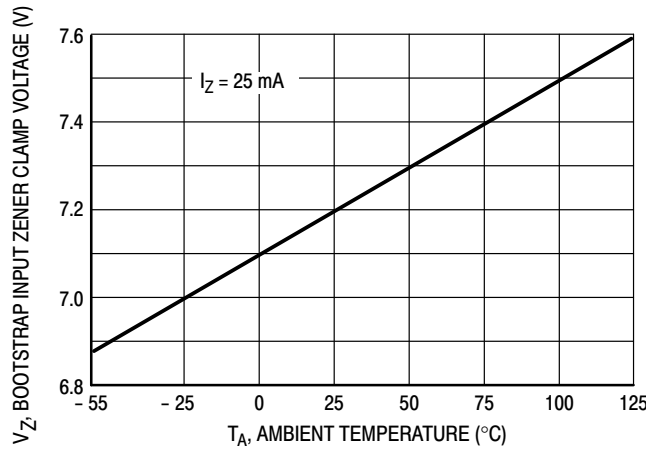


Figure 7. Bootstrap Input Zener Clamp Voltage versus Temperature

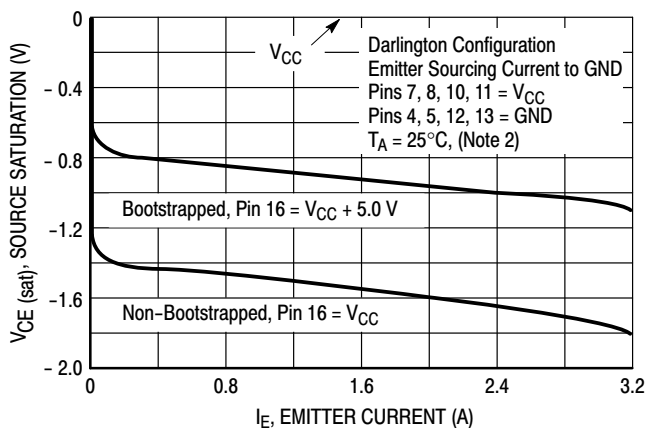


Figure 8. Output Switch Source Saturation versus Emitter Current

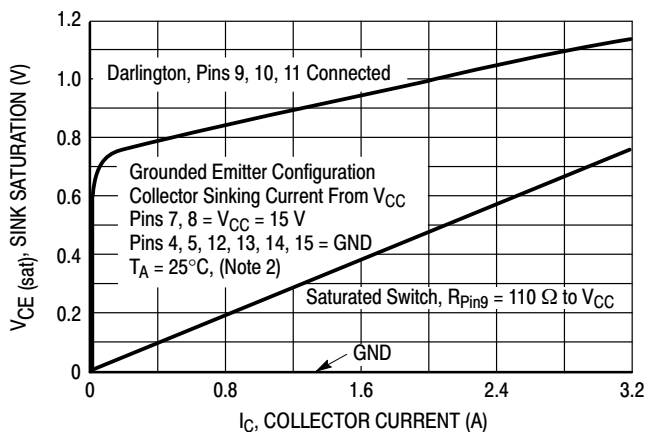


Figure 9. Output Switch Sink Saturation versus Collector Current

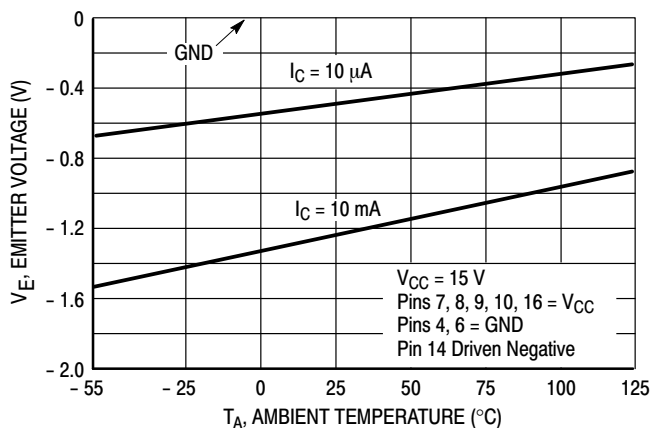


Figure 10. Output Switch Negative Emitter Voltage versus Temperature

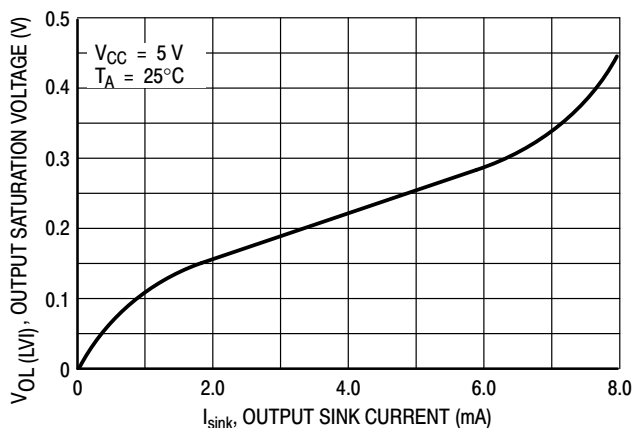


Figure 11. Low Voltage Indicator Output Sink Saturation Voltage versus Sink Current

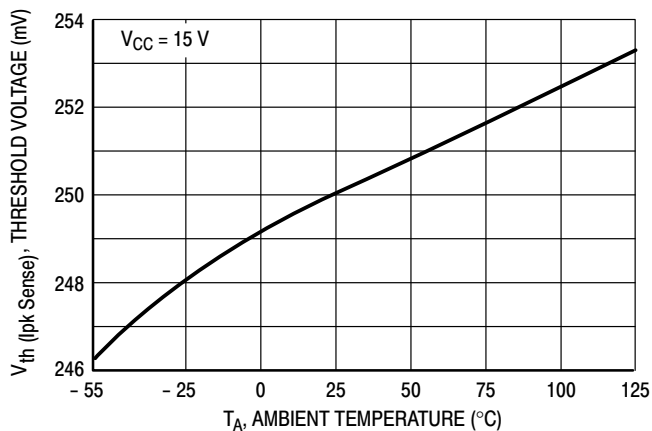


Figure 12. Current Limit Comparator Threshold Voltage versus Temperature

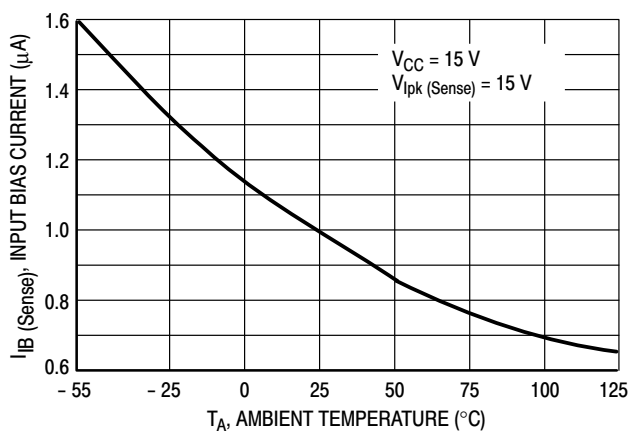


Figure 13. Current Limit Comparator Input Bias Current versus Temperature

MC34163, MC33163

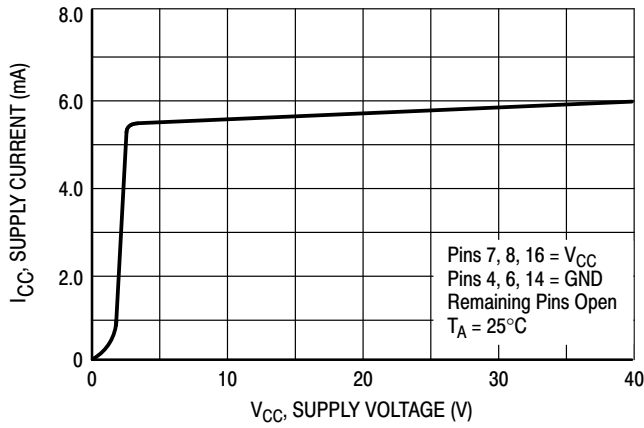


Figure 14. Standby Supply Current versus Supply Voltage

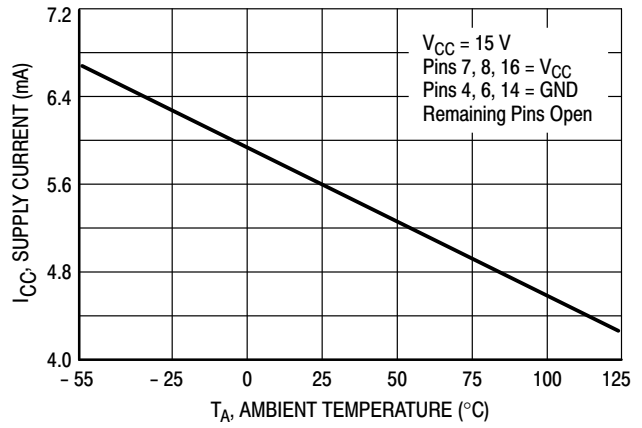


Figure 15. Standby Supply Current versus Temperature

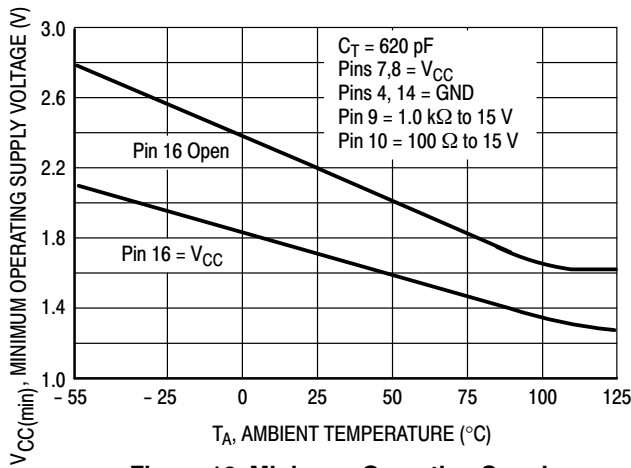


Figure 16. Minimum Operating Supply Voltage versus Temperature

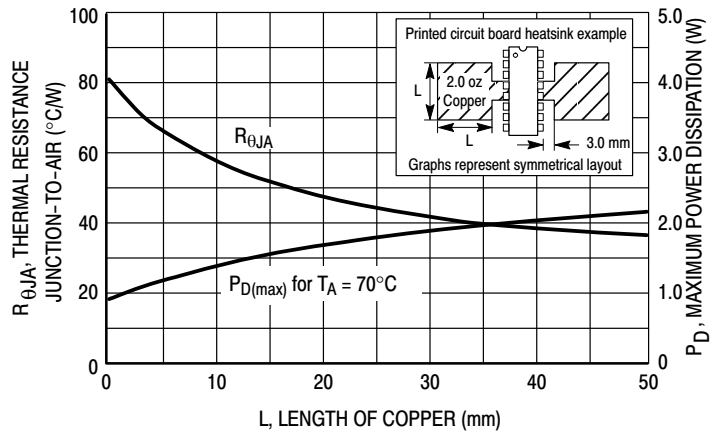


Figure 17. P Suffix (DIP-16) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

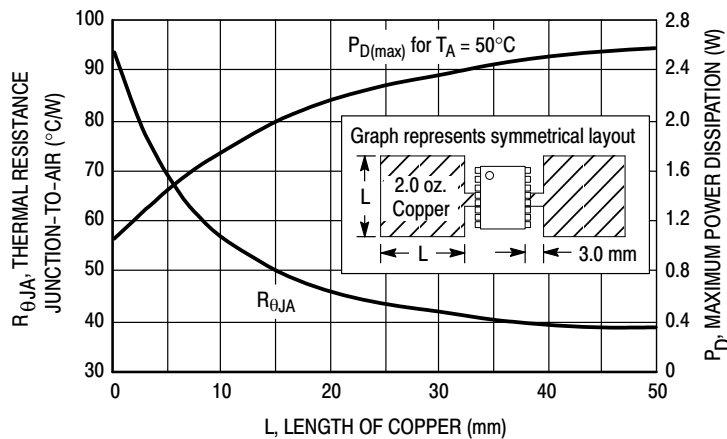


Figure 18. DW Suffix (SOP-16L) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

MC34163, MC33163

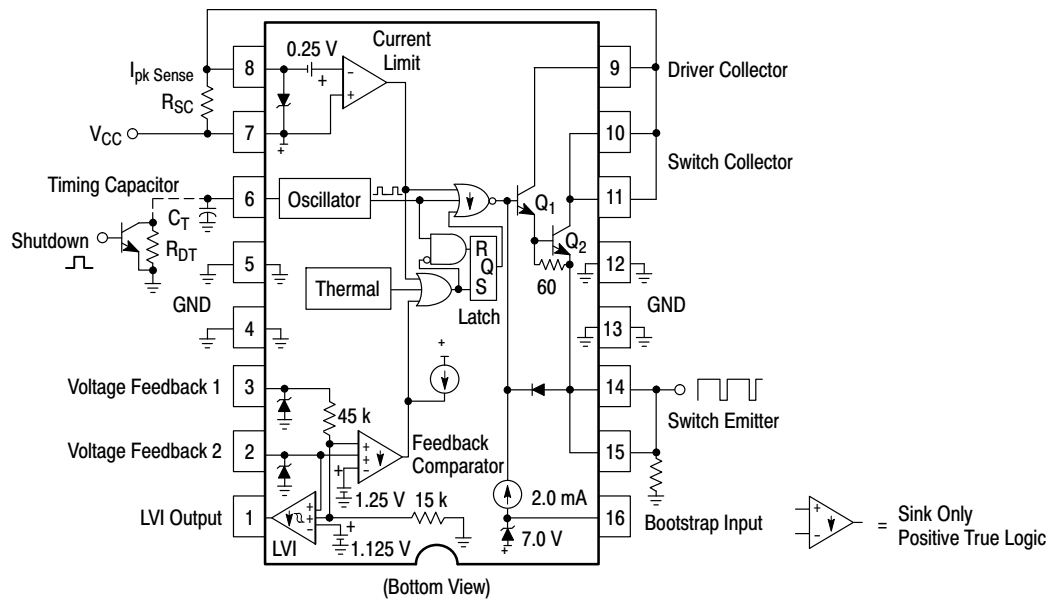


Figure 19. Representative Block Diagram

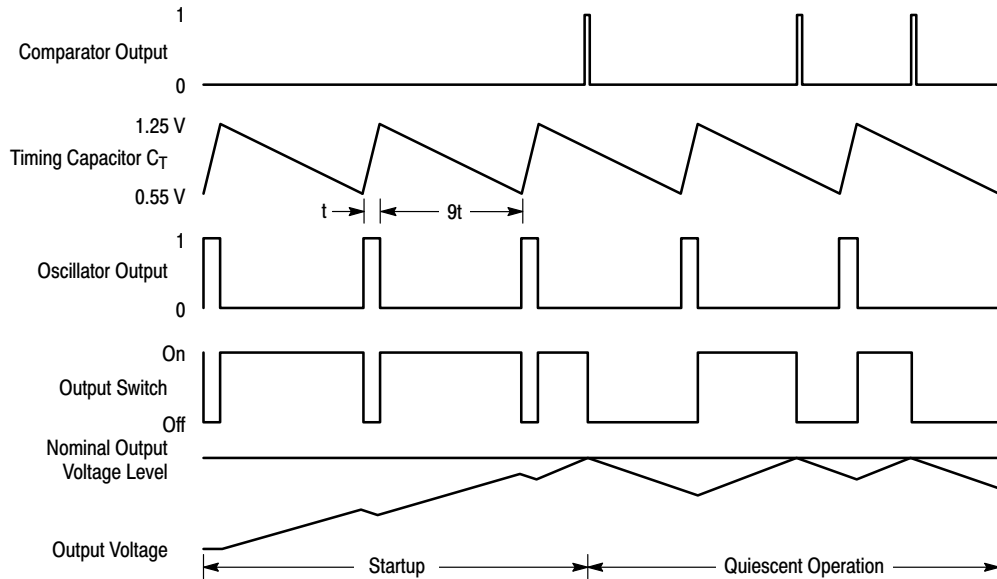


Figure 20. Typical Operating Waveforms

INTRODUCTION

The MC34163 series are monolithic power switching regulators optimized for dc-to-dc converter applications. The combination of features in this series enables the system designer to directly implement step-up, step-down, and voltage-inverting converters with a minimum number of external components. Potential applications include cost sensitive consumer products as well as equipment for the automotive, computer, and industrial markets. A Representative Block Diagram is shown in Figure 19.

OPERATING DESCRIPTION

The MC34163 operates as a fixed on-time, variable off-time voltage mode ripple regulator. In general, this mode of operation is somewhat analogous to a capacitor charge pump and does not require dominant pole loop compensation for converter stability. The Typical Operating Waveforms are shown in Figure 20. The output voltage waveform shown is for a step-down converter with the ripple and phasing exaggerated for clarity. During initial converter startup, the feedback comparator senses that the output voltage level is below nominal. This causes the output switch to turn on and off at a frequency and duty cycle controlled by the oscillator, thus pumping up the output filter capacitor. When the output voltage level reaches nominal, the feedback comparator sets the latch, immediately terminating switch conduction. The feedback comparator will inhibit the switch until the load current causes the output voltage to fall below nominal. Under these conditions, output switch conduction can be inhibited for a partial oscillator cycle, a partial cycle plus a complete cycle, multiple cycles, or a partial cycle plus multiple cycles.

Oscillator

The oscillator frequency and on-time of the output switch are programmed by the value selected for timing capacitor C_T . Capacitor C_T is charged and discharged by a 9 to 1 ratio internal current source and sink, generating a negative going sawtooth waveform at Pin 6. As C_T charges, an internal pulse is generated at the oscillator output. This pulse is connected to the NOR gate center input, preventing output switch conduction, and to the AND gate upper input, allowing the latch to be reset if the comparator output is low. Thus, the output switch is always disabled during ramp-up and can be enabled by the comparator output only at the start of ramp-down. The oscillator peak and valley thresholds are 1.25 V and 0.55 V, respectively, with a charge current of 225 μA and a discharge current of 25 μA , yielding a maximum on-time duty cycle of 90%. A reduction of the maximum duty cycle may be required for specific converter configurations. This can be accomplished with the addition of an external deadtime resistor (R_{DT}) placed across C_T . The

resistor increases the discharge current which reduces the on-time of the output switch. A graph of the Output Switch On-Off Time versus Oscillator Timing Capacitance for various values of R_{DT} is shown in Figure 2. Note that the maximum output duty cycle, $t_{on}/t_{on} + t_{off}$, remains constant for values of C_T greater than 0.2 nF. The converter output can be inhibited by clamping C_T to ground with an external NPN small-signal transistor.

Feedback and Low Voltage Indicator Comparators

Output voltage control is established by the Feedback comparator. The inverting input is internally biased at 1.25 V and is not pinned out. The converter output voltage is typically divided down with two external resistors and monitored by the high impedance noninverting input at Pin 2. The maximum input bias current is $\pm 0.4 \mu\text{A}$, which can cause an output voltage error that is equal to the product of the input bias current and the upper divider resistance value. For applications that require 5.0 V, the converter output can be directly connected to the noninverting input at Pin 3. The high impedance input, Pin 2, must be grounded to prevent noise pickup. The internal resistor divider is set for a nominal voltage of 5.05 V. The additional 50 mV compensates for a 1.0% voltage drop in the cable and connector from the converter output to the load. The Feedback comparator's output state is controlled by the highest voltage applied to either of the two noninverting inputs.

The Low Voltage Indicator (LVI) comparator is designed for use as a reset controller in microprocessor-based systems. The inverting input is internally biased at 1.125 V, which sets the noninverting input thresholds to 90% of nominal. The LVI comparator has 15 mV of hysteresis to prevent erratic reset operation. The Open Collector output is capable of sinking in excess of 6.0 mA (see Figure 11). An external resistor (R_{LVI}) and capacitor (C_{DLY}) can be used to program a reset delay time (t_{DLY}) by the formula shown below, where $V_{th(MPU)}$ is the microprocessor reset input threshold. Refer to Figure 21.

$$t_{DLY} = R_{LVI} C_{DLY} \ln \left(\frac{1}{1 - \frac{V_{th(MPU)}}{V_{out}}} \right)$$

Current Limit Comparator, Latch and Thermal Shutdown

With a voltage mode ripple converter operating under normal conditions, output switch conduction is initiated by the oscillator and terminated by the Voltage Feedback comparator. Abnormal operating conditions occur when the converter output is overloaded or when feedback voltage sensing is lost. Under these conditions, the Current Limit comparator will protect the Output Switch.

The switch current is converted to a voltage by inserting a fractional ohm resistor, R_{SC} , in series with V_{CC} and output switch transistor Q_2 . The voltage drop across R_{SC} is monitored by the Current Sense comparator. If the voltage drop exceeds 250 mV with respect to V_{CC} , the comparator will set the latch and terminate output switch conduction on a cycle-by-cycle basis. This Comparator/Latch configuration ensures that the Output Switch has only a single on-time during a given oscillator cycle. The calculation for a value of R_{SC} is:

$$R_{SC} = \frac{0.25 \text{ V}}{I_{pk} (\text{Switch})}$$

Figures 12 and 13 show that the Current Sense comparator threshold is tightly controlled over temperature and has a typical input bias current of 1.0 μA . The propagation delay from the comparator input to the Output Switch is typically 200 ns. The parasitic inductance associated with R_{SC} and the circuit layout should be minimized. This will prevent unwanted voltage spikes that may falsely trip the Current Limit comparator.

Internal thermal shutdown circuitry is provided to protect the IC in the event that the maximum junction temperature is exceeded. When activated, typically at 170°C, the Latch is forced into the “Set” state, disabling the Output Switch. This feature is provided to prevent catastrophic failures from accidental device overheating. It is not intended to be used as a replacement for proper heatsinking.

Driver and Output Switch

To aid in system design flexibility and conversion efficiency, the driver current source and collector, and output switch collector and emitter are pinned out separately. This allows the designer the option of driving the output switch into saturation with a selected force gain or driving it near saturation when connected as a Darlington. The output switch has a typical current gain of 70 at 2.5 A and is designed to switch a maximum of 40 V collector to emitter, with up to 3.4 A peak collector current. The minimum value for R_{SC} is:

$$R_{SC(\text{min})} = \frac{0.25 \text{ V}}{3.4 \text{ A}} = 0.0735 \Omega$$

When configured for step-down or voltage-inverting applications, as in Figures 21 and 25, the inductor will forward bias the output rectifier when the switch turns off. Rectifiers with a high forward voltage drop or long turn-on delay time should not be used. If the emitter is allowed to go sufficiently negative, collector current will flow, causing

additional device heating and reduced conversion efficiency.

Figure 10 shows that by clamping the emitter to 0.5 V, the collector current will be in the range 10 μA over temperature. A 1N5822 or equivalent Schottky barrier rectifier is recommended to fulfill these requirements.

A bootstrap input is provided to reduce the output switch saturation voltage in step-down and voltage-inverting converter applications. This input is connected through a series resistor and capacitor to the switch emitter and is used to raise the internal 2.0 mA bias current source above V_{CC} . An internal zener limits the bootstrap input voltage to $V_{CC} + 7.0 \text{ V}$. The capacitor's equivalent series resistance must limit the zener current to less than 100 mA. An additional series resistor may be required when using tantalum or other low ESR capacitors. The equation below is used to calculate a minimum value bootstrap capacitor based on a minimum zener voltage and an upper limit current source.

$$C_{B(\text{min})} = I \frac{\Delta t}{\Delta V} = 4.0 \text{ mA} \frac{t_{on}}{4.0 \text{ V}} = 0.001 t_{on}$$

Parametric operation of the MC34163 is guaranteed over a supply voltage range of 2.5 V to 40 V. When operating below 3.0 V, the Bootstrap Input should be connected to V_{CC} . Figure 16 shows that functional operation down to 1.7 V at room temperature is possible.

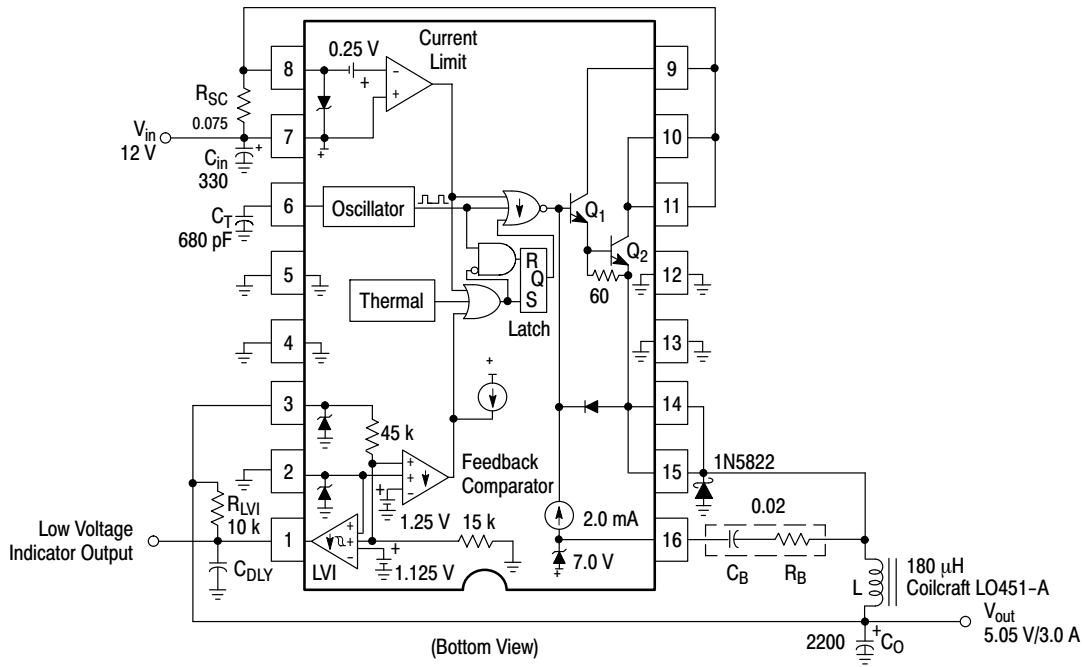
Package

The MC34163 is contained in a heatsinkable 16-lead plastic dual-in-line package in which the die is mounted on a special heat tab copper alloy lead frame. This tab consists of the four center ground pins that are specifically designed to improve thermal conduction from the die to the circuit board. Figures 17 and 18 show a simple and effective method of utilizing the printed circuit board medium as a heat dissipater by soldering these pins to an adequate area of copper foil. This permits the use of standard layout and mounting practices while having the ability to halve the junction-to-air thermal resistance. These examples are for a symmetrical layout on a single-sided board with two ounce per square foot of copper.

APPLICATIONS

The following converter applications show the simplicity and flexibility of this circuit architecture. Three main converter topologies are demonstrated with actual test data shown below each of the circuit diagrams.

MC34163, MC33163



| Test | Condition | Results |
|-------------------------------|--|-----------------------------|
| Line Regulation | $V_{in} = 8.0 \text{ V to } 24 \text{ V}, I_O = 3.0 \text{ A}$ | $6.0 \text{ mV} \pm 0.06\%$ |
| Load Regulation | $V_{in} = 12 \text{ V}, I_O = 0.6 \text{ A to } 3.0 \text{ A}$ | $2.0 \text{ mV} \pm 0.02\%$ |
| Output Ripple | $V_{in} = 12 \text{ V}, I_O = 3.0 \text{ A}$ | 36 mVpp |
| Short Circuit Current | $V_{in} = 12 \text{ V}, R_L = 0.1 \Omega$ | 3.3 A |
| Efficiency, Without Bootstrap | $V_{in} = 12 \text{ V}, I_O = 3.0 \text{ A}$ | 76.7% |
| Efficiency, With Bootstrap | $V_{in} = 12 \text{ V}, I_O = 3.0 \text{ A}$ | 81.2% |

Figure 21. Step-Down Converter

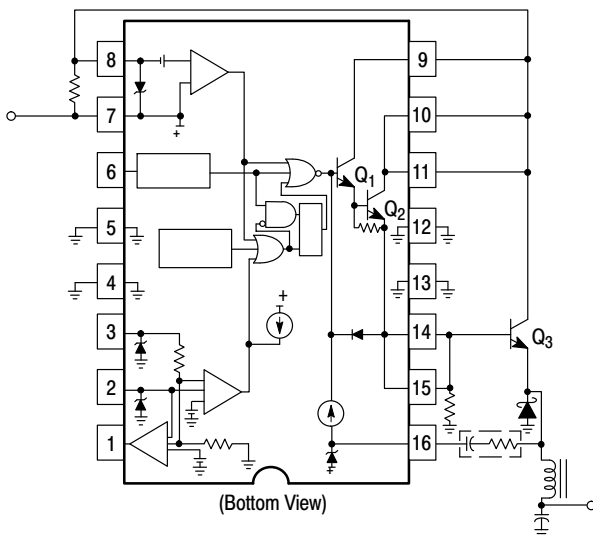


Figure 22A. External NPN Switch

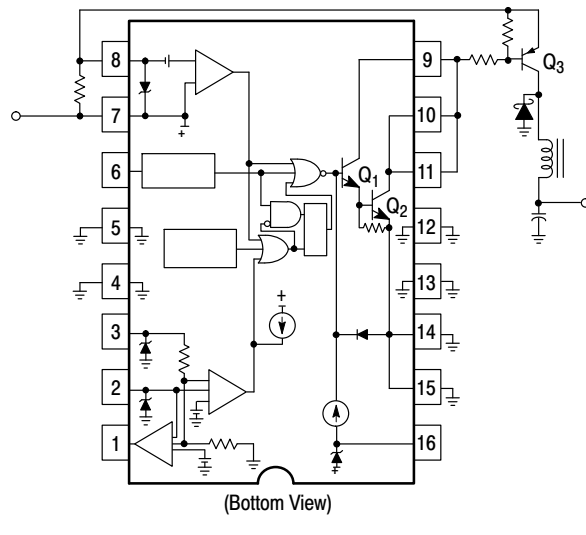
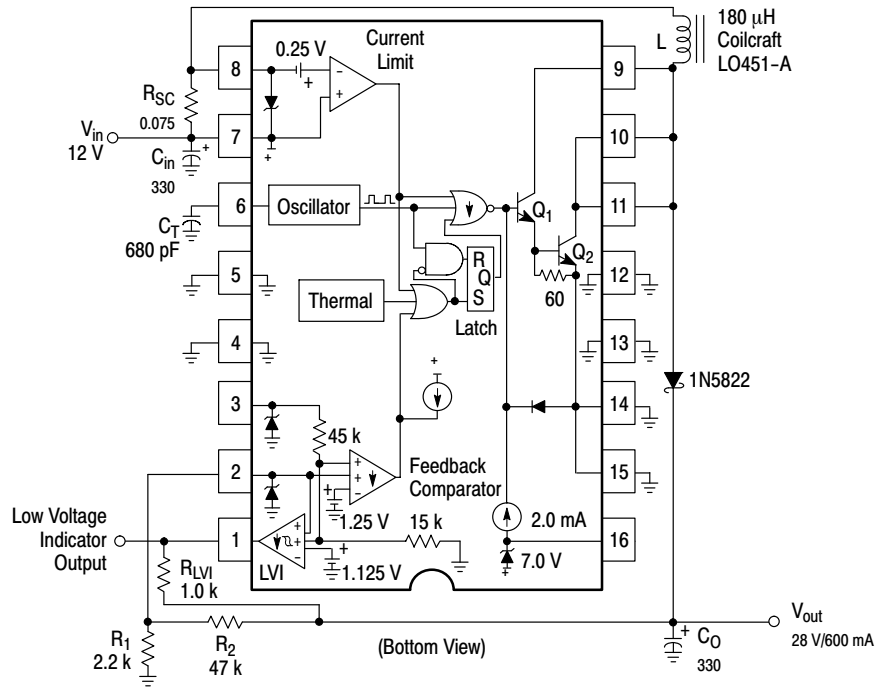


Figure 22B. External PNP Saturated Switch

Figure 22. External Current Boost Connections for $I_{pk}(\text{Switch})$ Greater Than 3.4 A

MC34163, MC33163



| Test | Condition | Results |
|-----------------|--|----------------------------|
| Line Regulation | $V_{in} = 9.0 \text{ V to } 16 \text{ V}, I_O = 0.6 \text{ A}$ | $30 \text{ mV} \pm 0.05\%$ |
| Load Regulation | $V_{in} = 12 \text{ V}, I_O = 0.1 \text{ A to } 0.6 \text{ A}$ | $50 \text{ mV} \pm 0.09\%$ |
| Output Ripple | $V_{in} = 12 \text{ V}, I_O = 0.6 \text{ A}$ | 140 mVpp |
| Efficiency | $V_{in} = 12 \text{ V}, I_O = 0.6 \text{ A}$ | 88.1% |

Figure 23. Step-Up Converter

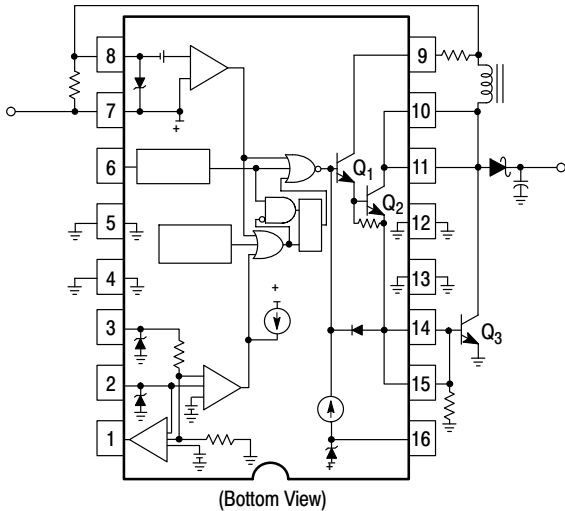


Figure 24A. External NPN Switch

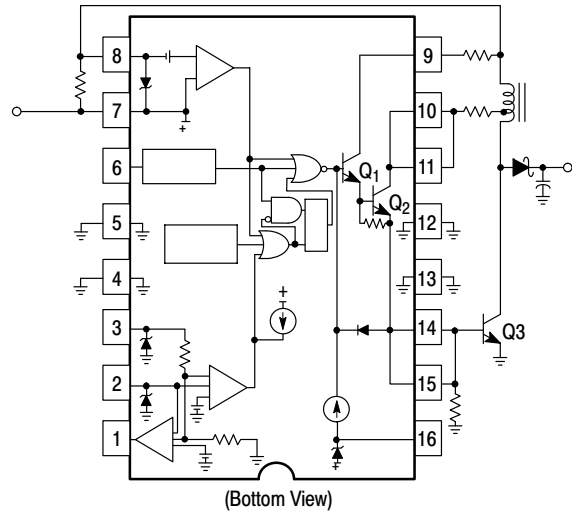
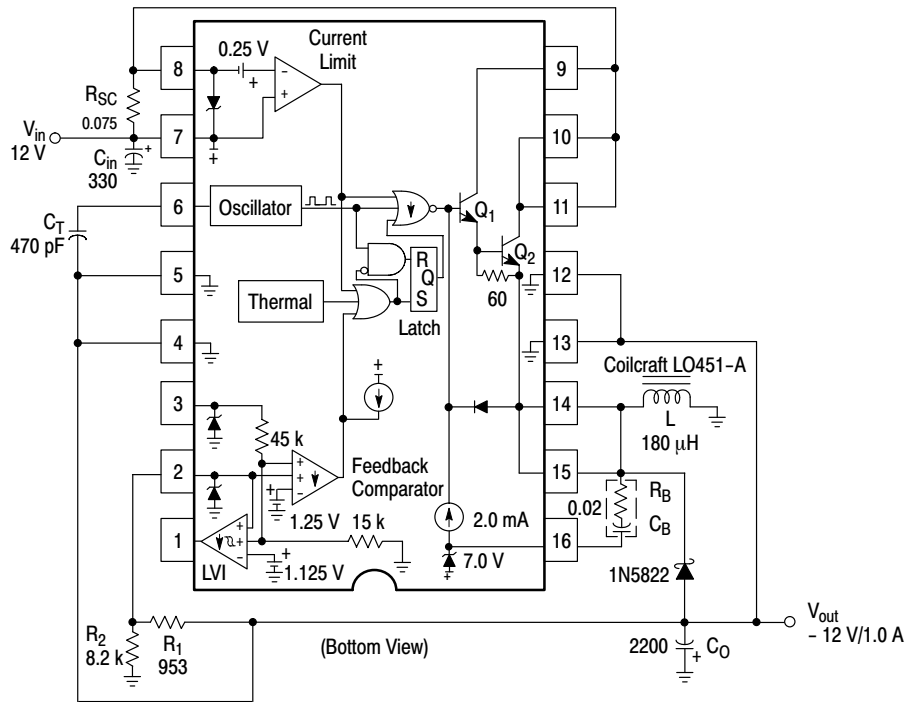


Figure 24B. External NPN Saturated Switch

Figure 24. External Current Boost Connections for $I_{pk} \text{ (Switch)}$ Greater Than 3.4 A

MC34163, MC33163



| Test | Condition | Results |
|-------------------------------|--|-------------------------------|
| Line Regulation | $V_{in} = 9.0 \text{ V to } 16 \text{ V}, I_O = 1.0 \text{ A}$ | $5.0 \text{ mV} = \pm 0.02\%$ |
| Load Regulation | $V_{in} = 12 \text{ V}, I_O = 0.6 \text{ A to } 1.0 \text{ A}$ | $2.0 \text{ mV} = \pm 0.01\%$ |
| Output Ripple | $V_{in} = 12 \text{ V}, I_O = 1.0 \text{ A}$ | 130 mVpp |
| Short Circuit Current | $V_{in} = 12 \text{ V}, R_L = 0.1 \Omega$ | 3.2 A |
| Efficiency, Without Bootstrap | $V_{in} = 12 \text{ V}, I_O = 1.0 \text{ A}$ | 73.1% |
| Efficiency, With Bootstrap | $V_{in} = 12 \text{ V}, I_O = 1.0 \text{ A}$ | 77.5% |

Figure 25. Voltage-Inverting Converter

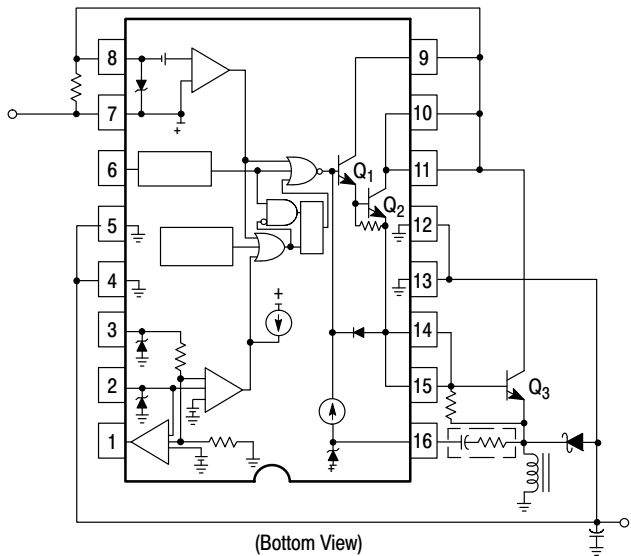


Figure 26A. External NPN Switch

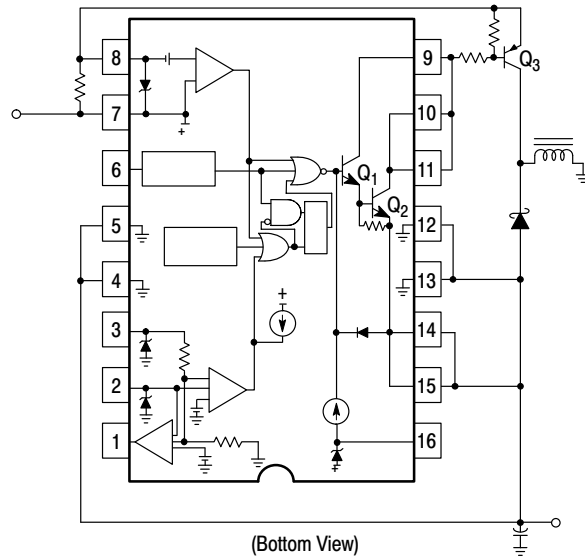
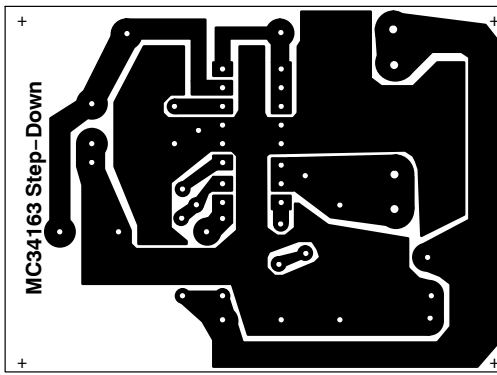


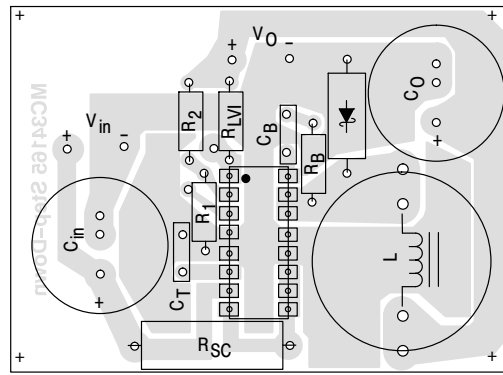
Figure 26B. External PNP Saturated Switch

Figure 26. External Current Boost Connections for $I_{pk} \text{ (Switch)}$ Greater Than 3.4 A

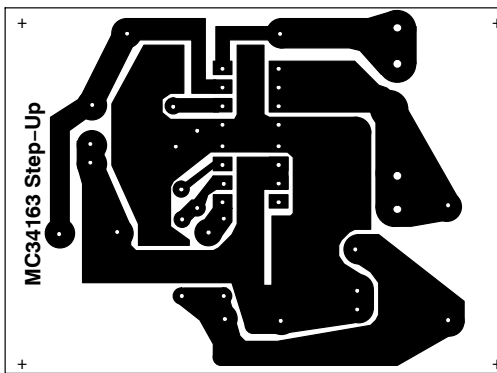
MC34163, MC33163



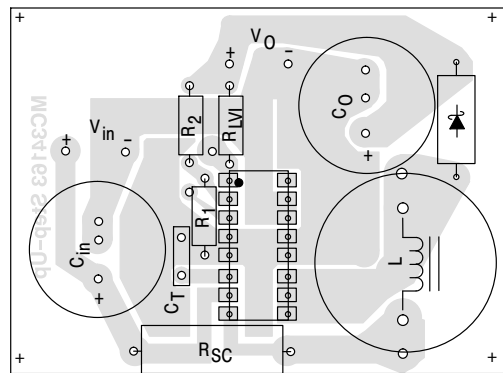
Bottom View



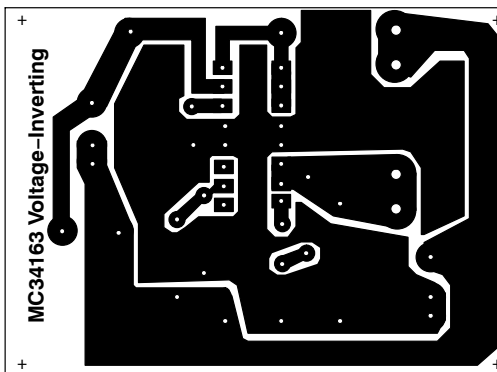
Top View



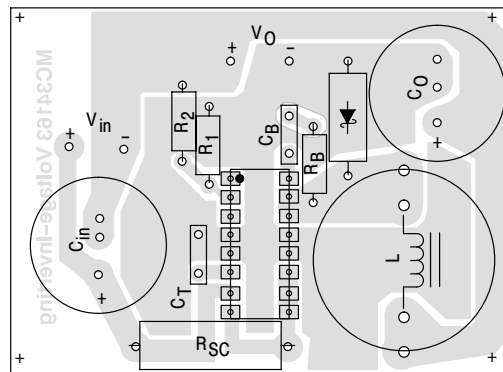
Bottom View



Top View



Bottom View



Top View

All printed circuit boards are 2.58" in width by 1.9" in height.

Figure 27. Printed Circuit Board and Component Layout
(Circuits of Figures 21, 23, 25)

MC34163, MC33163

| Calculation | Step-Down | Step-Up | Voltage-Inverting |
|---------------------------|---|---|---|
| t_{on} (Notes 2, 3) | $\frac{V_{out} + V_F}{V_{in} - V_{sat} - V_{out}}$ | $\frac{V_{out} + V_F \cdot V_{in}}{V_{in} \cdot V_{sat}}$ | $\frac{ V_{out} + V_F}{V_{in} - V_{sat}}$ |
| t_{on} | $\frac{t_{on}}{t_{off}}$ $f \left(\frac{t_{on}}{t_{off}} + 1 \right)$ | $\frac{t_{on}}{t_{off}}$ $f \left(\frac{t_{on}}{t_{off}} + 1 \right)$ | $\frac{t_{on}}{t_{off}}$ $f \left(\frac{t_{on}}{t_{off}} + 1 \right)$ |
| C_T | $\frac{32.143 \cdot 10^6}{f}$ | $\frac{32.143 \cdot 10^6}{f}$ | $\frac{32.143 \cdot 10^6}{f}$ |
| $I_{L(av)}$ | I_{out} | $I_{out} \left(\frac{t_{on}}{t_{off}} + 1 \right)$ | $I_{out} \left(\frac{t_{on}}{t_{off}} + 1 \right)$ |
| $I_{pk} \text{ (Switch)}$ | $I_{L(av)} + \frac{\Delta I_L}{2}$ | $I_{L(av)} + \frac{\Delta I_L}{2}$ | $I_{L(av)} + \frac{\Delta I_L}{2}$ |
| RSC | $\frac{0.25}{I_{pk} \text{ (Switch)}}$ | $\frac{0.25}{I_{pk} \text{ (Switch)}}$ | $\frac{0.25}{I_{pk} \text{ (Switch)}}$ |
| L | $\left(\frac{V_{in} - V_{sat} - V_{out}}{\Delta I_L} \right) t_{on}$ | $\left(\frac{V_{in} - V_{sat}}{\Delta I_L} \right) t_{on}$ | $\left(\frac{V_{in} - V_{sat}}{\Delta I_L} \right) t_{on}$ |
| $V_{ripple(pp)}$ | $\Delta I_L \sqrt{\left(\frac{1}{8 \cdot f C_O} \right)^2 + (ESR)^2}$ | $\approx \frac{t_{on} I_{out}}{C_O}$ | $\approx \frac{t_{on} I_{out}}{C_O}$ |
| V_{out} | $V_{ref} \left(\frac{R_2}{R_1} + 1 \right)$ | $V_{ref} \left(\frac{R_2}{R_1} + 1 \right)$ | $V_{ref} \left(\frac{R_2}{R_1} + 1 \right)$ |

The following Converter Characteristics must be chosen:

- V_{in} – Nominal operating input voltage.
- V_{out} – Desired output voltage.
- I_{out} – Desired output current.
- ΔI_L – Desired peak-to-peak inductor ripple current. For maximum output current it is suggested that ΔI_L be chosen to be less than 10% of the average inductor current $I_{L(av)}$. This will help prevent $I_{pk} \text{ (Switch)}$ from reaching the current limit threshold set by R_{SC} . If the design goal is to use a minimum inductance value, let $\Delta I_L = 2(I_{L(av)})$. This will proportionally reduce converter output current capability.
- f – Maximum output switch frequency.
- $V_{ripple(pp)}$ – Desired peak-to-peak output ripple voltage. For best performance the ripple voltage should be kept to a low value since it will directly affect line and load regulation. Capacitor C_O should be a low equivalent series resistance (ESR) electrolytic designed for switching regulator applications.

- NOTES:**
1. V_{sat} – Saturation voltage of the output switch, refer to Figures 8 and 9.
 2. V_F – Output rectifier forward voltage drop. Typical value for 1N5822 Schottky barrier rectifier is 0.5 V.
 3. The calculated t_{on}/t_{off} must not exceed the minimum guaranteed oscillator charge to discharge ratio of 8, at the minimum operating input voltage.

Figure 28. Design Equations

MECHANICAL CASE OUTLINE

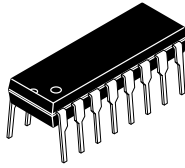
PACKAGE DIMENSIONS

ON Semiconductor®

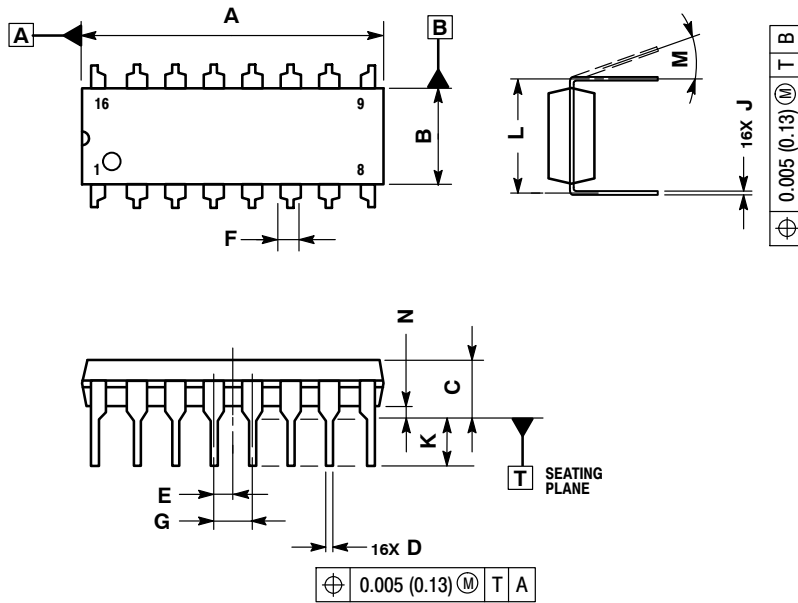


PDIP CASE 648C-04 ISSUE D

DATE 07/28/1998



SCALE 1:1



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.744 | 0.783 | 18.90 | 19.90 |
| B | 0.240 | 0.260 | 6.10 | 6.60 |
| C | 0.145 | 0.185 | 3.69 | 4.69 |
| D | 0.015 | 0.021 | 0.38 | 0.53 |
| E | 0.050 BSC | | 1.27 BSC | |
| F | 0.040 | 0.70 | 1.02 | 1.78 |
| G | 0.100 BSC | | 2.54 BSC | |
| J | 0.008 | 0.015 | 0.20 | 0.38 |
| K | 0.115 | 0.135 | 2.92 | 3.43 |
| L | 0.300 BSC | | 7.62 BSC | |
| M | 0° | 10° | 0° | 10° |
| N | 0.015 | 0.040 | 0.39 | 1.01 |

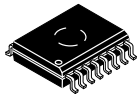
| | | |
|-------------------------|--------------------|---|
| DOCUMENT NUMBER: | 98ASB42434B | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | PDIP | PAGE 1 OF 1 |

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

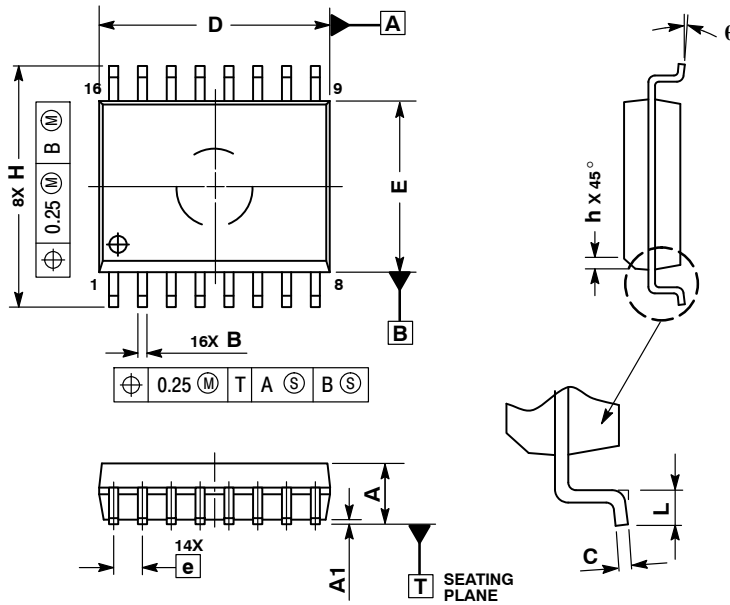
ON Semiconductor®



1
SCALE 1:1

SOIC-16 WB
CASE 751G-03
ISSUE D

DATE 12 FEB 2013

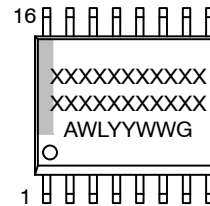


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

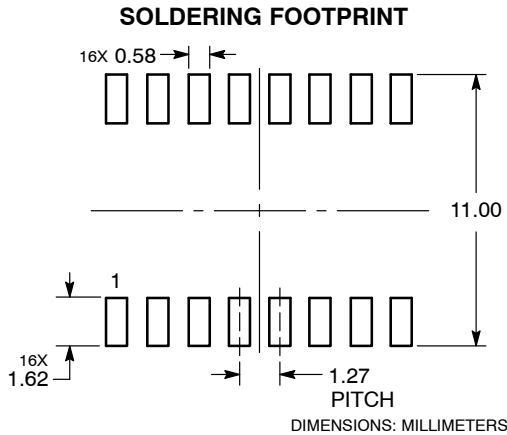
| MILLIMETERS | | |
|-------------|----------|-------|
| DIM | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| B | 0.35 | 0.49 |
| C | 0.23 | 0.32 |
| D | 10.15 | 10.45 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| q | 0° | 7° |

GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.



| | | |
|-------------------------|--------------------|--|
| DOCUMENT NUMBER: | 98ASB42567B | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | SOIC-16 WB | PAGE 1 OF 1 |

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Email Requests to: orderlit@onsemi.com

ON Semiconductor Website: www.onsemi.com

TECHNICAL SUPPORT

North American Technical Support:
Voice Mail: 1 800-282-9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative