

5V/3.3V ECL 1:2 Differential Fanout Buffer

Features

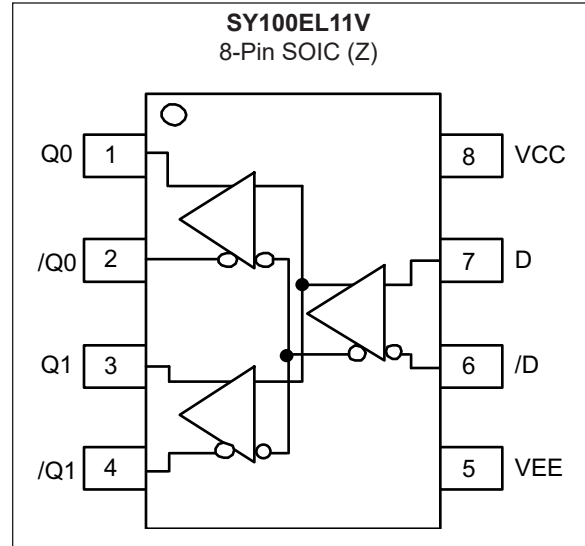
- 3.3V and 5V Power Supply Options
- 265 ps Propagation Delay (Typical)
- 5 ps Skew (Typical) Between Outputs
- High Bandwidth Output Transitions
- Internal 75 k Ω Input Pull-Down Resistors
- Replaces SY100EL11
- Improved Output Waveform Characteristics
- Available in 8-pin SOIC Package

General Description

The SY100EL11V is a 1:2 differential fanout gate. Having low within-device skews and output transition times, the EL11V is ideally suited for those applications that require the ultimate in AC performance.

The differential inputs of the EL11V employ clamping circuitry to maintain stability under open input conditions. If the inputs are left open (pulled to V_{EE}), the Q outputs will go low.

Package Type



SY100EL11V

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

PECL Power Supply Voltage (V_{CC}) (Note 1)	+8V
NECL Power Supply Voltage (V_{EE}) (Note 2)	-8V
PECL Mode Input Voltage (V_{IN}) (Note 3)	+6V
NECL Mode Input Voltage (V_{IN}) (Note 4)	-6V
Continuous Output Current (I_{OUT})	50 mA
Surge Output Current (I_{OUT})	100 mA
ESD Rating (Note 5)	>1.5 kV

† **Notice:** Stresses above those listed under “Absolute Maximum ratings” may cause permanent damage to the device. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: $V_{EE} = 0V$

2: $V_{CC} = 0V$

3: $V_{EE} = 0V, V_{IN} \leq V_{CC}$

4: $V_{CC} = 0V, V_{IN} \geq V_{EE}$

5: Human body model, 1.5 k Ω in series with 100 pF

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications PECL: $V_{CC} = 3.0V$ to $5.5V$; $V_{EE} = 0V$; $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise stated (Note 1)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply Current	I_{EE}	—	26	31	mA	$T_A = -40^\circ C$ to $+25^\circ C$
		—	30	36		$T_A = +85^\circ C$
Output High Voltage (Note 2)	V_{OH}	$V_{CC}-1.085$	$V_{CC}-1.005$	$V_{CC}-0.88$	V	$T_A = -40^\circ C$
		$V_{CC}-1.025$	$V_{CC}-0.955$	$V_{CC}-0.88$		$T_A = 0^\circ C$ to $+85^\circ C$
Output Low Voltage (Note 2)	V_{OL}	$V_{CC}-1.830$	$V_{CC}-1.695$	$V_{CC}-1.555$	V	$T_A = -40^\circ C$
		$V_{CC}-1.810$	$V_{CC}-1.705$	$V_{CC}-1.620$		$T_A = 0^\circ C$ to $+85^\circ C$
Input High Voltage (Single-Ended)	V_{IH}	$V_{CC}-1.165$	—	$V_{CC}-0.880$	V	—
Input Low Voltage (Single-Ended)	V_{IL}	$V_{CC}-1.810$	—	$V_{CC}-1.475$	V	—
Common Mode Range (Note 3)	V_{IHCMR}	2.0	—	$V_{CC}-0.4$	V	$T_A = -40^\circ C$
		1.9	—	$V_{CC}-0.4$		$T_A = 0^\circ C$ to $+85^\circ C$
Input High Current	I_{IH}	—	—	150	μA	—
Input Low Current	I_{IL}	0.5	—	—	μA	$V_{IN} = V_{IL(MIN)}$

Note 1: Devices are designed to meet the DC specifications shown in the above table after thermal equilibration has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lpm is maintained.

2: Outputs are terminated through a 50 Ω resistor to $V_{CC} - 2.0V$.

3: The CMR range is referenced to the most positive side of the differential input voltage. Normal operation is obtained if the high level falls within the specified range and the peak-to-peak voltage lies between 150 mV and 1V.

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications NECL: $V_{EE} = -5.5V$ to $-3.0V$; $V_{CC} = 0V$; $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise stated (Note 1)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply Current	I_{EE}	—	26	31	mA	$T_A = -40^\circ C$ to $+25^\circ C$
		—	30	36		$T_A = +85^\circ C$
Output High Voltage (Note 2)	V_{OH}	-1.085	-1.005	-0.88	V	$T_A = -40^\circ C$
		-1.025	-0.955	-0.88		$T_A = 0^\circ C$ to $+85^\circ C$
Output Low Voltage (Note 2)	V_{OL}	-1.830	-1.695	-1.555	V	$T_A = -40^\circ C$
		-1.810	-1.705	-1.620		$T_A = 0^\circ C$ to $+85^\circ C$
Input High Voltage (Single-Ended)	V_{IH}	-1.165	—	-0.880	V	—
Input Low Voltage (Single-Ended)	V_{IL}	-1.810	—	-1.475	V	—
Common Mode Range (Note 3)	V_{IHCMR}	$V_{EE} + 2.0$	—	-0.4	V	$T_A = -40^\circ C$
		$V_{EE} + 1.9$	—	-0.4		$T_A = 0^\circ C$ to $+85^\circ C$
Input High Current	I_{IH}	—	—	150	μA	—
Input Low Current	I_{IL}	0.5	—	—	μA	$V_{IN} = V_{IL(MIN)}$

- Note 1:** Devices are designed to meet the DC specifications shown in the above table after thermal equilibration has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.
- 2:** Outputs are terminated through a 50Ω resistor to $V_{CC}-2.0V$.
- 3:** The CMR range is referenced to the most positive side of the differential input voltage. Normal operation is obtained if the high level falls within the specified range and the peak-to-peak voltage lies between 150 mV and 1V.

AC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: $V_{CC} = 3.0V$ to $5.5V$; $V_{EE} = 0V$ or $V_{EE} = -5.5V$ to $-3.0V$; $V_{CC} = 0V$; $T_A = -40^\circ C$ to $85^\circ C$, unless otherwise stated

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Propagation Delay D to Q	t_{PLH} t_{PHL}	135	260	385	ps	$T_A = -40^\circ C$
		185	260	335		$T_A = 0^\circ C$
		190	265	340		$T_A = +25^\circ C$
		215	290	365		$T_A = +85^\circ C$
Within-Device Skew (Note 1)	t_{SKEW}	—	5	—	ps	$T_A = -40^\circ C$
Duty Cycle Skew (Note 2)		—	5	20		$T_A = 0^\circ C$ to $+85^\circ C$
		—	5	—		$T_A = -40^\circ C$
		—	5	20		$T_A = 0^\circ C$ to $+85^\circ C$
Additive Phase Jitter (RMS)	t_{JITTER}	—	28	—	f_{SRMS}	Carrier = 622 MHz, Integration Range: 12 kHz to 20 MHz, $T_A = +25^\circ C$
Input Swing (Note 3)	V_{PP}	150	—	1000	mV	—
Output Rise/Fall Times Q (20% to 80%)	t_r/t_f	100	225	350	ps	—

- Note 1:** Within-device skew defined as identical transitions on similar paths through a device.
- 2:** Duty cycle skew is the difference between a t_{PLH} and t_{PHL} propagation delay through a device.
- 3:** Input swing for which AC parameters are ensured. The device has a DC gain of 40.

SY100EL11V

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Temperature Range	T_A	-40	—	+85	°C	—
Storage Temperature Range	T_S	-65	—	+150	°C	—
Lead Temperature	T_{LEAD}	—	—	+260	°C	Soldering, 20 sec.
Thermal Resistance						
Junction-to-Ambient	θ_{JA}	—	160	—	°C/W	Still-Air
		—	109	—		500 lfpm
Junction-to-Case	θ_{JC}	—	39	—	°C/W	—

2.0 TYPICAL PERFORMANCE CURVES

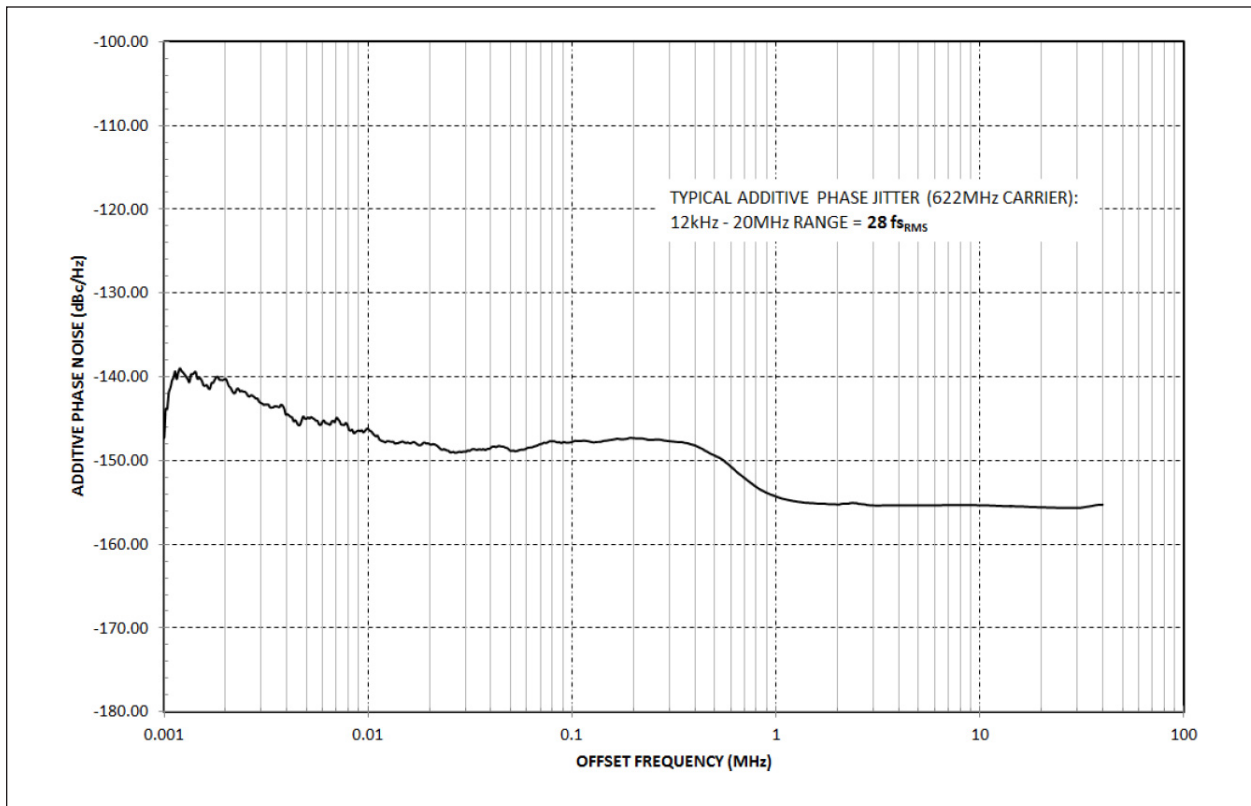


FIGURE 2-1: Additive Phase Noise Plot ($V_{CC} = 3.3V$, $T_A = +25^{\circ}C$)

SY100EL11V

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 3-1](#).

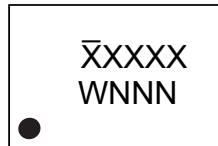
TABLE 3-1: PIN FUNCTION TABLE

Pin Name	Description
D	Data inputs
Q0, Q1	Data outputs
VCC	Positive power supply
VEE	Negative power supply

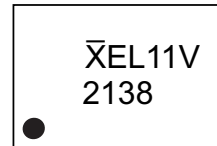
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

8-Lead SOIC*



Example



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
	•, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (̄) and/or Overbar (̂) symbol may not be to scale.	

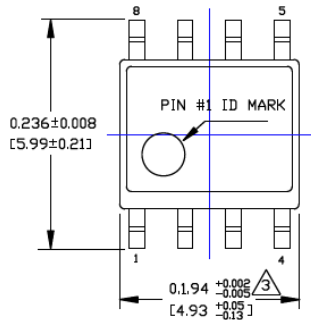
SY100EL11V

8-Lead SOIC Package Outline and Recommended Land Pattern

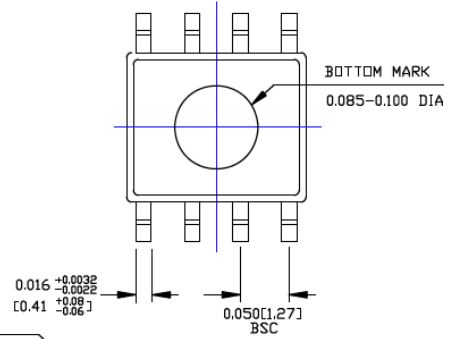
TITLE

8 LEAD SOICN PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

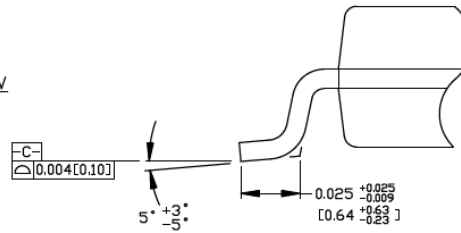
DRAWING #	SOICN-8LD-PL-1	UNIT	INCH [MM]
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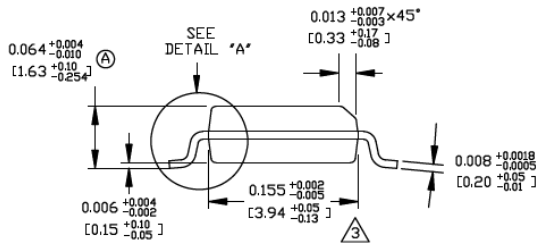
TOP VIEW



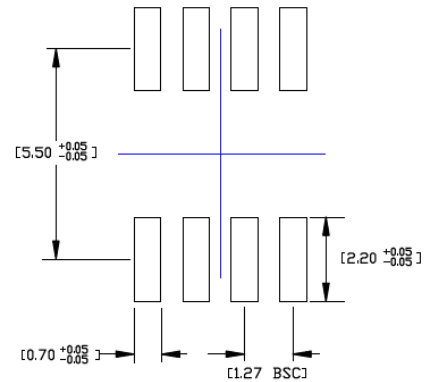
BOTTOM VIEW



DETAIL "A"



END VIEW



RECOMMENDED LAND PATTERN

NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.010[0.25] PER SIDE.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.

APPENDIX A: REVISION HISTORY

Revision A (October 2018)

- Converted Micrel document SY100EL11V to Microchip data sheet DS20006087A.
- Minor text changes throughout.
- Removed all reference to the EOL SY10EL11V version.

Revision B (August 2019)

- Updated minimum values for Common Mode Range voltage in PECL DC Electrical Characteristics table and NECL DC Electrical Characteristics table.
- Updated two Conditions values for t_{SKEW} in AC Electrical Characteristics table.
- Minor stylistic updates to align data sheet with current style.

SY100EL11V

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>PART NO.</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>-XX</u>
Device	Supply Voltage	Package	Temperature Range	Special Processing
Device:	SY100EL11: 5V/3.3V ECL 1:2 Differential Fanout Buffer			
Supply Voltage Range:	V	=	3.3V/5V	
Package:	Z	=	8-Lead SOIC	
Temperature Range:	G	=	-40°C to +85°C (Pb-Free NiPdAu)	
Special Processing:	<blank>	=	95/Tube	
	TR	=	1,000/Reel	

Examples:	
a) SY100EL11VZG:	SY100EL11, 3.3V/5V, 8-Lead SOIC, -40°C to +85°C (Pb-Free NiPdAu), 95/Tube
b) SY100EL11VZG-TR:	SY100EL11, 3.3V/5V, 8-Lead SOIC, -40°C to +85°C (Pb-Free NiPdAu), 1,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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