Click here for production status of specific part numbers.

MAX9939

SPI Programmable-Gain Amplifier with Input V_{OS} Trim and Output Op Amp

General Description

The MAX9939 is a general-purpose, differential-input programmable-gain amplifier (PGA) that is ideal for conditioning a variety of wide dynamic range signals such as those found in motor current-sense, medical instrumentation, and sonar data acquisition applications. It features programmable differential gains from 0.2V/V to 157V/V, input offset-voltage compensation, and an output amplifier that can be configured either as a high-order active filter or to provide a differential output.

The PGA is optimized for high-signal bandwidth and its gain can be programmed to be 0.2V/V, 1V/V, 10V/V, 20V/V, 30V/V, 40V/V, 60V/V, 80V/V, 119V/V, and 157V/V. Precision resistor matching provides extremely low gain tempco and high CMRR. Although the MAX9939 operates from a single supply V_{CC} between 2.9V to 5.5V, it can process signals both above and below ground due to the use of an input level-shifting amplifier stage. Furthermore, its inputs are protected to ±16V, allowing it to withstand fault conditions and signal overranges.

The output amplifier is designed for high bandwidth and low-bias currents, making it ideal for use in multiple-feedback active filter topologies that offer much higher Qs and stopband attenuation than Sallen-Key architectures.

The MAX9939 draws 3.4mA of quiescent supply current at 5V, and includes a software-programmable shutdown mode that reduces its supply current to only 13µA. The MAX9939 is available in a 10-pin µMAX® package and operates over the -40°C to +125°C automotive temperature range.

Applications

- Sensorless Motor Control
- Medical Signal Conditioning
- Sonar and General Purpose Data Acquisition
- Differential to Single-Ended Conversion
- Differential-Input, Differential-Output Signal Amplification
- Sensor Interface and Signal Processing

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Functional Diagram appears at end of data sheet.

Features

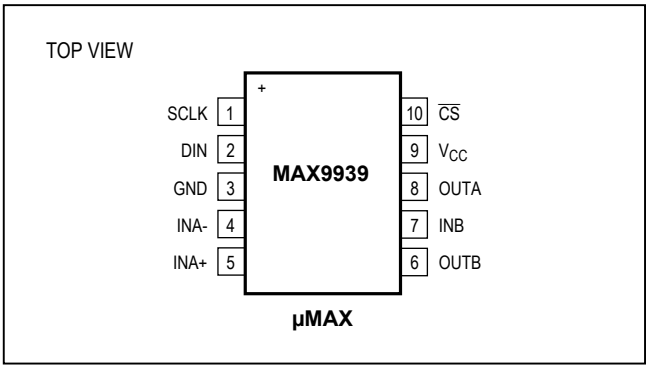
- SPI-Programmable Gains: 0.2V/V to 157V/V
- Extremely Low Gain Tempco
- Integrated Amplifier for R/C Programmable Active Filter
- Input Offset-Voltage Compensation
- Input Protection to ±16V
- 13µA Software Shutdown Mode
- -40°C to +125°C Operating Temperature Range
- 10-Pin µMAX Package

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9939AUB+	-40ºC to +125ºC	10 µMAX
MAX9939AUB/V+T	-40ºC to +125ºC	10 µMAX

/V denotes an automotive-qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.

Pin Configuration



maxim integrated™

Absolute Maximum Ratings

V_{CC} to GND .....-0.3V to +6V
INB, OUTA, OUTB, SCLK, DIN, $\overline{CS}$.....-0.3V to (V_{CC} + 0.3V)
INA+, INA- to GND.....-16V to +16V
Output Short-Circuit Current Duration.....Continuous
Continuous Input Current into Any Terminal .....±20mA
Continuous Power Dissipation (T_A = +70°C)
10-Pin µMAX (derate 5.6mW/°C above +70°C).....707mW

Operating Temperature Range..... -40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{CC} = 5V, V_{GND} = 0V, V_{INA+} = V_{INA-}, Gain = 10V/V, R_{OUTA} = R_{OUTB} = 1kΩ to V_{CC}/2, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PGA CHARACTERISTICS						
Gain Error	GE	T_A = +25°C, 0.2V ≤ V_{OUTA} ≤ VCC - 0.2V		0.05	0.38	%
Gain Temperature-Coefficient	Tc-GE			2.2	17	ppm/°C
Input Offset Voltage (Note 2)	V_{OS-A}	With no V_{OS} trim, T_A = +25°C		1.5	9	mV
		With no V_{OS} trim, T_A = T_{MIN} to T_{MAX}			15	
Input Offset-Voltage Drift				10		µV/C
Input Offset-Voltage Trim Range				±17		mV
Input Common-Mode Range	V_{CM}	Guaranteed by CMRR test (Note 3)	-V_{CC}/2		V_{CC} - 2.2	V
Common-Mode Rejection Ratio	CMRR	-1V ≤ V_{CM} ≤ V_{CC} - 2.2V	50	60		dB
		-V_{CC}/2 ≤ V_{CM} ≤ V_{CC} - 2.2V, T_A = +25°C	50	60		
		-V_{CC}/2 ≤ V_{CM} ≤ V_{CC} - 2.2V	39			
Output Short-Circuit current	I_{SC}			70		mA
Input-Voltage Noise Density	V_N	f = 10kHz, gain = 157V/V		54		nV/√Hz
Gain-Bandwidth Product	GBW	Gain = 0.2V/V		2.15		MHz
		Gain = 1V/V				
		Gain = 157V/V		279		
Slew Rate	SR			9		V/µs
Settling Time	t_S	To 1%, 2V output step		0.45		µs
Distortion	THD	f = 1kHz, V_{OUTA} = 2.5V_{P-P}		89		dB
Max Capacitive Load	$C_{L(MAX)}$			1		nF
Output Swing	V_{OH}, V_{OL}	Voltage output high = V_{CC} - V_{OUTA}, voltage output low = V_{OUTA} - V_{GND}		25	60	mV
OUTPUT AMPLIFIER CHARACTERISTICS						
Input Bias Current	Ib	(Note 4)		1		pA
Input Offset Voltage (Note 2)	V_{OS-B}	T_A = +25°C		1.5	9	mV
		T_A = T_{MIN} to T_{MAX}			15	
Output Short-Circuit Current	I_{SC}			70		mA

Electrical Characteristics (continued)

(V_{CC} = 5V, V_{GND} = 0V, V_{INA+} = V_{INA-}, Gain = 10V/V, R_{OUTA} = R_{OUTB} = 1kΩ to V_{CC}/2, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Unity-Gain Bandwidth	UGBW			2.2		MHz
Slew Rate	SR			6.4		V/µs
Settling Time	t_S	To 1%, 2V output step		0.86		µs
Input-Voltage Noise Density	V_N			36		nV/√Hz
Distortion	THD	f = 1kHz, V_{OUTA} = 2.5V_{P-P}, gain = -1V/V		90		dB
Max Capacitive Load	$C_{L(MAX)}$			1		nF
Output Swing	V_{OH}, V_{OL}	Voltage output high = V_{CC} - V_{OUTB}, voltage output low = V_{OUTB} - V_{GND}		25	60	mV
POWER SUPPLY						
Supply Voltage Range	V_{CC}	Guaranteed by PSRR	2.9		5.5	V
Power-Supply Rejection Ratio	PSRR	1kΩ between OUTA and INB, 1kΩ between OUTB and INB, measured differentially between OUTA and OUTB	60	80		dB
Supply Current	I_{CC}	OUTA and OUTB unloaded		3.4	6.7	mA
Shutdown Supply Current	$I_{\overline{SHDN}}$	Soft shutdown through SPI		13	24	µA
SPI CHARACTERISTICS						
Input-Voltage Low	V_{IL}				0.8	V
Input-Voltage High	V_{IH}	V_{CC} = 5V	2.0			V
		V_{CC} = 3.3V	1.65			
Input Leakage Current	I_{IN}				±1	µA
Input Capacitance	C_{IN}			5		pF
SPI TIMING CHARACTERISTICS						
SCLK Frequency	f_{SCLK}	(Note 5)			5	MHz
SCLK Period	t_{CP}		200			ns
SCLK Pulse-Width High	t_{CH}		80			ns
SCLK Pulse-Width Low	t_{CL}		80			ns
$\overline{CS}$ Fall to SCLK Rise Setup	t_{CSS}		80			ns
$\overline{CS}$ Fall to SCLK Rise Hold	t_{CSH}		20 + (0.5 x t_{CP})			ns
DIN to SCLK Setup	t_{DS}		55			ns
DIN Hold after SCLK	t_{DH}		0			ns
SCLK Rise to CS Fall Delay	t_{CS0}		20			ns
$\overline{CS}$ Rise to SCLK Rise Hold	t_{CS1}		80			ns
$\overline{CS}$ Pulse-Width High	t_{CSW}		200			ns

Note 1: All devices are 100% production tested at T_A = +25°C. Temperature limits are guaranteed by design.
Note 2: The input offset voltage includes the effects of mismatches in the internal V_{CC}/2 resistor dividers.
Note 3: For gain of 0.25V/V, the input common-mode range is -1V to V_{CC} - 2V.
Note 4: The input current of a CMOS device is too low to be accurately measured on an ATE and is typically on the order of 1pA.
Note 5: Parts are functional with f_{SCLK} = 10MHz.

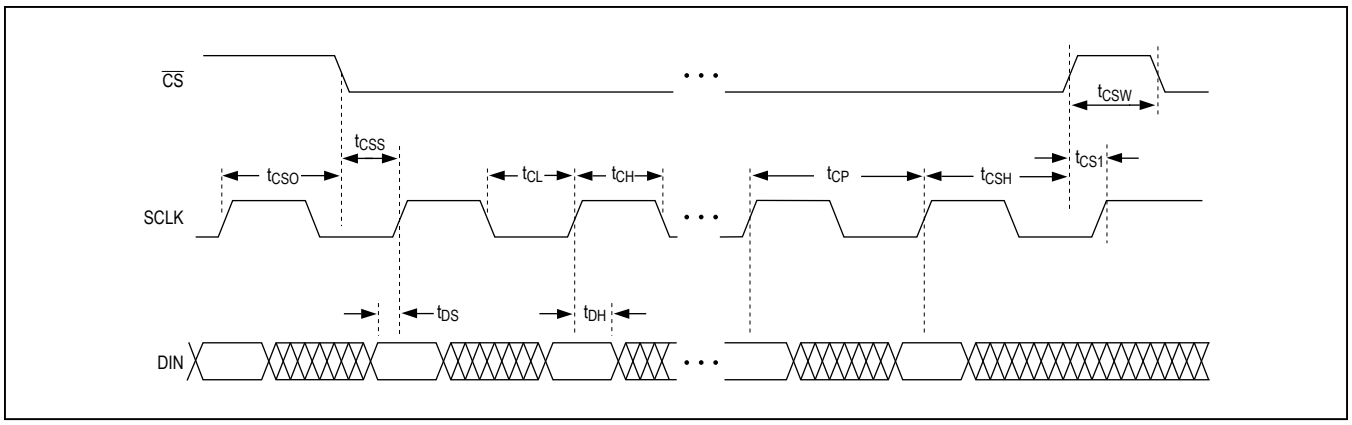
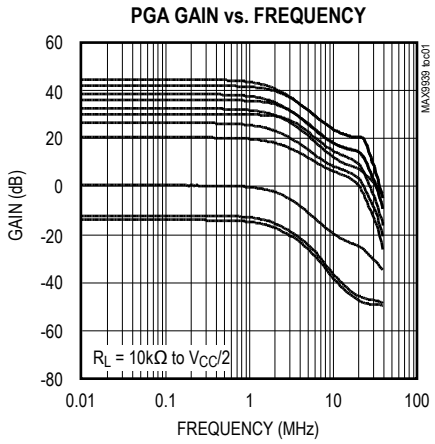
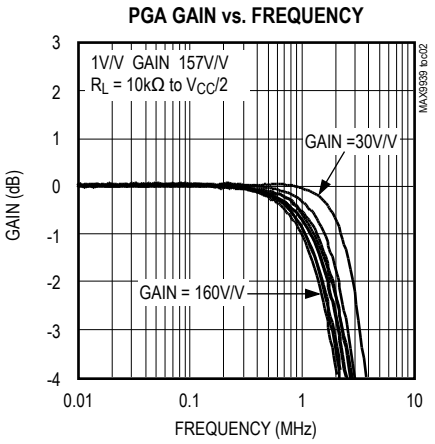


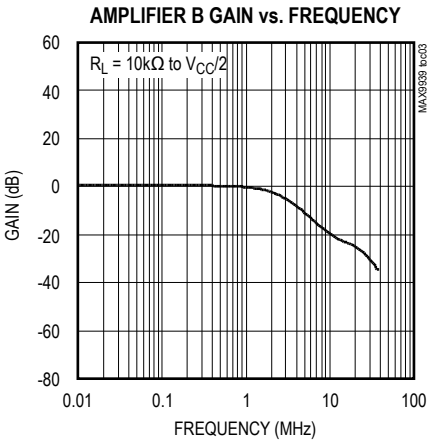
Figure 1. SPI Interface Timing Diagram

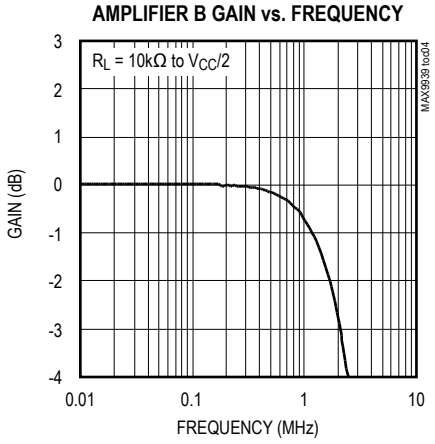
Typical Operating Characteristics

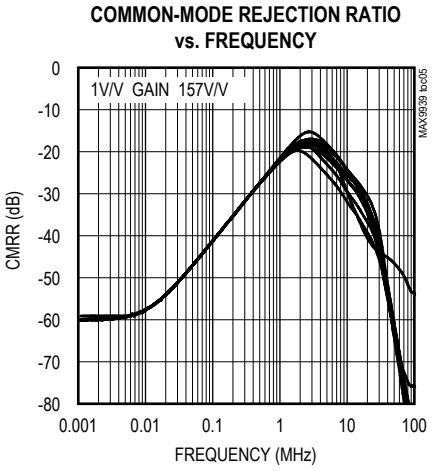
(V_{CC} = 5V, V_{GND} = 0V, V_{IN+} = V_{IN-} = 0V, Gain = 10V/V, R_{OUTA} = R_{OUTB} = 1kΩ to $V_{CC}/2$, T_A = +25°C, unless otherwise noted.)

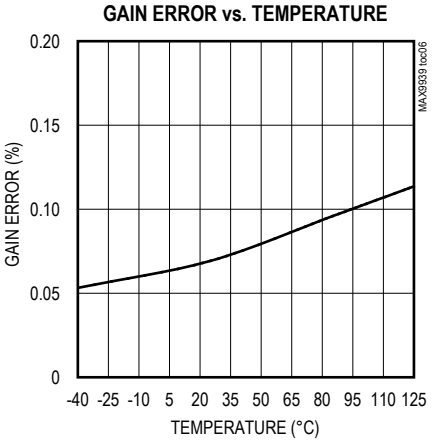








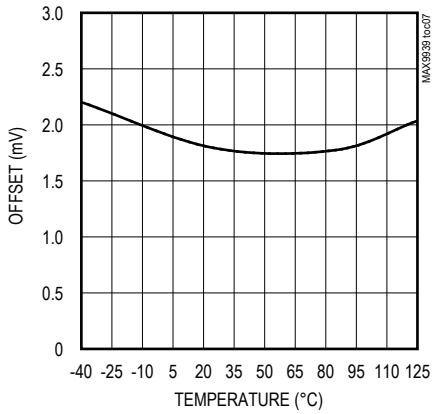




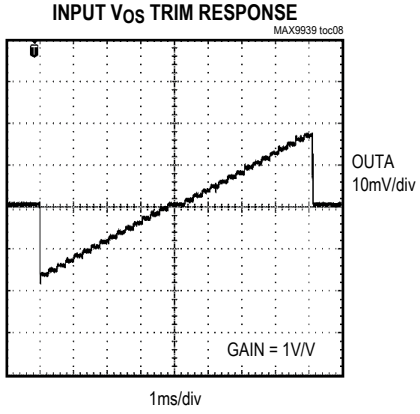
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_{GND} = 0V, V_{IN+} = V_{IN-} = 0V, Gain = 10V/V, R_{OUTA} = R_{OUTB} = 1kΩ to V_{CC}/2, T_A = +25°C, unless otherwise noted.)

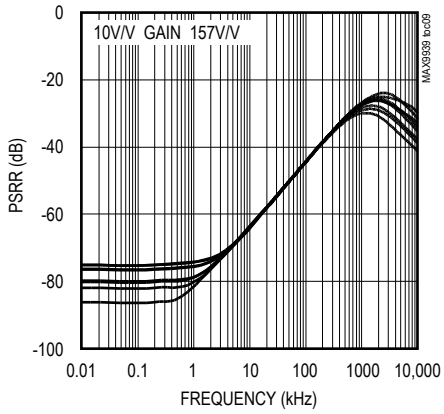
INPUT V_{OS} vs. TEMPERATURE



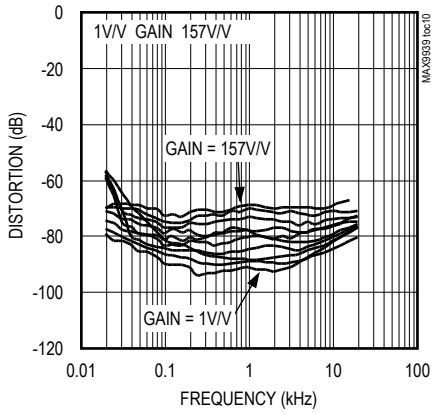
INPUT V_{OS} TRIM RESPONSE



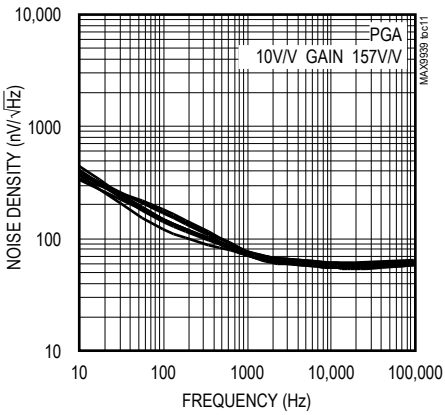
DIFFERENTIAL PSRR vs. FREQUENCY



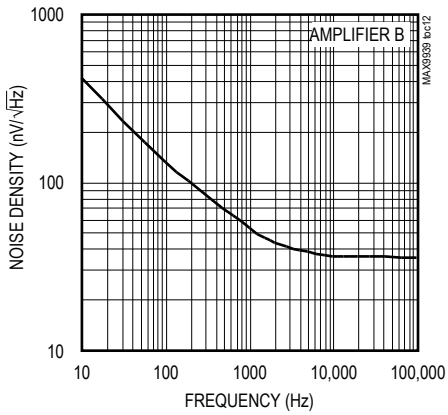
TOTAL HARMONIC DISTORTION vs. FREQUENCY



NOISE VOLTAGE DENSITY



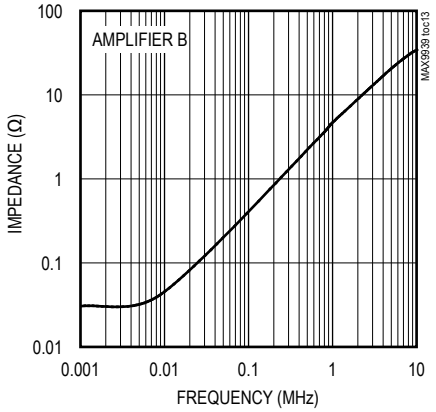
NOISE VOLTAGE DENSITY



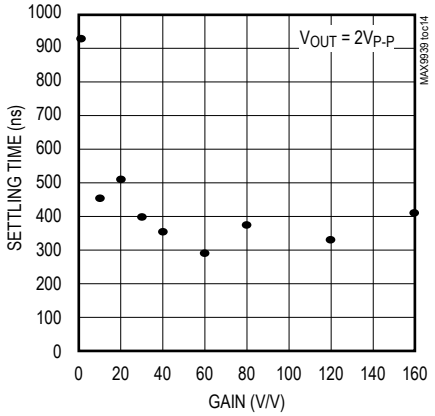
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_{GND} = 0V, V_{IN+} = V_{IN-} = 0V, Gain = 10V/V, R_{OUTA} = R_{OUTB} = 1kΩ to V_{CC}/2, T_A = +25°C, unless otherwise noted.)

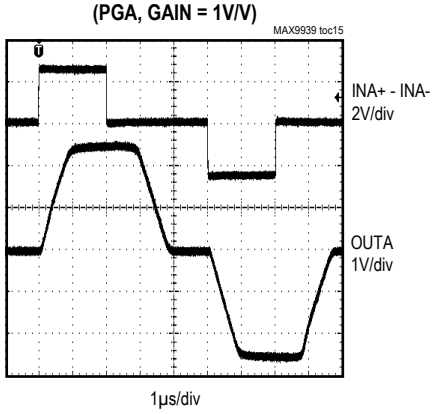
OUTPUT IMPEDANCE vs. FREQUENCY



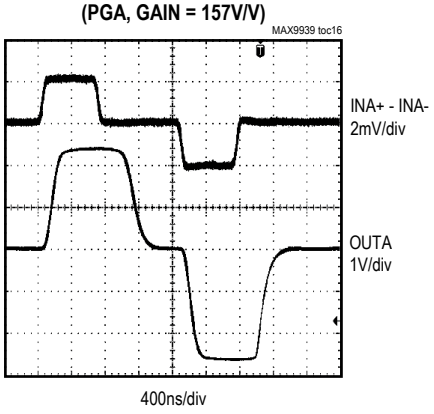
1% SETTLING TIME vs. GAIN (PGA)



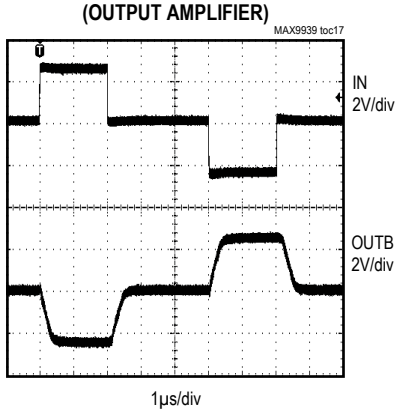
RECOVERY FROM INPUT OVERLOAD (PGA, GAIN = 1V/V)



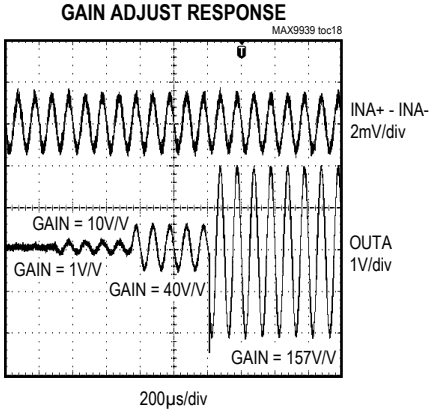
RECOVERY FROM INPUT OVERLOAD (PGA, GAIN = 157V/V)



RECOVERY FROM INPUT OVERLOAD (OUTPUT AMPLIFIER)



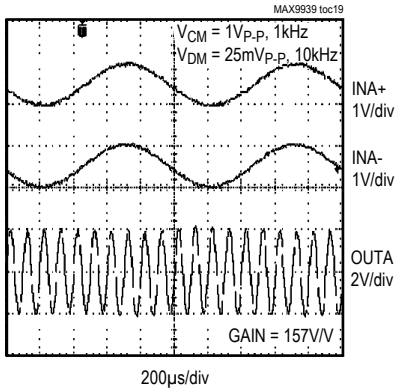
GAIN ADJUST RESPONSE



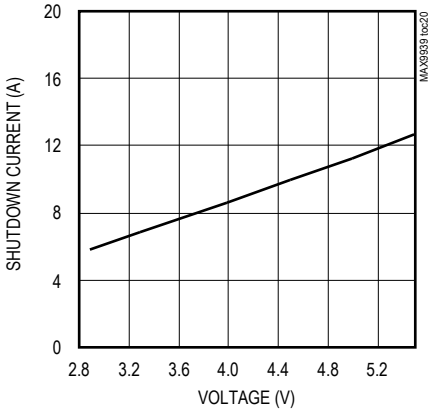
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_{GND} = 0V, V_{IN+} = V_{IN-} = 0V, Gain = 10V/V, R_{OUTA} = R_{OUTB} = 1kΩ to V_{CC}/2, T_A = +25°C, unless otherwise noted.)

COMMON-MODE REJECTION RESPONSE



SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



Pin Description

PIN	NAME	FUNCTION
1	SCLK	Serial-Clock Input
2	DIN	Serial-Data Input. Data is clocked into the serial interface on the rising edge of SCLK.
3	GND	Ground
4	INA-	PGA Inverting Input
5	INA+	PGA Noninverting Input
6	OUTB	Buffer Output
7	INB	Buffer Input
8	OUTA	PGA Output
9	V_{CC}	Power Supply. Bypass to GND with 0.1µF and 1µF capacitors.
10	$\overline{CS}$	Active-Low Chip-Select Input. Drive $\overline{CS}$ low to enable the serial interface. Drive $\overline{CS}$ high to disable the serial interface.

Detailed Description

The MAX9939 is a general-purpose PGA with input offset trim capability. Its gain and input offset voltage (V_{OS}) are SPI programmable. The device also includes an uncommitted output operational amplifier that can be used as either a high-order active filter or to provide a differential output. The device can be put into shutdown through SPI.

The gain of the amplifier is programmable between 0.2V/V and 157V/V (default gain is set to 1 V/V). The input offset is programmable between ±17mV and can be used to regain output dynamic range in high gain settings. An input offset-voltage measurement mode enables input offset voltage to be calibrated out in firmware to obtain excellent DC accuracy.

The main amplifier accepts a differential input and provides a single-ended output. The relationship between the differential input and singled-ended output is given by the representative equation:

$$V_{OUTA} = V_{CC}/2 - Gain \times (V_{INA+} - V_{INA-}) + Gain \times V_{OS}$$

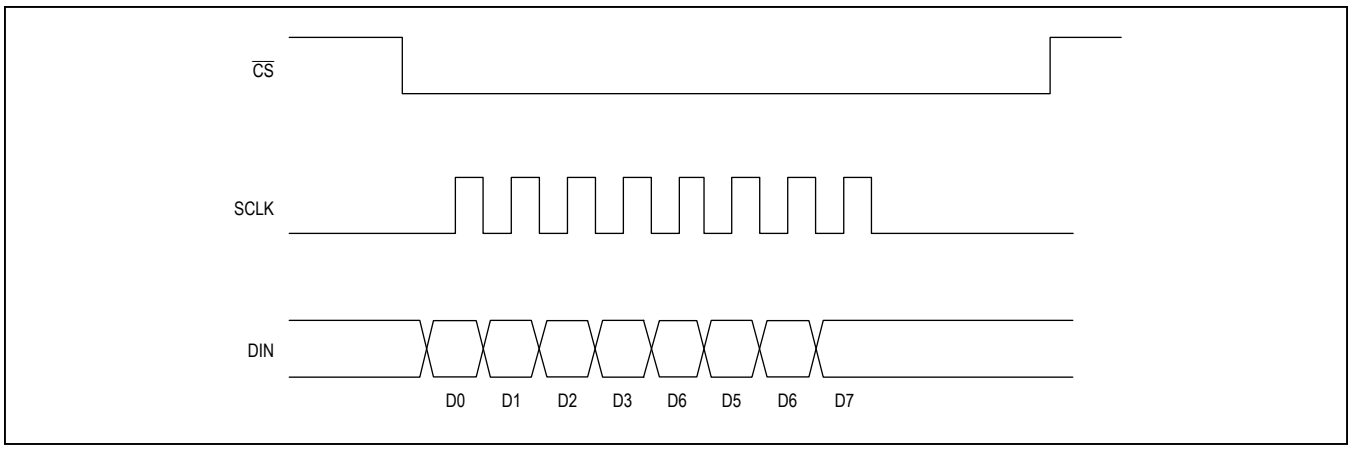


Figure 2. SPI Interface Timing Diagram (CPOL = CPHA = 0)

Architecture

The MAX9939 features three internal amplifiers as shown in the *Functional Diagram*. The first amplifier (amplifier LVL) is configured as a differential amplifier for differential to single-ended conversion with an input offset-voltage trim network. It has extremely high CMRR, gain accuracy, and very low temperature drift due to precise resistor matching. The output of this amplifier is level shifted to $V_{CC}/2$.

This amplifier is followed by a programmable-gain inverting amplifier (amplifier A) with programmable R_F and R_I resistors whose gain varies between 0.2V/V and 157V/V. The output of this amplifier is biased at $V_{CC}/2$ and has extremely high gain accuracy and low temperature drift. The MAX9939 has an uncommitted op amp (amplifier B) whose noninverting input is referenced to $V_{CC}/2$. Its inverting input and output are externally accessible, allowing it to be configured either as an active filter or as a differential output.

A robust input ESD protection scheme allows input voltages at INA+ and INA- to reach ±16V without damaging the MAX9939, thus making the part extremely attractive for use in front-ends that can be exposed to high voltages during fault conditions. In addition, its input-voltage range extends down to $-V_{CC}/2$ (e.g., -2.5V when powered from a 5V single supply) allowing the MAX9939 to translate below ground signals to a 0V to 5V output signal. This feature simplifies interfacing ground-referenced signals with unipolar-input ADCs.

SPI-Compatible Serial Interface

The MAX9939 has a write-only interface, consisting of three inputs: the clock signal (SCLK), data input (DIN), and chip-select input ($\overline{CS}$). The serial interface works with the clock polarity (CPOL) and clock phase (CPHA) both set to 0 (see Figure 1). Initiating a write to the MAX9939 is accomplished by pulling $\overline{CS}$ low. Data is clocked in on the rising edge of each clock pulse, and is written LSB first. Each write to the MAX9939 consists of 8 bits (1 byte). Pull $\overline{CS}$ high after the 8th bit has been clocked in to latch the data and before sending the next byte of instruction. Note that the internal register is not updated if $\overline{CS}$ is pulled high before the falling edge of the 8th clock pulse.

Register Description

The MAX9939 consists of three registers: a shift register and two internal registers. The shift register accepts data and transfers it to either of the two internal registers. The two internal registers store data that is used to determine the gain, input offset voltage, and operating modes of the amplifier. The two internal registers are the Input V_{OS} Trim register and Gain register. The format of the 8-bit write to these registers is shown in Tables 1 and 2. Data is sent to the shift register LSB first.

Table 1. Input V_{OS} Trim Register

D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB
SHDN	MEAS	V4	V3	V2	V1	V0	SEL = 0

Table 2. Gain Register

D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB
SHDN	MEAS	X	G3	G2	G1	G0	SEL = 1

X = Don't care.

SEL: The SEL bit selects which internal register is written to. Set SEL to 0 to write bits D5:D1 to the input V_{OS} trim register. Set SEL to 1 to write D4:D1 to the Gain register (D5 is don't care when SEL = 1).

SHDN: Set SHDN to 0 for normal operation. Set SHDN to 1 to place the device in a low-power 13µA shutdown mode. In shutdown mode, the outputs OUTA and OUTB are high impedance, however, the SPI decode circuitry is still active. Each instruction requires a write to the SHDN bit.

MEAS: The MAX9939 provides a means for measuring its own input offset voltage. When MEAS is set to 1, the INA- input is disconnected from the input signal path and internally shorted to INA+. This architecture thus allows the input common-mode voltage to be compensated at the application-specific input common-mode voltage of interest. The input offset voltage of the PGA is the output offset voltage divided by the programmed gain without any V_{OS} trim (i.e., V3:V0 set to 0):

$$V_{OS\text{-}INHERENT} = (V_{OUTA} - V_{CC}/2)/Gain$$

Program V_{OS} to offset $V_{OS\text{-}INHERENT}$. The input V_{OS} also includes the effect of mismatches in the resistor-dividers. Setting MEAS to 0 switches the inputs back to the signals on INA+ and INA-. Each instruction requires a write to the MEAS bit.

Programming Gain

The PGA's gain is set by the bits G3:G0 in the Gain register. Table 3 shows the relationship between the bits G3:G0 and the amplifier's gain. The slew rate and small-signal bandwidth (SSBW) of the PGA depend on its gain setting as shown in Table 3.

Programming Input Offset Voltage (VOS)

The input offset voltage is set by the bits V4:V0 in the Input Offset Voltage Trim register. Bit V4 determines the polarity of the offset. Setting V4 to 0 makes the offset positive, while setting V4 to 1 makes the offset negative. Table 4 shows the relationship between V3:V0 and V_{OS}.

To determine the effect of V_{OS} at the output of the amplifier for gains other than 1, use the following formula:

$$V_{OUTA} = V_{CC}/2 + Gain \times (V_{OS\text{-}INHERENT} + V_{OS})$$

where $V_{OS\text{-}INHERENT}$ is the inherent input offset voltage of the amplifier, which can be measured by setting MEAS to 1.

Applications Information

Use of Output Amplifier as Active Filter

The output amplifier can be configured as a multiple-feedback active filter as shown in Figure 3, which traditionally has better stopband attenuation characteristics than Sallen-Key filters. These filters also possess inherently better distortion performance since there are no common-mode induced effects (i.e., the common-mode voltage of the operational amplifier is always fixed at $V_{CC}/2$ instead of it being signal dependent such as in Sallen-Key filters). Choose external resistors and capacitors to create lowpass, bandpass, or highpass filters.

Table 3. Gain

G3:G0	GAIN (V/V)	SLEW RATE (V/µs)	SMALL-SIGNAL BANDWIDTH (MHz)
0000	1	2.90	2.15
0001	10	8.99	2.40
0010	20	8.70	1.95
0011	30	12.80	3.40
0100	40	12.50	2.15
0101	60	13.31	2.60
0110	80	12.15	1.91
0111	120	18.53	2.30
1000	157	16.49	1.78
1001	0.2 (V_{CC} = 5V)	2.86	1.95
	0.25 (V_{CC} = 3.3V)		
1010	1	2.90	2.15

Table 4. Input Offset-Voltage Trim

INPUT OFFSET VOLTAGE (V4 = 0 TRIMS POSITIVE, V4 = 1 TRIMS NEGATIVE)	
V3:V0	**V_{OS} (mV)**
0000	0
0001	1.3
0010	2.5
0011	3.8
0100	4.9
0101	6.1
0110	7.3
0111	8.4
1000	10.6
1001	11.7
1010	12.7
1011	13.7
1100	14.7
1101	15.7
1110	16.7
1111	17.6

Differential-Input, Differential-Output PGA

The output amplifier can be configured so that the MAX9939 operates as a differential-input, differential-output programmable gain amplifier. As shown in Figure 4, use a 10kΩ resistor between OUTA and INB, and between INB and OUTB. Such a differential-output configuration is ideal for use in low-voltage applications that can benefit from the 2X output voltage dynamic range when compared to single-ended output format.

Use of Output Operational Amplifier as TIA

CMOS inputs on the output op amp makes it ideal for use as an input transimpedance amplifier (TIA) in certain current-output sensor applications. In such a situation, keep in mind that the inverting input operates at fixed voltage of $V_{CC}/2$. Use a high-value resistor as a feedback gain element, and use a feedback capacitor in parallel with this resistor if necessary to aid amplifier stability in the presence of high photodiode or cable capacitance. The output of this TIA can be routed to INA+ or INA- for further processing and signal amplification.

Power-Supply Bypassing

Bypass V_{CC} to GND with a 0.1µF capacitor in parallel with a 1µF low-ESR capacitor placed as close as possible to the MAX9939.

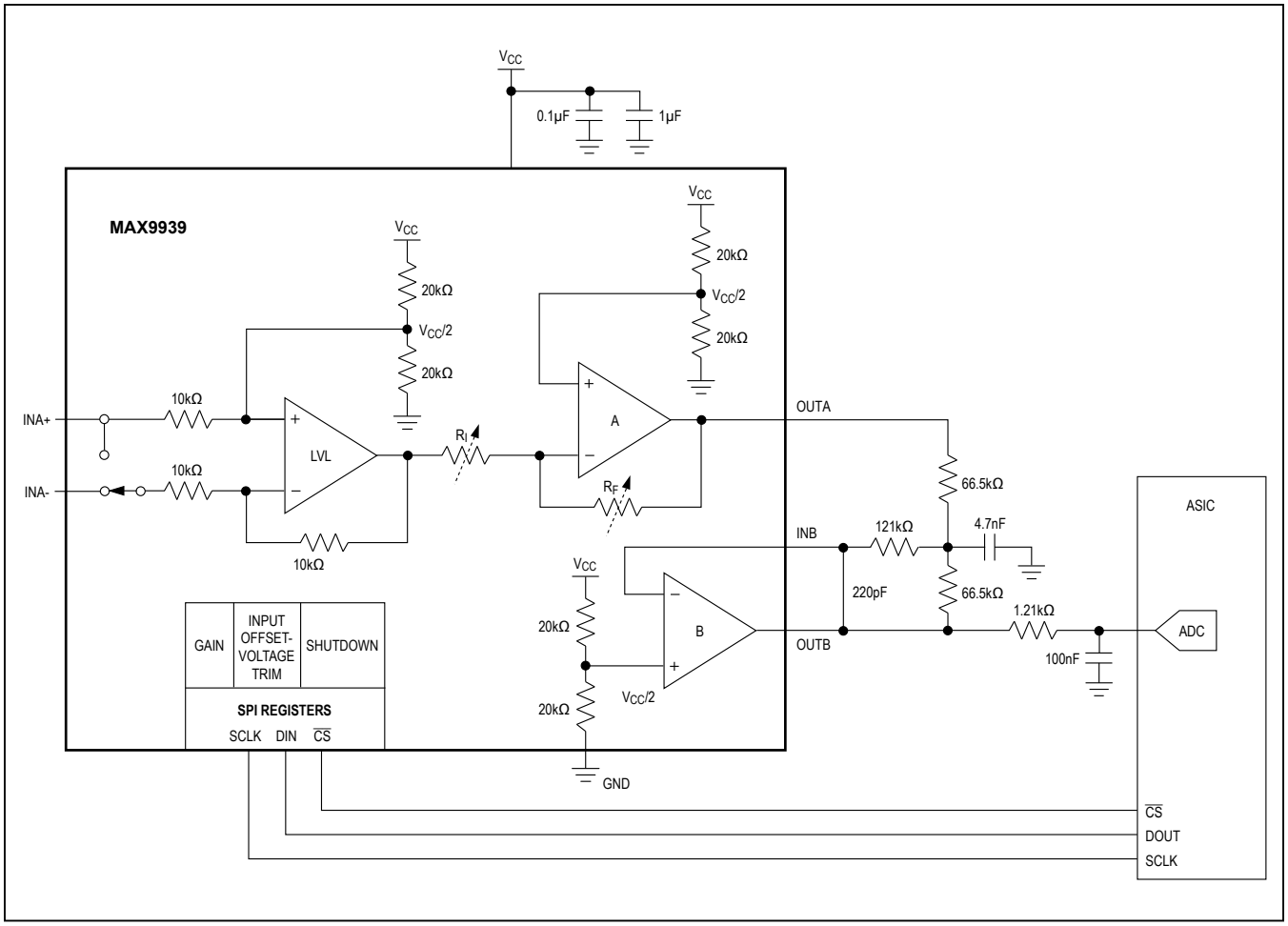


Figure 3. Using the MAX9939 Output Amplifier as an Anti-Aliasing Filter (Corner Frequency = 1.3kHz) to Maximize Nyquist Bandwidth

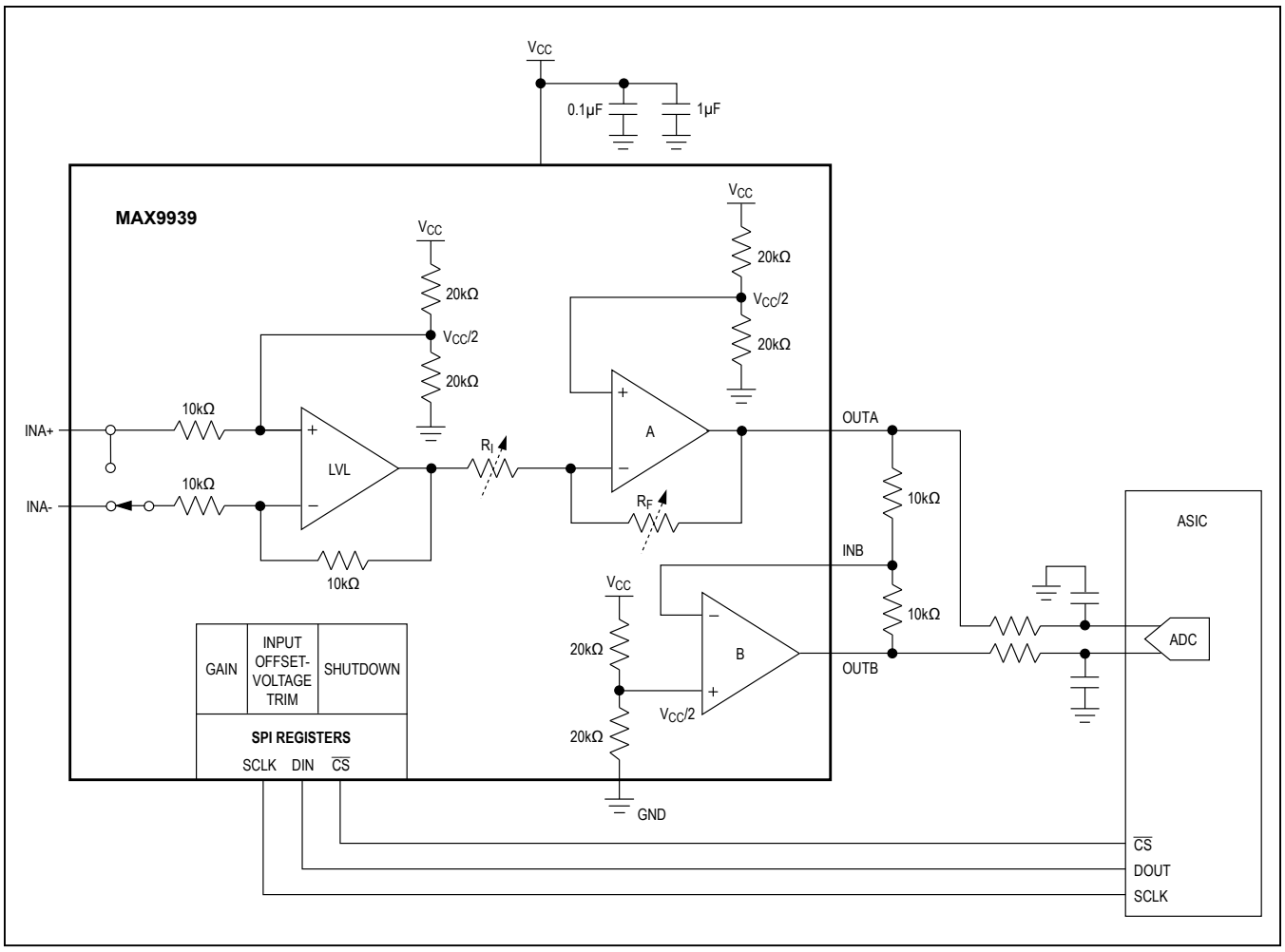
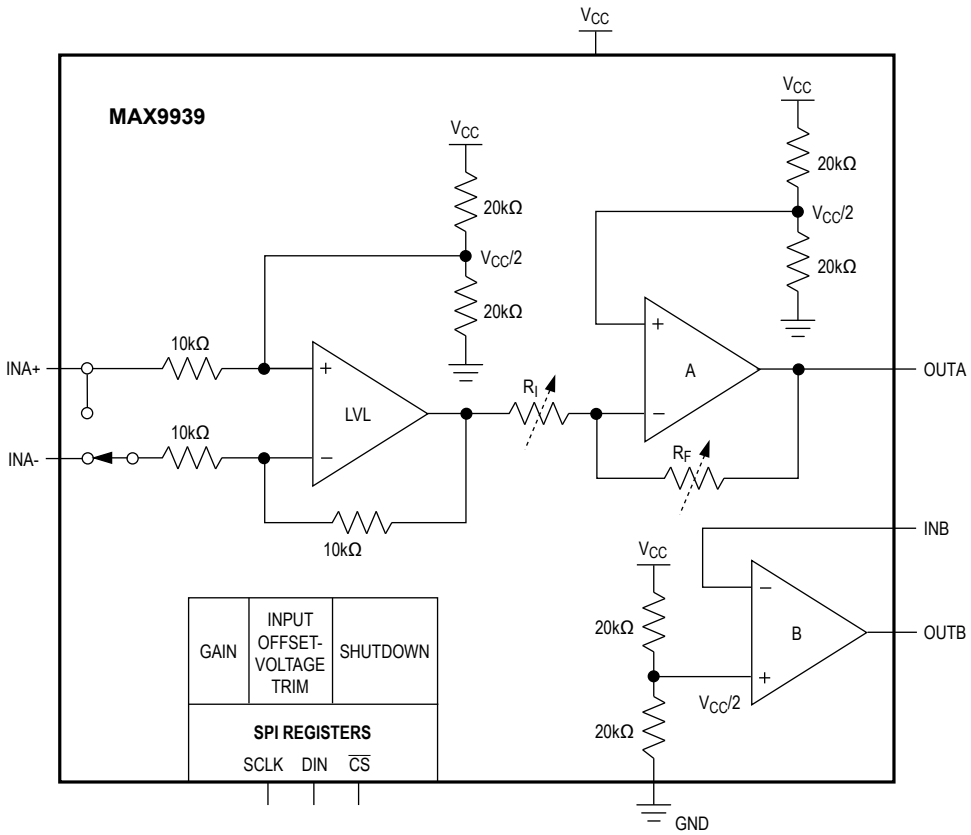


Figure 4. Using the MAX9939 as a Differential-Input, Differential-Output PGA

Chip Information

PROCESS: BiCMOS

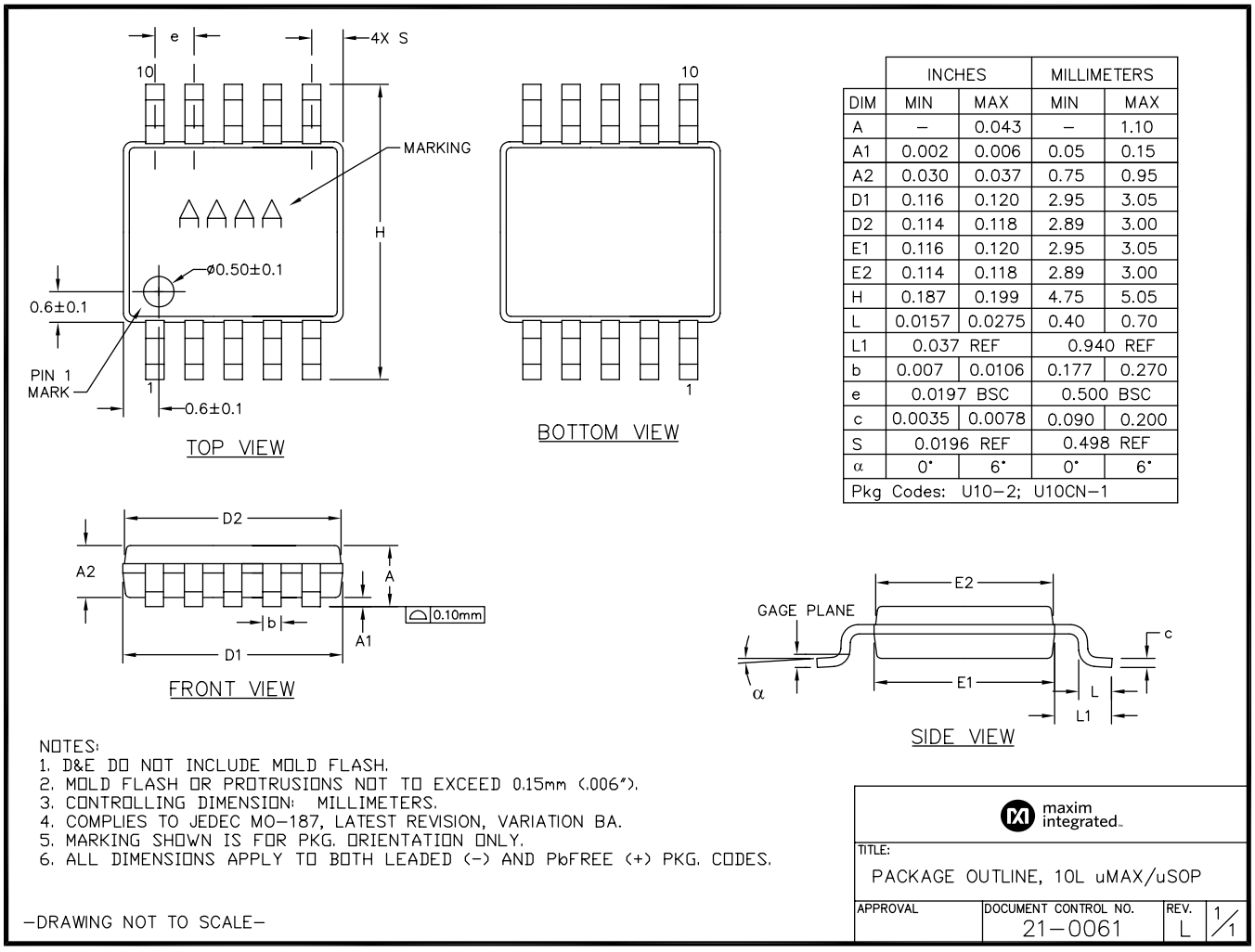
Functional Diagram



Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
10 µMAX	U10+2	21-0061	90-0330



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	–	0.043	–	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
D1	0.116	0.120	2.95	3.05
D2	0.114	0.118	2.89	3.00
E1	0.116	0.120	2.95	3.05
E2	0.114	0.118	2.89	3.00
H	0.187	0.199	4.75	5.05
L	0.0157	0.0275	0.40	0.70
L1	0.037 REF		0.940 REF	
b	0.007	0.0106	0.177	0.270
e	0.0197 BSC		0.500 BSC	
c	0.0035	0.0078	0.090	0.200
S	0.0196 REF		0.498 REF	
α	0°	6°	0°	6°
Pkg Codes: U10–2; U10CN–1				

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. COMPLIES TO JEDEC MO–187, LATEST REVISION, VARIATION BA.
5. MARKING SHOWN IS FOR PKG. ORIENTATION ONLY.
6. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

–DRAWING NOT TO SCALE–

maxim integrated

TITLE: PACKAGE OUTLINE, 10L uMAX/uSOP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21–0061	L	1/1

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/08	Initial release	—
1	2/09	Corrected gain value in Table 3	9
2	12/10	Modified Figure 2	8
3	12/12	Added the MAX9939AUB/V+T	1
4	8/19	Updated *Detailed Description*	7

