Notification Number:	20210118003	Notification Date:	Jan. 19, 2021
Title:	Datasheet for ADS54J40		
Customer Contact:	PCN Manager	Dept:	Quality Services
Change Type:	Electrical Specification		

Notification Details

Description of Change:

Texas Instruments Incorporated is announcing an information only notification.
The product datasheet(s) is being updated as summarized below.
The following change history provides further details.

TEXAS INSTRUMENTS

ADS54J40

SBAS714C – MAY 2015 – REVISED DECEMBER 2020

Changes from Revision B (January 2017) to Revision C (December 2020) **Page**

- Added text '(Including Interleaving Tones)' to *Features* bullet 1
- Added *ADS54J40 Comparison* section, moved *Device Comparison Table* to this section 5
- Changed the description of SYSREFM, SYSREFP, and PDN pins in *Pin Functions* table 5
- Changed f_{IN} = *470 MHz* test conditions and typical values across parameters in *AC Characteristics* table 11
- Added f_{IN} = *720 MHz* test conditions across parameters in *AC Characteristics* table 11
- Changed ENOB unit from *dBFS* to *Bits* in *AC Characteristics* table 11
- Changed typical values of SFDR_IL parameter 11
- Changed first IMD3 typical value from *–85 dBFS* to *–89 dBFS* 11
- Changed first footnote in *Timing Characteristics* table 15
- Changed typical value of *FOVR latency* from *18 + 4 ns* to *18* 15
- Changed t_{PD} parameter name to t_{PDI} in *Timing Characteristics* table 15
- Changed *FFT for 470-MHz Input Signal at –3 dBFS* figure, title, and conditions 17
- Added *FFT for 720-MHz Input Signal at –6 dBFS* figure 17
- Changed *Spurious-Free Dynamic Range vs Input Frequency* figure 17
- Changed *IL Spur vs Input Frequency* figure 17
- Changed *16-bit* to *14-bit* in first sentence of *Overview* section 27
- Added *DDC Block* section 30
- Changed Table 8-6 36
- Added last sentence to Step 4 in *Serial Register Readout: Analog Bank* section 39
- Added last sentence to Step 4 in *Serial Register Readout: JESD Bank* section 40
- Added *SDOUT Timing Diagram* figure 40
- Changed the *JESD204B Test Patterns* section 43
- Changed *Serial Interface Registers* diagram 48
- Added register addresses 1 and 2 to *GENERAL REGISTERS* in *Register Map* section 48
- Changed the name of *JESD ANALOG PAGE (6A00h)* to *JESD ANALOG PAGE (JESD BANK PAGE SEL=6A00h)* in *Register Map* table 48

- Changed bit 1, register 12 of *JESD ANALOG PAGE (6A00h)* from *0* to *ALWAYS WRITE 1* 48
- Added *OFFSET READ Page* and *OFFSET LOAD Page* registers to *Register Map* table 48
- Added *ADS54J40 Access Type Codes* table..... 52
- Deleted legends from bit registers in *Register Descriptions* section..... 53
- Added register 1h and 2h to *Register Descriptions* section 53
- Added text '6100h = OFFSET READ or LOAD Page' to the JESD BANK PAGE SEL[7:0] bit description..... 53
- Changed description of *Registers 3h and 4h (address = 3h and 4h)*in *General Registers Page*. 54
- Changed description of bit 0 in Register 4Fh (address = 4Fh), Master Page (080h)..... 58
- Changed *Register 53H* 59
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- Added *Register 40h* 62
- Changed *Register 4Eh* 67
- Changed *Register 52h* 67
- Added *Register 68h* 68
- Changed the *Register ABh* description..... 69
- Changed bit 1 from *0* to *ALWAYS WRITE 1* in Register 12h (address = 12h), JESD Analog Page (6A00h)... 76
- Changed *Register 1Ah* 79
- Added *Offset Read Page Register* and *Offset Load Page Register* sections to *Register Descriptions* section... 81
- Changed *Register 075h, 077h, 079h, 7Bh (address = 075h, 077h, 079h, 7Bh* 82
- Changed *Register 00h, 04h, 08h, 0Ch* 83
- Changed *Register 01h, 05h, 09h, 0Dh* 83
- Added *Register 78h* 84
- Added *DC Offset Correction Block in the ADS54J40* section..... 89
- Added *Idle Channel Histogram* section..... 93
- Added the *Interleaving (IL) Mismatch Compensation* section..... 94
- Changed the description in Transformer-Coupled Circuits section..... 104
- Changed the *Layout Guidelines* 107

The datasheet number will be changing.

Device Family	Change From:	Change To:
ADS54J40	SBAS714B	SBAS714C

These changes may be reviewed at the datasheet links provided.

http://www.ti.com/product/ADS54J40

Reason for Change:

To accurately reflect device characteristics.

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

No anticipated impact. This is a specification change announcement only. There are no changes to the actual device.

Changes to product identification resulting from this notification:

None.

Product Affected:

ADS54J40IRMP	ADS54J40IRMPT		

For questions regarding this notice, e-mails can be sent to the contacts shown below or your local Field Sales Representative.

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