ADS5401 Single 12-Bit 800-Msps Analog-to-Digital Converter

1 Features

- Single-Channel
- 12-Bit Resolution
- Maximum Clock Rate: 800 Msps
- Low Swing Fullscale Input: 1.0 Vpp
- Analog Input Buffer With High Impedance Input
- Input Bandwidth (3 dB): > 1.2 GHz
- Data Output Interface: DDR LVDS
- Optional 2x Decimation With Lowpass or Highpass Filter
- 196-Pin BGA Package (12 mm × 12 mm)

2 Applications

- Test and Measurement Instrumentation
- Ultra-Wide Band Software Defined Radio
- Data Acquisition
- Power Amplifier Linearization
- Signal Intelligence and Jamming
- Radar and Satellite Systems
- Microwave Receivers
- Cable Infrastructure
- Non-Destructive Testing
- Power Dissipation: 1.33 W/ch
- Spectral Performance at f_{in} = 230 MHz IF
  - SNR: 61.3 dBFS
  - SFDR: 74 dBc
- Spectral Performance at f_{in} = 700 MHz IF
  - SNR: 59.8 dBFS
  - SFDR: 69 dBc

3 Description

The ADS5401 device is a high-linearity single-channel 12-bit, 800-Msps analog-to-digital converter (ADC) easing front-end filter design for wide bandwidth receivers. The analog input buffer isolates the internal switching of the on-chip track-and-hold from disturbing the signal source as well as providing a high-impedance input. Optionally the output data can be decimated by two. Designed for high SFDR, the ADC has low-noise performance and outstanding spurious-free dynamic range over a large input-frequency range. The device is available in a 196-pin BGA package and is specified over the full industrial temperature range (–40°C to 85°C).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADS5401	NFBGA (196)	12.00 mm x 12.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

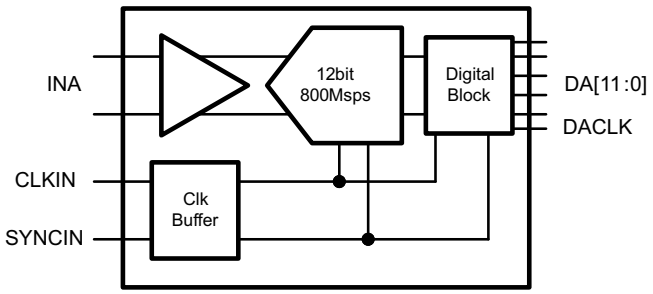


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (December 2013) to Revision B **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Original (April 2013) to Revision A **Page**

- Deleted text from last paragraph in INTERLEAVING CORRECTION section ... 21
- Changed text in second paragraph in MULTI DEVICE SYNCHRONIZATION section ... 22
- Deleted Register Initialization section and added Device Initialization section ... 23
- Changed Register Address E Bits D1 and D2 to 0 in SERIAL REGISTER MAP ... 25
- Changed Register Address 38 Bits D3 to D0 from 0 to 1 in SERIAL REGISTER MAP ... 25
- Changed Register Address 1 Bit D14 from 1 to 0 ... 27
- Changed Register Address E Bit D1 and D0 to 0 ... 29
- Changed Register Address 38 Bits D3 to D0 from 0 to 1 and add D3 to D0 Read back 1 ... 31
- Changed Register Address 66 D15-D10 to D15-D0 and DA11-D0 to DA11-DA0 ... 33

5 Device Options

DEVICE PART NO.	NUMBER OF CHANNELS	SPEED GRADE
ADS5402	2	800 Msps
ADS5401	1	800 Msps
ADS5404	2	500 Msps
ADS5403	1	500 Msps
ADS5407	2	500 Msps
ADS5409	2	900 Msps

6 Pin Configuration and Functions

ZAY Package
196-Pin NFBGA
Top View

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	
14	VREF	VCM	GND	NC	NC	GND	AVDDC	AVDDC	GND	INA_P	INA_N	GND	GND	CLKINP	14
13	SDENB	TEST MODE	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	CLKINN	13
12	SCLK	SRESET B	GND	AVDD33	AVDD33	AVDD33	AVDD33	AVDD33	AVDD33	AVDD33	AVDD33	GND	AVDD33	AVDD33	12
11	SDIO	ENABLE	GND	AVDD18	AVDD18	AVDD18	AVDD18	AVDD18	AVDD18	AVDD18	AVDD18	GND	AVDD18	AVDD18	11
10	SDO	IOVDD	GND	AVDD18	GND	GND	GND	GND	GND	GND	AVDD18	GND	NC	NC	10
9	DVDD	DVDD	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	SYNCN	SYNCP	9
8	DVDD	DVDD	DVDD	DVDD	GND	GND	GND	GND	GND	GND	DVDD	DVDD	DVDD	DVDD	8
7	NC	NC	DVDD LVDS	DVDD LVDS	GND	GND	GND	GND	GND	GND	DVDD LVDS	DVDD LVDS	NC	NC	7
6	NC	NC	DVDD LVDS	DVDD LVDS	GND	GND	GND	GND	GND	GND	DVDD LVDS	DVDD LVDS	NC	NC	6
5	NC	NC	NC	NC	GND	GND	GND	GND	GND	GND	OVRAN	OVRAP	SYNC OUTN	SYNC OUTP	5
4	NC	NC	NC	NC	NC	NC	NC	DA0P	DA2P	DA4P	DA6P	DA8P	NC	NC	4
3	NC	NC	NC	NC	NC	NC	NC	DA0N	DA2N	DA4N	DA6N	DA8N	DA11N	DA11P	3
2	NC	NC	NC	NC	NC	NC	NC	DACLKP	DA1P	DA3P	DA5P	DA7P	DA10N	DA10P	2
1	NC	NC	NC	NC	NC	NC	NC	DACLKN	DA1N	DA3N	DA5N	DA7N	DA9N	DA9P	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
INPUT/REFERENCE			
INA_P/N	K14, L14	I	Analog ADC A differential input signal.
VCM	B14	O	Output of the analog input common-mode (nominally 1.9 V). A 0.1-µF capacitor to AGND is recommended.
VREF	A14	O	Reference voltage output (2-V nominal). A 0.1-µF capacitor to AGND is recommended, but not required.
CLOCK/SYNC			
CLKINP/N	P14, P13	I	Differential input clock
SYNCP/N	P9, N9	I	Synchronization input. Inactive if logic low. When clocked in a high state initially, this is used for resetting internal clocks and digital logic and starting the SYNCOUT signal. Internal 100-Ω termination.
CONTROL/SERIAL			
ENABLE	B11	I	Chip enable – active high. Power-down function can be controlled through SPI register assignment. Internal 50-kΩ pullup resistor to IOVDD.
SCLK	A12	I	Serial interface clock. Internal 50-kΩ pulldown resistor.
SDENB	A13	I	Serial interface enable. Internal 50-kΩ pulldown resistor.
SDIO	A11	I/O	Bidirectional serial data in 3 pin mode (default). In 4-pin interface mode (register x00, D16), the SDIO pin is an input only. Internal 50-kΩ pulldown.
SDO	A10	O	Unidirectional serial interface data in 4 pin mode (register x00, D16). The SDO pin is tri-stated in 3-pin interface mode (default). Internal 50-kΩ pulldown resistor.
SRESET	B12	I	Serial interface reset input. Active low. Initialized internal registers during high to low transition. Asynchronous. Internal 50-kΩ pullup resistor to IOVDD.
TESTMODE	B13	—	Factory internal test, do not connect
DATA INTERFACE			
DA[11:0]P/N	P3, N3, P2, N2, P1, N1, M4, M3, M2, M1, L4, L3, L2, L1, K4, K3, K2, K1, J4, J3, J2, J1, H4, H3	O	ADC A Data Bits 11 (MSB) to 0 (LSB) in DDR output mode. Standard LVDS output.
DACLKP/N	H2, H1	O	DDR differential output data clock for Bus A. Register programmable to provide either rising or falling edge to center of stable data nominal timing.
OVRAP/N	M5, L5	O	Bus A, Overrange indicator, LVDS output. A logic high signals an analog input in excess of the full-scale range. Optional SYNC output.
NC	A1, A2, A3, A4, A5, A6, A7, B1, B2, B3, B4, B5, B6, B7, C1, C2, C3, C4, C5, D1, D2, D3, D4, D5, D14, E1, E2, E3, E4, E14, F3, F4, G1, G2, G3, G4, N4, N6, N7, N10, P4, P6, P7, P10	—	Do not connect to pin
SYNCOUTP/N	F2, F1, P5, N5	O	Synchronization output signal for synchronizing multiple ADCs. Can be disabled through SPI.
POWER SUPPLY			
AVDD18	D10, D11, E11, F11, G11, H11, J11, K11, L10, L11, N11, P11	I	1.8-V analog supply
AVDD33	D12, E12, F12, G12, H12, J12, K12, L12, N12, P12	I	3.3-V analog supply
AVDDC	G14, H14	I	1.8-V supply for clock input
DVDD	A8, A9, B8, B9, C8, D8, L8, M8, N8, P8	I	1.8-V supply for digital block
DVDDLVDS	C6, C7, D6, D7, L6, L7, M6, M7	I	1.8-V supply for LVDS outputs

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
GND		I	Ground
IOVDD	B10	I	1.8-V for digital I/Os

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	AVDD33	–0.5	4	V
	AVDDC	–0.5	2.3	
	AVDD18	–0.5	2.3	
	DVDD	–0.5	2.3	
	DVDDLVDS	–0.5	2.3	
	IOVDD	–0.5	4	
Voltage applied to input pins	INA_P, INA_N	–0.5	AVDD33 + 0.5	V
	CLKINP, CLKINN	–0.5	AVDDC + 0.5	V
	SYNCP, SYNCN	–0.5	AVDD33 + 0.5	V
	SRESET, SDENB, SCLK, SDIO, SDO, ENABLE	–0.5	IOVDD + 0.5	V
Operating free-air temperature, T_A		–40	85	°C
Operating junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
SUPPLY					
Supply voltage	AVDD33	3.15	3.3	3.45	V
	AVDDC, AVDD18, DVDD, DVDDLVDS	1.7	1.8	1.9	
	IOVDD	1.7	1.8	3.45	
GENERAL PARAMETERS					
	ADC Clock Frequency	40		800	MSPS
	Resolution	12			Bits
T_J	Recommended operating junction temperature			105	°C
	Maximum rated operating junction temperature(1)			125	
T_A	Recommended free-air temperature	–40	25	85	°C

(1) Prolonged use at this junction temperature may increase the device failure-in-time (FIT) rate.

7.4 Thermal Information

THERMAL METRIC(1)		ADS5401 ZAY (NFBGA) 196 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	37.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance(3)	6.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance(4)	16.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter(5)	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter(6)	16.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance(7)	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

7.5 Electrical Characteristics - Supply, Power Supply

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85 °C, ADC sampling rate = 800 Msps, 50% clock duty cycle, AVDD33 = 3.3V, AVDDC/AVDD18/DVDD/DVDDLVDS/IOVDD = 1.8 V, –1 dBFS differential input (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_{AVDD33}	3.3-V analog supply current			161	181	mA
I_{AVDD18}	1.8-V analog supply current			73	85	mA
I_{AVDDC}	1.8-V clock supply current			52	70	mA
I_{DVDD}	1.8-V digital supply current	Auto correction enabled		238	280	mA
I_{DVDD}	1.8-V digital supply current	Auto correction disabled		175		mA
I_{DVDD}	1.8-V digital supply current	Auto correction disabled, decimation filter enabled		190		mA
$I_{DVDDLVDS}$	1.8-V LVDS supply current			80	100	mA
I_{IOVDD}	1.8-V I/O Voltage supply current			1	2	mA
P_{dis}	Total power dissipation	Auto correction enabled, decimation filter disabled		1.33	1.6	W
P_{dis}	Total power dissipation	Auto correction disabled, decimation filter disabled		1.22		W
PSRR		250kHz to 500MHz	40			dB
	Shut-down power dissipation			7		mW
	Shut-down wake-up time			2.5		ms
	Standby power dissipation			7		mW
	Standby wake-up time			100		µs
	Deep-sleep mode power dissipation	Auto correction disabled		295		mW
		Auto correction enabled		360		mW
	Deep-sleep mode wake-up time			20		µs
	Light-sleep mode power dissipation	Auto correction disabled		465		mW
		Auto correction enabled		530		mW
	Light-sleep mode wake-up time			2		µs

7.6 Electrical Characteristics - Analog Inputs, Dynamic Accuracy, Clock Input

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 800 Msps, 50% clock duty cycle, AVDD3V = 3.3V, AVDD/DRVDD/IOVDD = 1.8 V, –1 dBFS differential input (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS					
Differential input full-scale			1.0		Vpp
Input common-mode voltage			1.9	±0.1	V
Input resistance	Differential at DC		1		kΩ
Input capacitance	Each input to GND		2		pF
VCM common-mode voltage output			1.9		V
Analog input bandwidth (3dB)			1200		MHz
DYNAMIC ACCURACY					
Offset Error	Auto correction disabled	–20	±6	20	mV
	Auto correction enabled	–1	0	1	mV
Offset temperature coefficient			–10		µV/°C
Gain error		–5	±0.6	5	%FS
Gain temperature coefficient			0.003		%FS/°C
Differential nonlinearity	f_{IN} = 230 MHz	–1	±0.8	2	LSB
Integral nonlinearity	f_{IN} = 230 MHz	-5	±2	5	LSB
CLOCK INPUT					
Input clock frequency		40		800	MHz
Input clock amplitude			2		Vpp
Input clock duty cycle		40%	50%	60%	
Internal clock biasing			0.9		V

7.7 Electrical Characteristics - Dynamic AC, Enabled

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 800 Msps, 50% clock duty cycle, AVDD33 = 3.3V, AVDDC / AVDD18 / DVDD / DVDDLVDS / IOVDD = 1.8 V, –1 dBFS differential input (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Auto Correction				Enabled		Vpp
DYNAMIC AC CHARACTERISTICS(1)						
SNR	Signal-to-Noise Ratio	f_{IN} = 10 MHz		61.7		dBFS
		f_{IN} = 100 MHz		61.7		
		f_{IN} = 230 MHz	58	61.3		
		f_{IN} = 450 MHz		60.7		
		f_{IN} = 700 MHz		59.8		
HD2,3	Second and third harmonic distortion	f_{IN} = 10 MHz		78		dBc
		f_{IN} = 100 MHz		77		
		f_{IN} = 230 MHz	67	77		
		f_{IN} = 450 MHz		76		
		f_{IN} = 700 MHz		74		
Non HD2,3	Spur free dynamic range (excluding second and third harmonic distortion Fs/2 – F_{IN} spur)	f_{IN} = 10 MHz		81		dBc
		f_{IN} = 100 MHz		79		
		f_{IN} = 230 MHz	67	78		
		f_{IN} = 450 MHz		78		
		f_{IN} = 700 MHz		76		

(1) SFDR and SNR calculations do not include the DC or Fs/2 bins when Auto Correction is disabled.

Electrical Characteristics - Dynamic AC, Enabled (continued)

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 800 Msps, 50% clock duty cycle, AVDD33 = 3.3V, AVDDC / AVDD18 / DVDD / DVDDLVDS / IOVDD = 1.8 V, –1 dBFS differential input (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IL	Fs/2-Fin interleaving spur	f_{IN} = 10 MHz		91		dBc
		f_{IN} = 100 MHz		81		
		f_{IN} = 230 MHz	63	74		
		f_{IN} = 450 MHz		72		
		f_{IN} = 700 MHz		69		
SINAD	Signal-to-noise and distortion ratio	f_{IN} = 10 MHz		61.6		dBFS
		f_{IN} = 100 MHz		61.4		
		f_{IN} = 230 MHz	57.7	61		
		f_{IN} = 450 MHz		60.5		
		f_{IN} = 700 MHz		59.5		
THD	Total Harmonic Distortion	f_{IN} = 10 MHz		75		dBc
		f_{IN} = 100 MHz		73		
		f_{IN} = 230 MHz	66	73		
		f_{IN} = 450 MHz		74		
		f_{IN} = 700 MHz		72		
IMD3	Inter modulation distortion	F_{in} = 169.5 and 170.5 MHz, -7dBFS		76		dBFS
		F_{in} = 649.5 and 650.5 MHz, -7dBFS		70		
	Crosstalk			90		dB
ENOB	Effective number of bits	f_{IN} = 230 MHz		9.8		LSB

7.8 Electrical Characteristics- Dynamic AC, Disabled

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Auto correction				Disabled		Vpp
DYNAMIC AC CHARACTERISTICS (1)						
SNR	Signal to Noise Ratio	f_{IN} = 10 MHz		61.8		dBFS
		f_{IN} = 100 MHz		61.8		
		f_{IN} = 230 MHz		61.5		
		f_{IN} = 450 MHz		61.1		
		f_{IN} = 700 MHz		60.6		
HD2,3	Second and third harmonic distortion	f_{IN} = 10 MHz		80		dBc
		f_{IN} = 100 MHz		77		
		f_{IN} = 230 MHz		79		
		f_{IN} = 450 MHz		77		
		f_{IN} = 700 MHz		75		
Non HD2,3	Spur Free Dynamic Range (excluding second and third harmonic distortion Fs/2 – F_{IN} spur)	f_{IN} = 10 MHz		83		dBc
		f_{IN} = 100 MHz		81		
		f_{IN} = 230 MHz		79		
		f_{IN} = 450 MHz		79		
		f_{IN} = 700 MHz		77		

(1) SFDR and SNR calculations do not include the DC or Fs/2 bins when Auto Correction is disabled.

Electrical Characteristics- Dynamic AC, Disabled (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IL	Fs/2-Fin interleaving spur	f_{IN} = 10 MHz		84		dBc
		f_{IN} = 100 MHz		80		
		f_{IN} = 230 MHz		75		
		f_{IN} = 450 MHz		71		
		f_{IN} = 700 MHz		69		
SINAD	Signal to noise and distortion ratio	f_{IN} = 10 MHz		61.7		dBFS
		f_{IN} = 100 MHz		61.6		
		f_{IN} = 230 MHz		61.3		
		f_{IN} = 450 MHz		61		
		f_{IN} = 700 MHz		60.3		
THD	Total Harmonic Distortion	f_{IN} = 10 MHz		77		dBc
		f_{IN} = 100 MHz		75		
		f_{IN} = 230 MHz		74		
		f_{IN} = 450 MHz		75		
		f_{IN} = 700 MHz		72		
IMD3	Inter modulation distortion	F_{in} = 169.5 and 170.5 MHz, -7dBFS		76		dBFS
		F_{in} = 649.5 and 650.5 MHz, -7dBFS		72		
	Crosstalk			90		dB
ENOB	Effective number of bits	f_{IN} = 230 MHz		9.8		LSB

7.9 Electrical Characteristics - Over-Drive Recovery Error, Sample Timing

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 800Msps, 50% clock duty cycle, AVDD33 = 3.3 V, AVDDC/AVDD18/DVDD/DVDDLVDS/IOVDD = 1.8 V, –1 dBFS differential input (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OVER-DRIVE RECOVERY ERROR					
Input overload recovery	Recovery to within 1% (of final value) for 6dB overload with sine wave input		2		Output Clock
SAMPLE TIMING CHARACTERISTICS					
Aperture Jitter	Sample uncertainty		100		fs rms
Data Latency	ADC sample to digital output, auto correction disabled		38		Clock Cycles
	ADC sample to digital output, auto correction enabled		50		
	ADC sample to digital output, Decimation filter enabled, Auto correction disabled		74		Sampling Clock Cycles
Over-range Latency	ADC sample to over-range output		12		Clock Cycles

7.10 Electrical Characteristics - Digital Inputs, Digital Outputs

The DC specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1. AVDD33 = 3.3 V, AVDDC/AVDD18/DVDD/DVDDLVDS/IOVDD = 1.8 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS – SRESET, SCLK, SDENB, SDIO, ENABLE						
	High-level input voltage	All digital inputs support 1.8-V and 3.3-V logic levels.	0.7 x IOVDD			V
	Low-level input voltage				0.3 x IOVDD	V
	High-level input current		–50		200	µA
	Low-level input current		–50		50	µA
	Input capacitance			5		pF
DIGITAL OUTPUTS – SDO						
	High-level output voltage	I_{load} = -100 µA	IOVDD – 0.2			V
		I_{load} = -2 mA	0.8 x IOVDD			
	Low-level output voltage	I_{load} = 100 µA			0.2	V
		I_{load} = 2 mA			0.22 x IOVDD	
DIGITAL INPUTS – SYNCP/N						
V_{ID}	Differential input voltage		250	350	450	mV
V_{CM}	Input common-mode voltage		1.125	1.2	1.375	V
t_{SU}			500			ps
DIGITAL OUTPUTS – DA[11:0]P/N, DACLKP/N, OVRAP/N, SYNCOUTP/N						
V_{OD}	Output differential voltage	I_{OUT} = 3.5 mA	250	350	450	mV
V_{OCM}	Output common-mode voltage	I_{OUT} = 3.5 mA	1.125	1.25	1.375	V
t_{su}		F_S = 800 Msps, Data valid to zero-crossing of DACLK	230	450		ps
t_h		F_S = 800 Msps, Zero-crossing of DACLK to data becoming invalid	230	410		ps
t_{PD}		F_S = 800 Msps, CLKIN falling edge to DACLK, DBCLK rising edge	3.36	3.69	3.92	ns
t_{RISE}		10% - 90%	100	150	200	ps
t_{FALL}		90% - 10%	100	150	200	ps

7.11 Serial Register Write Timing Requirements

		MIN	MAX	UNIT
f_{SCLK}	SCLK frequency (equal to 1/tSCLK)	> DC	20	MHz
t_{SLOADS}	SDENB to SCLK setup time	25		ns
t_{SLOADH}	SCLK to SDENB hold time	25		ns
t_{DSU}	SDIO setup time	25		ns
t_{DH}	SDIO hold time	25		ns

7.12 Reset Timing Requirements

			MIN	NOM	MAX	UNIT
t_1	Power-on delay	Delay from power up to active low RESET pulse	3			ms
t_2	Reset pulse width	Active low RESET pulse width	20			ns
t_3	Register write delay	Delay from RESET disable to SDENb active	100			ns

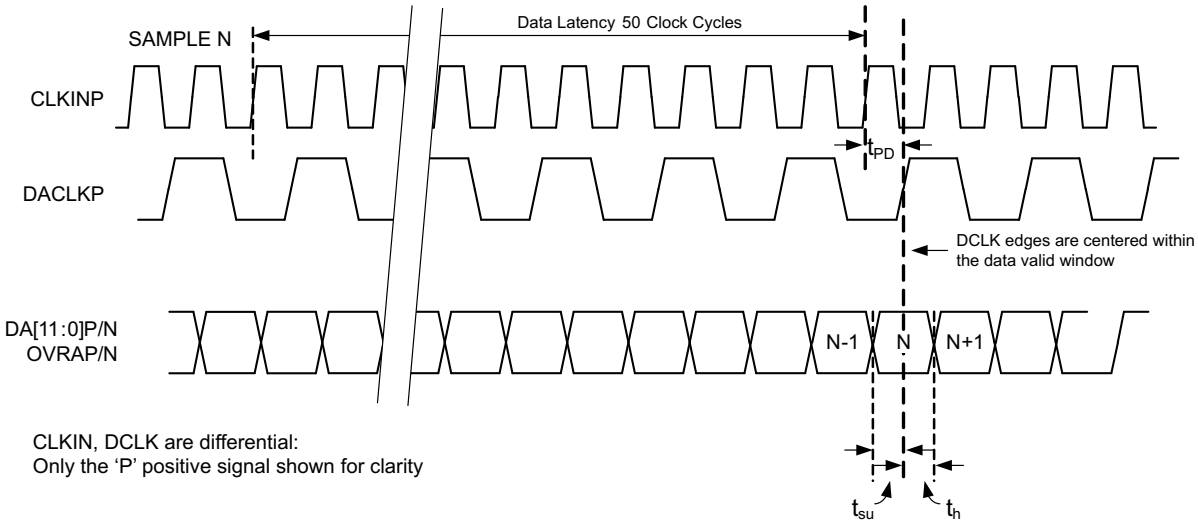


Figure 1. Timing Diagram for 12-Bit DDR Output

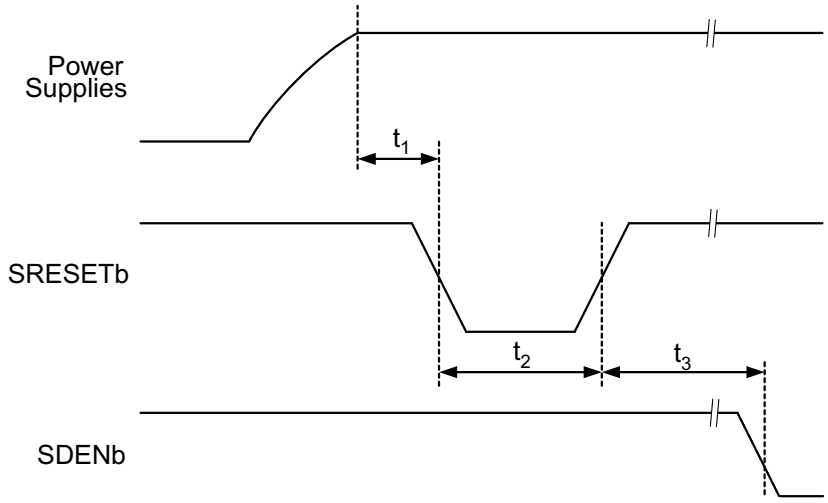


Figure 2. Device Initialization Timing Diagram

7.13 Typical Characteristics

Typical values at TA = +25°C, full temperature range is T_{MIN} = -40°C to T_{MAX} = +85°C, ADC sampling rate = 800 Msps, 50% clock duty cycle, AVDD33 = 3.3 V, AVDDC /AVDD18 / DVDD / DVDDLVDS / IOVDD = 1.8 V, -1dBFS differential input, unless otherwise noted.

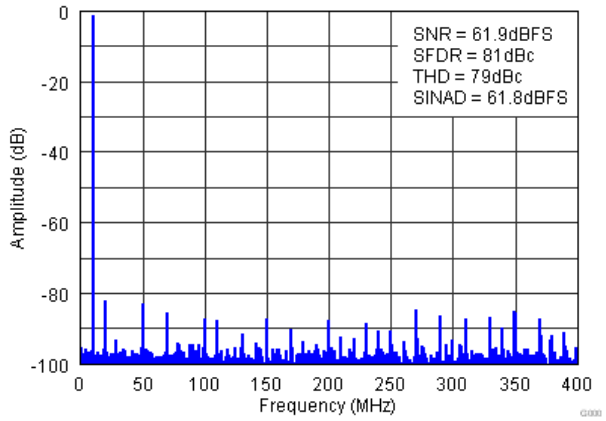


Figure 3. FFT for 10-MHz Input Signal (Auto On)

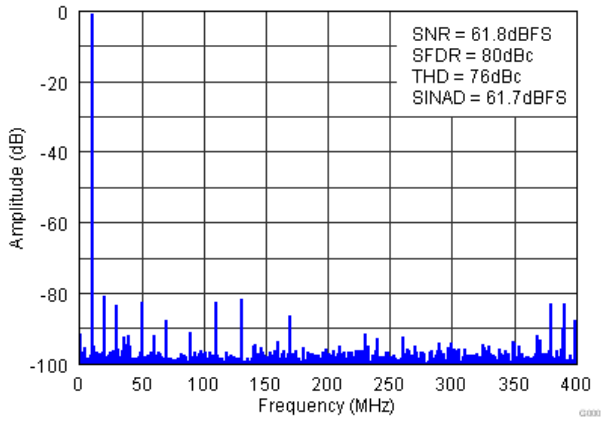


Figure 4. FFT for 10-MHz Input Signal (Auto Off)

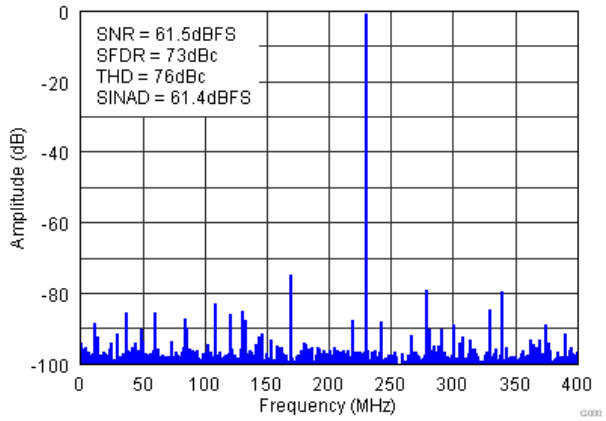


Figure 5. FFT for 230-MHz Input Signal (Auto On)

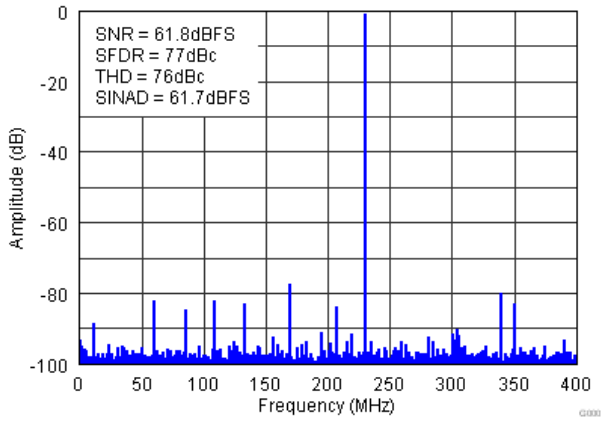


Figure 6. FFT for 230-MHz Input Signal (Auto Off)

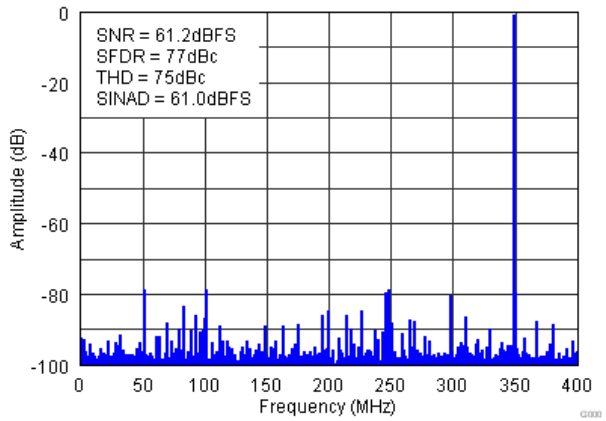


Figure 7. FFT for 450-MHz Input Signal (Auto On)

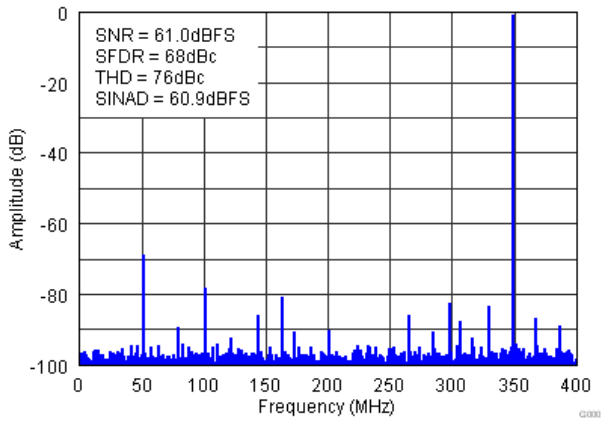


Figure 8. FFT for 450-MHz Input Signal (Auto Off)

Typical Characteristics (continued)

Typical values at TA = +25°C, full temperature range is T_{MIN} = -40°C to T_{MAX} = +85°C, ADC sampling rate = 800 Msps, 50% clock duty cycle, AVDD33 = 3.3 V, AVDDC /AVDD18 / DVDD / DVDDLVDS / IOVDD = 1.8 V, -1dBFS differential input, unless otherwise noted.

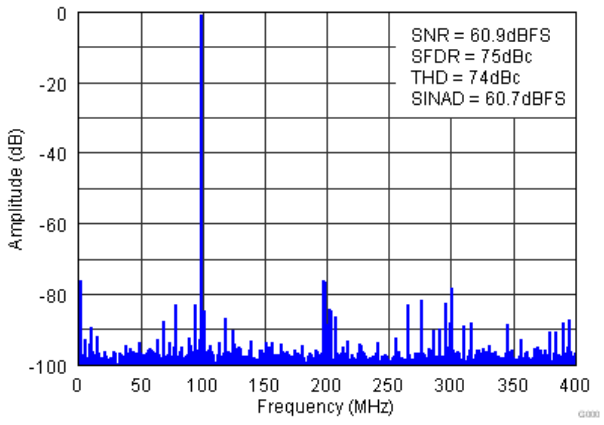


Figure 9. FFT for 700-MHz Input Signal (Auto On)

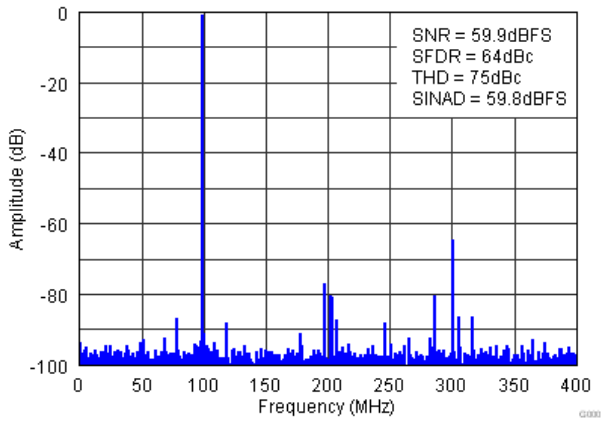


Figure 10. FFT for 700-MHz Input Signal (Auto Off)

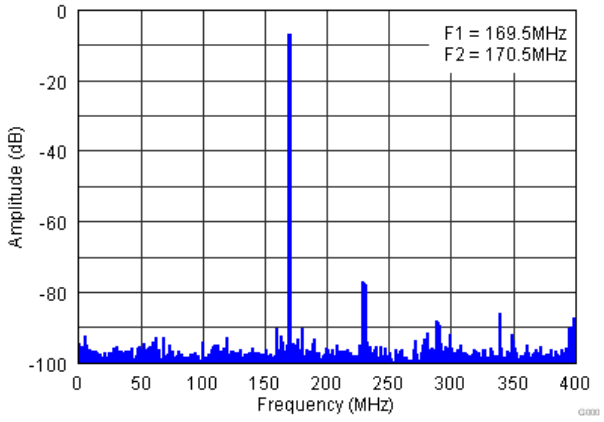


Figure 11. FFT for Two Tone Input Signal (Auto On)

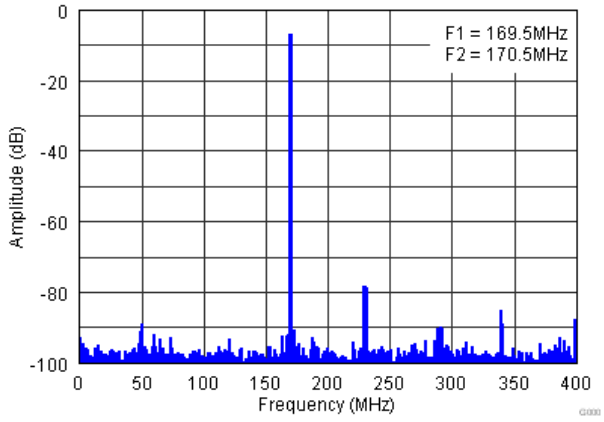


Figure 12. FFT for Two Tone Input Signal (Auto Off)

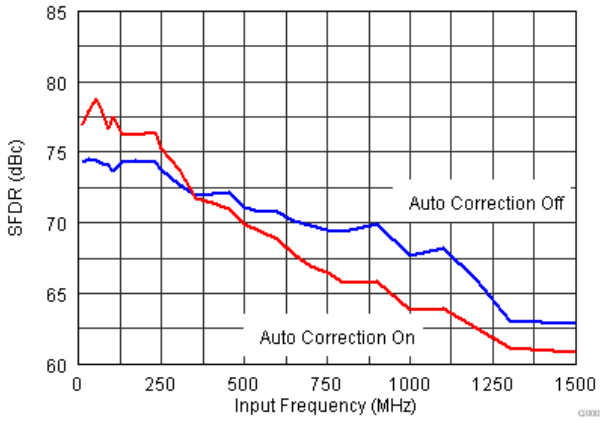


Figure 13. SFDR vs Input Frequency

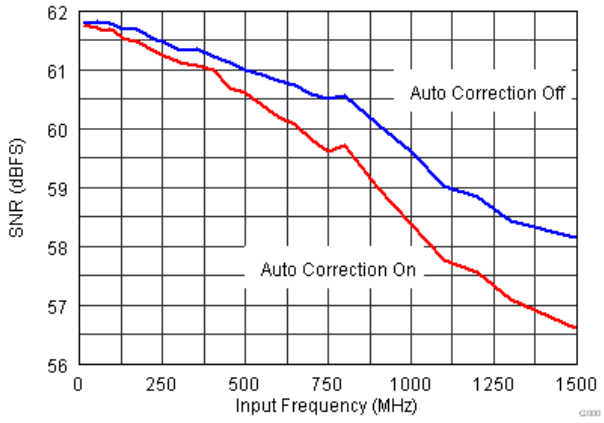


Figure 14. SNR vs Input Frequency

Typical Characteristics (continued)

Typical values at TA = +25°C, full temperature range is T_{MIN} = -40°C to T_{MAX} = +85°C, ADC sampling rate = 800 Msps, 50% clock duty cycle, AVDD33 = 3.3 V, AVDDC /AVDD18 / DVDD / DVDDLVDS / IOVDD = 1.8 V, -1dBFS differential input, unless otherwise noted.

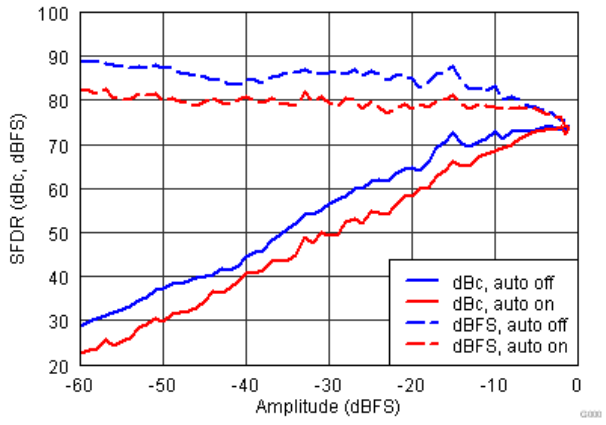


Figure 15. SFDR vs Amplitude (f_{in} = 230 MHz)

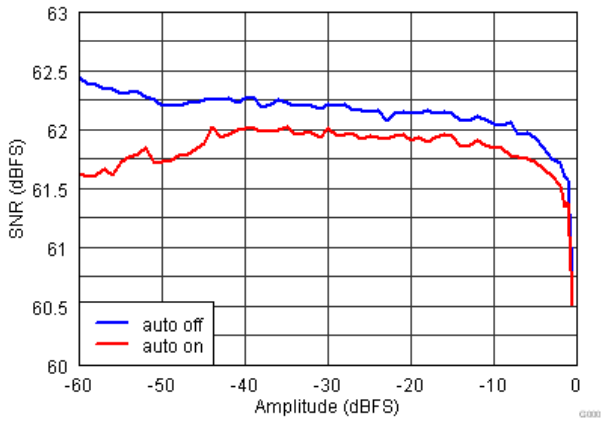


Figure 16. SNR vs Amplitude (f_{in} = 230 MHz)

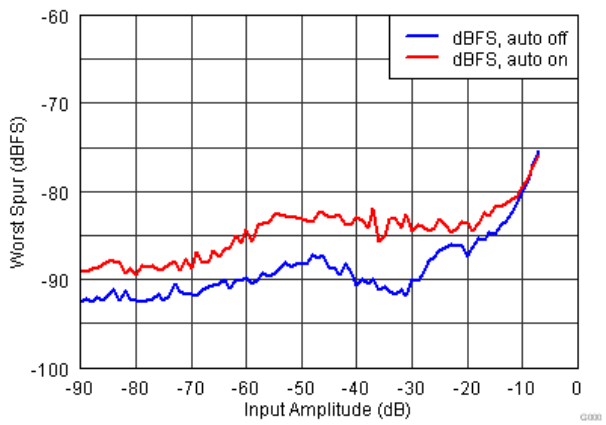


Figure 17. Tow Tone Performance Across Input Amplitude (f_{in} = 170 MHz)

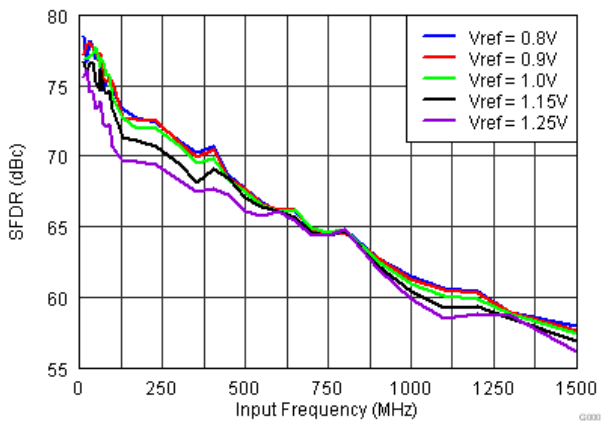


Figure 18. SFDR vs Vref (Auto On)

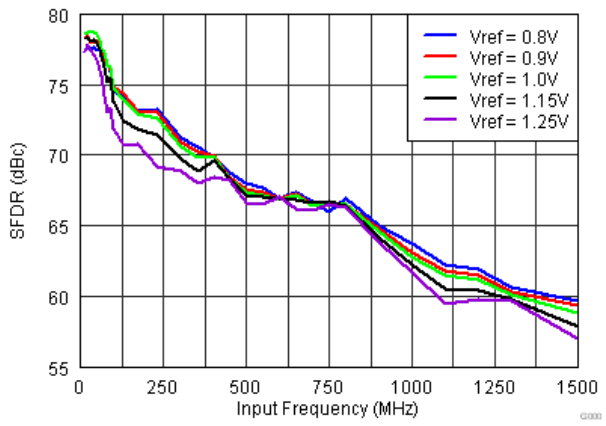


Figure 19. SFDR vs Vref (Auto Off)

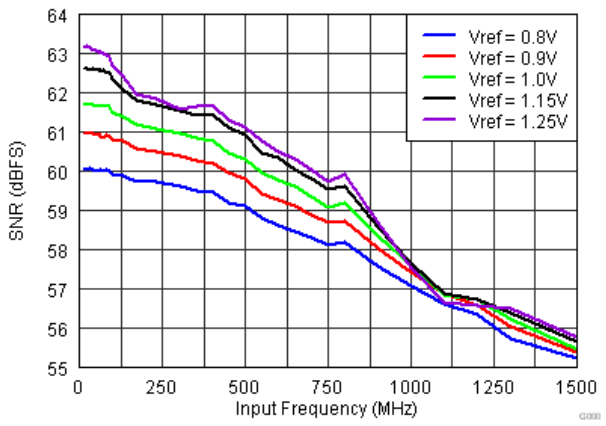


Figure 20. SNR vs Vref (Auto On)

Typical Characteristics (continued)

Typical values at TA = +25°C, full temperature range is T_{MIN} = -40°C to T_{MAX} = +85°C, ADC sampling rate = 800 Msps, 50% clock duty cycle, AVDD33 = 3.3 V, AVDDC /AVDD18 / DVDD / DVDDLVDS / IOVDD = 1.8 V, -1dBFS differential input, unless otherwise noted.

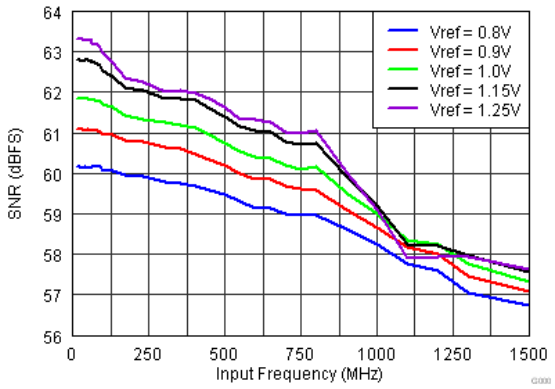


Figure 21. SNR vs Vref (Auto Off)

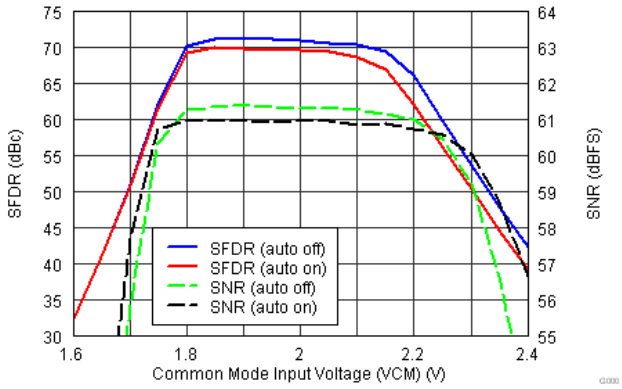


Figure 22. Performance Across Input Common-Mode Voltage (f_{in} = 230 MHz)

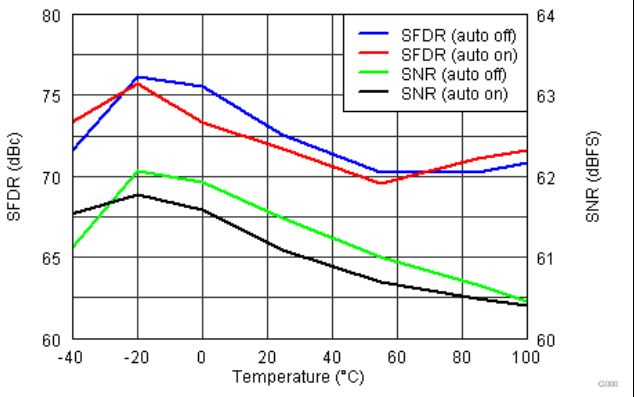


Figure 23. Performance Across Temperature (f_{in} = 230 MHz)

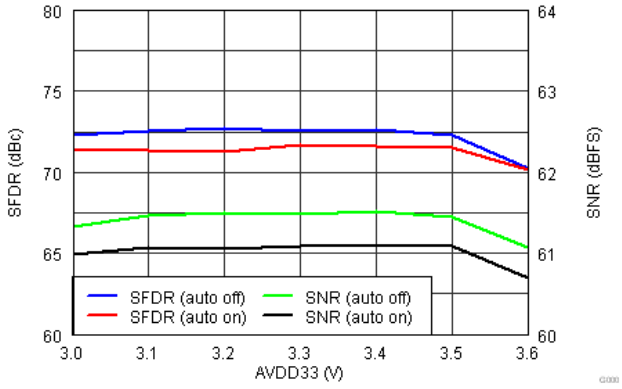


Figure 24. Performance Across AVDD33 (f_{in} = 230 MHz)

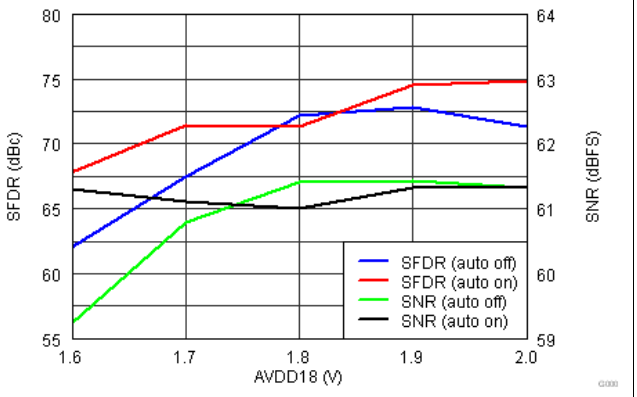


Figure 25. Performance Across AVDD18 (f_{in} = 230MHz)

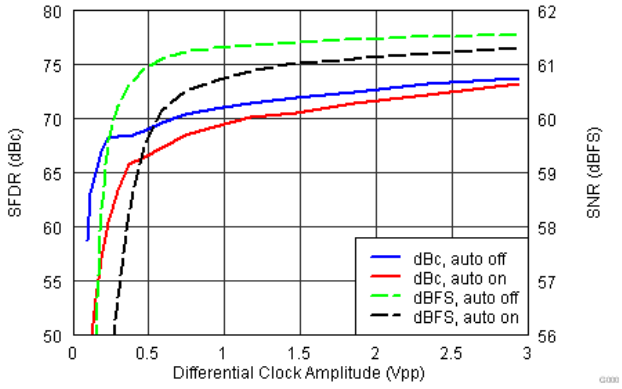


Figure 26. Performance Across Clock Amplitude

Typical Characteristics (continued)

Typical values at TA = +25°C, full temperature range is T_{MIN} = -40°C to T_{MAX} = +85°C, ADC sampling rate = 800 Msps, 50% clock duty cycle, AVDD33 = 3.3 V, AVDDC /AVDD18 / DVDD / DVDDLVDS / IOVDD = 1.8 V, -1dBFS differential input, unless otherwise noted.

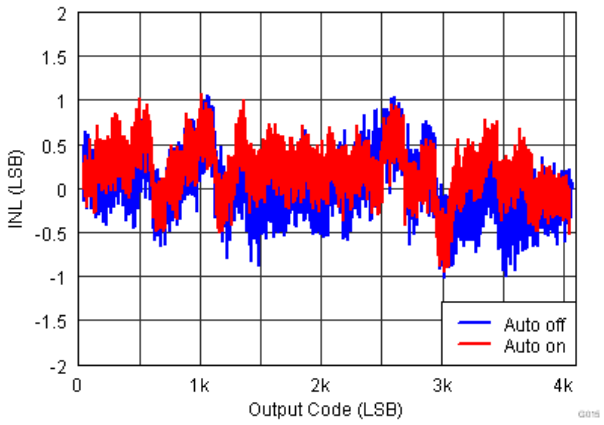


Figure 27. INL

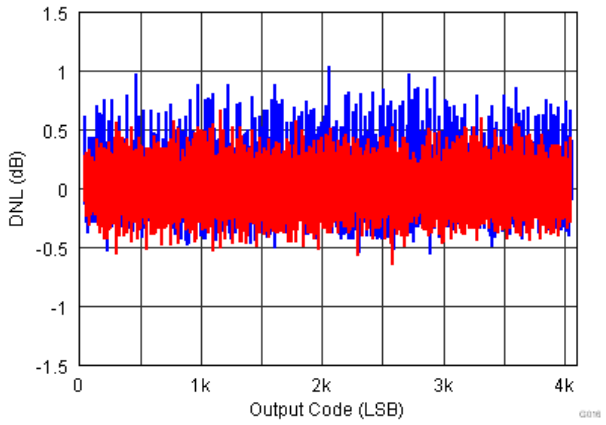


Figure 28. DNL

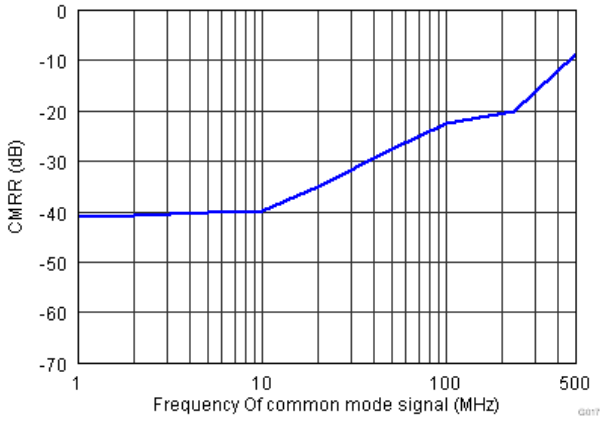


Figure 29. CMRR Across Frequency

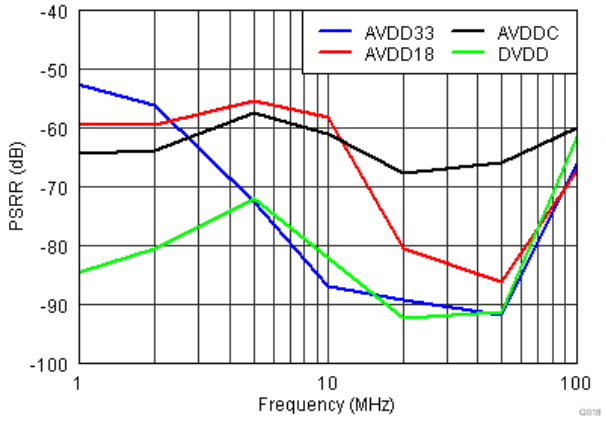


Figure 30. PSRR Across Frequency

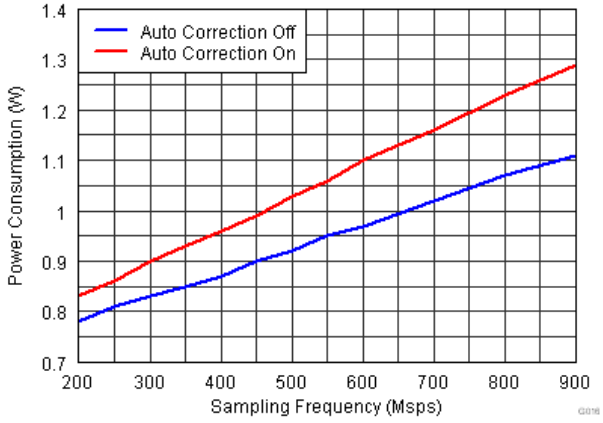


Figure 31. Power Across Sampling Frequency

Typical Characteristics (continued)

Typical values at TA = +25°C, full temperature range is T_{MIN} = -40°C to T_{MAX} = +85°C, ADC sampling rate = 800 Msps, 50% clock duty cycle, AVDD33 = 3.3 V, AVDDC /AVDD18 / DVDD / DVDDLVDS / IOVDD = 1.8 V, -1dBFS differential input, unless otherwise noted.

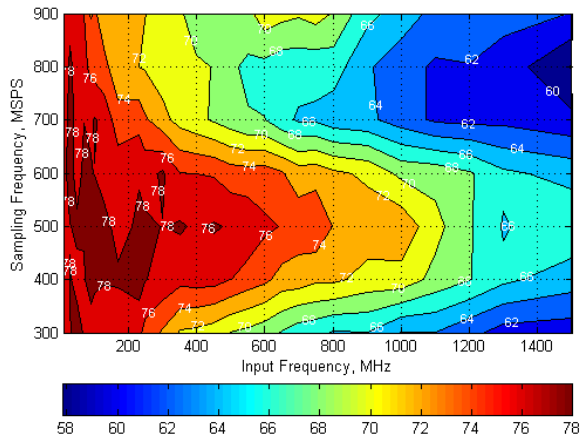


Figure 32. SFDR Across Input and Sampling Frequencies (Auto On)

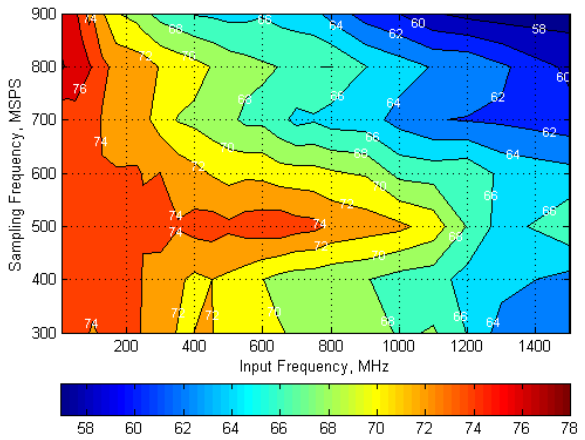


Figure 33. SFDR Across Input and Sampling Frequencies (Auto Off)

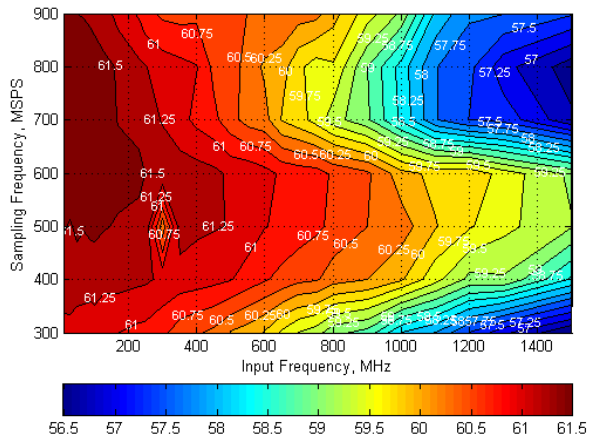


Figure 34. SNR Across Input and Sampling Frequencies (Auto On)

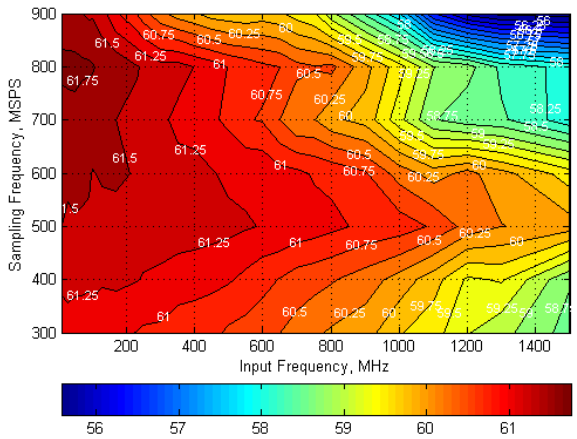


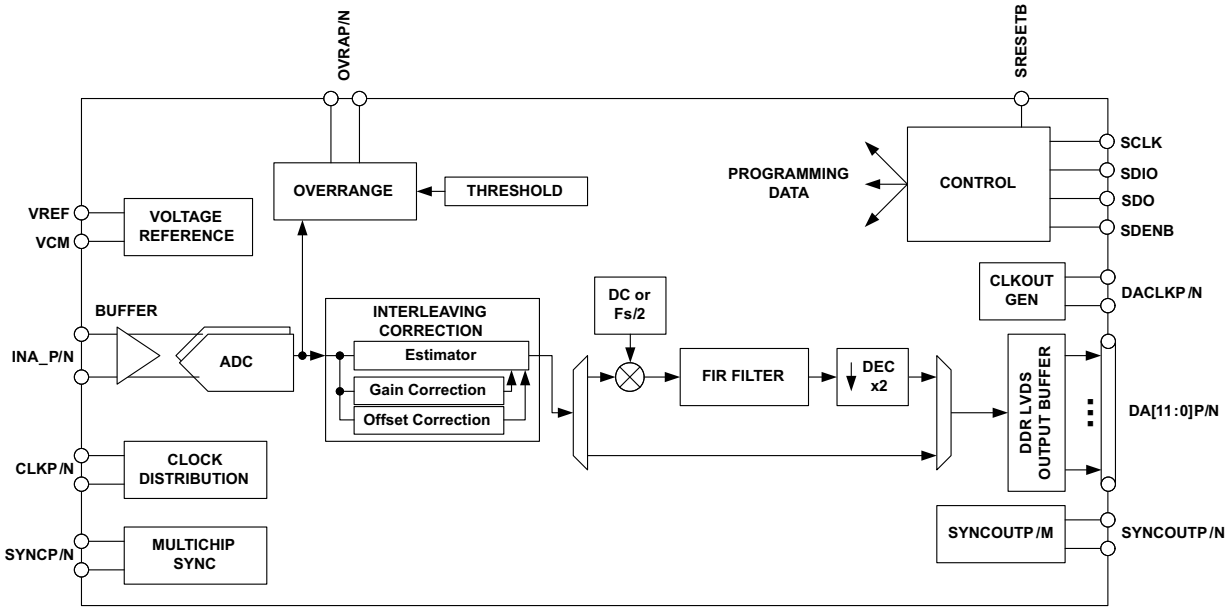
Figure 35. SNR Across Input and Sampling Frequencies (Auto On)

8 Detailed Description

8.1 Overview

The ADS5401 is a wide bandwidth 12-bit 800-Msps single-channel ADC. Designed for high SFDR, the ADS has low-noise performance and outstanding spurious-free dynamic range over a large input frequency. The buffered analog input provides uniform input impedance across a wide frequency range while minimizing sample-and-hold glitch energy. The ADC also provides an option to decimate the output data by two.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Test Pattern Output

The ADS5401 can be configured to output different test patterns that can be used to verify the digital interface is connected and working properly. To enable test pattern mode, high performance mode 1 has to be disabled first through a SPI register write. Then different test patterns can be selected by configuring registers x3C, x3D and x3E. All three registers must be configured for the test pattern to work properly.

First set HP1 = 0 (Addr 0x01, D01).

Table 1. Test Pattern Register Configurations

REGISTER ADDRESS	ALL 0s	ALL 1s	TOGGLE (0xAAA => 0x555)	TOGGLE (0xFFF => 0x000)
0x3C	0x8000	0xBFFC	0x9554	0xBFFC
0x3D	0x0000	0x3FFC	0x2AA8	0x0000
0x3E	0x0000	0x3FFC	0x1554	0x3FFC

Table 2. Custom Test Patterns

REGISTER ADDRESS	CUSTOM PATTERN															
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
x3C	1	0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0	0
x3D	0	0													0	0
x3E	0	0													0	0

For normal operation, set HP1 = 1 (Addr 0x01, D01) and 0x3C, 0x3D, 0x3E all to 0.

8.3.2 Clock Input

The ADS5401 clock input can be driven differentially with a sine wave, LVPECL or LVDS source with little or no difference in performance. The common-mode voltage of the clock input is set to 0.9 V using internal 2-kΩ resistors. This allows for AC coupling of the clock inputs. The termination resistors should be placed as close as possible to the clock inputs in order to minimize signal reflections and jitter degradation.

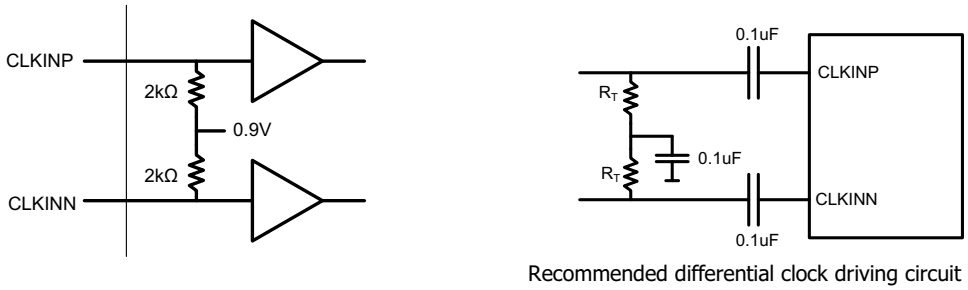


Figure 36. Recommended Differential Clock Driving Circuit

8.3.3 Analog Inputs

The ADS5401 analog signal input is designed to be driven differentially. The analog input pins have internal analog buffers that drive the sampling circuit. As a result of the analog buffer, the input pins present a high impedance input across a very wide frequency range to the external driving source which enables great flexibility in the external analog filter design as well as excellent 50-Ω matching for RF applications. The buffer also helps to isolate the external driving circuit from the internal switching currents of the sampling circuit which results in a more constant SFDR performance across input frequencies.

The common-mode voltage of the signal input is internally biased to 1.9 V using 500-Ω resistors which allows for AC coupling of the input drive network. Each input pin (INP, INM) must swing symmetrically between (VCM + 0.25 V) and (VCM – 0.25 V), resulting in a 1.0-Vpp (default) differential input swing. The input sampling circuit has a 3-dB bandwidth that extends up to 1.2 GHz.

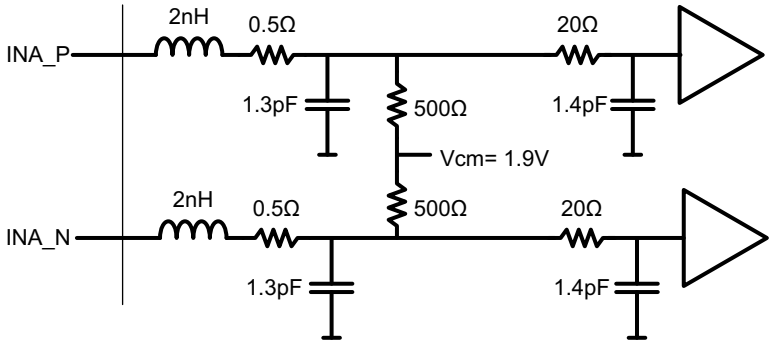


Figure 37. Equivalent Analog Input Circuit

8.3.4 Overrange Indication

The ADS5401 provides a fast overrange indication on the OVRA pins. The fast OVR is triggered if the input voltage exceeds the programmable overrange threshold and it gets presented after just 12 clock cycles enabling a quicker reaction to an overrange event. The OVR threshold can be configured using SPI register writes.

The input voltage level at which the overload is detected is referred to as the threshold and is programmable using the overrange threshold bits. The threshold at which fast OVR is triggered is (full-scale × [the decimal value of the FAST OVR THRESH bits] /16). After reset, the default value of the overrange threshold is set to 15 (decimal) which corresponds to a threshold of 0.56 dB below full scale (20 × log(15/16)).

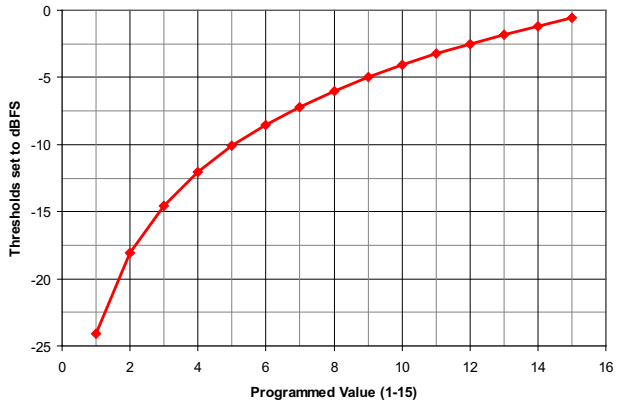


Figure 38. OVR Detection Threshold

8.3.5 Interleaving Correction

The two data converter channel consists of two interleaved ADCs each operating at half of the ADC sampling rate but 180º out of phase from each other. The front end track and hold circuitry is operating at the full ADC sampling rate which minimizes the timing mismatch between the two interleaved ADCs. In addition the ADS5401 is equipped with internal interleaving correction logic that can be enabled through SPI register write.

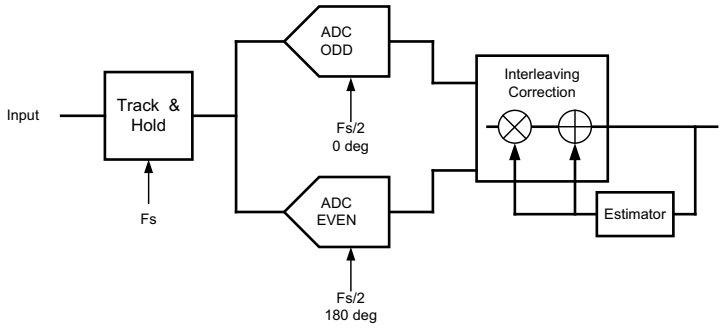


Figure 39. Interleaving Correction Circuit

The interleaving operation creates 2 distinct and interleaving products:

- Fs/2 – Fin: this spur is created by gain timing mismatch between the ADCs. Because internally the front end track and hold is operated at the full sampling rate, this component is greatly improved and mostly dependent on gain mismatch.
- Fs/2 Spur: due to offset mismatch between ADCs.

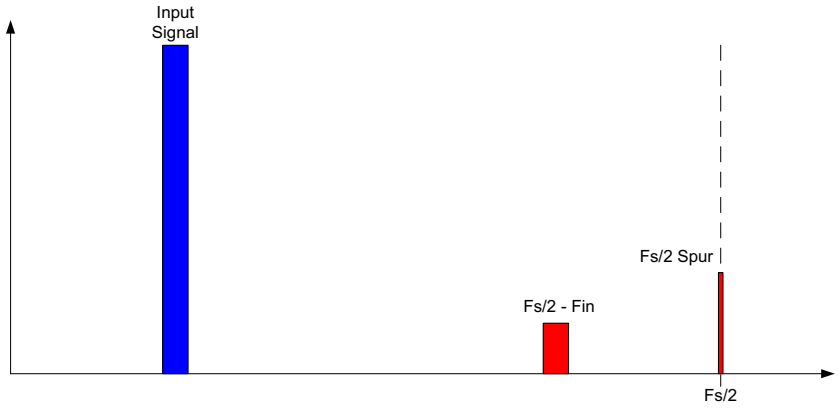


Figure 40. Interleaving Spur at Fs/2 due to Offset Mismatch

The auto correction loop can be enabled through SPI register write in address 0x01 and resetting the correction circuit in address 0x03. By default it is disabled for lowest possible power consumption.

The auto correction function yields best performance for input frequencies below 250 MHz.

8.3.6 Decimation Filter

There is an optional digital decimation filter in the data path as shown in Figure 41. The filter can be programmed as a lowpass or a highpass filter and the normalized frequency response of both filters is shown in Figure 42.

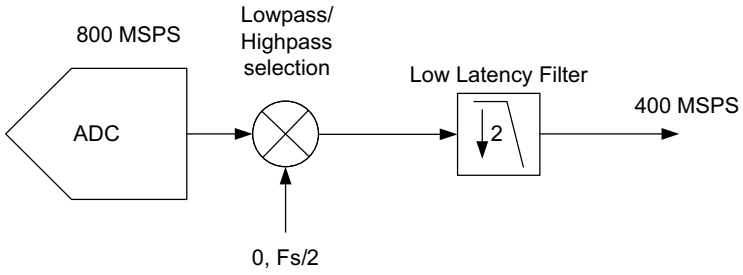


Figure 41. 2x Decimation Filter

The decimation filter response has a 0.1-dB pass band ripple with approximately 41% pass-band bandwidth. The stop-band attenuation is approximately 40 dB.

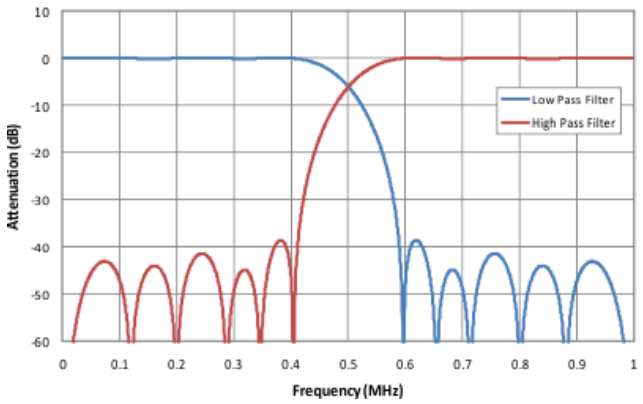


Figure 42. Decimation Filter Response

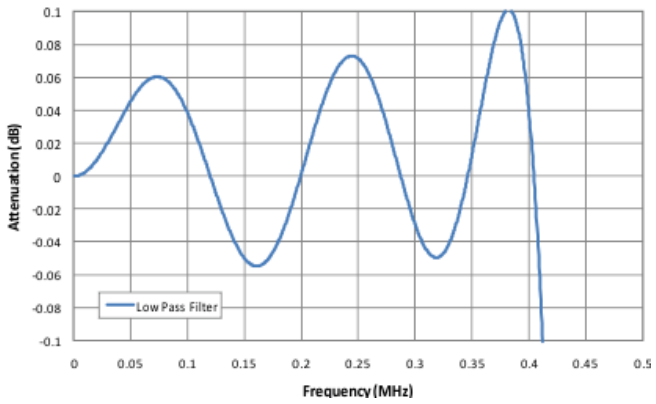


Figure 43. Decimation Filter Response

8.3.7 Multi Device Synchronization

The ADS5401 simplifies the synchronization of data from multiple ADCs in one common receiver. Upon receiving the initial SYNC input signal, the ADS5401 resets all the internal clocks and digital logic while also starting a SYNCOUT signal which operates on a 5-bit counter (32 clock cycles). Therefore by providing a common SYNC signal to multiple ADCs their output data can be synchronized as the SYNCOUT signal marks a specific sample with the same latency in all ADCs. The SYNCOUT signal then can be used in the receiving device to synchronize the FIFO pointers across the different input data streams. Thus the output data of multiple ADCs can be aligned properly even if there are different trace lengths between the different ADCs. By default ADS5401 is not configured for multi device synchronization. The ADC can be configured by setting the SYNCOUT enable bit (D2 config1) to 1 on all the ADCs.

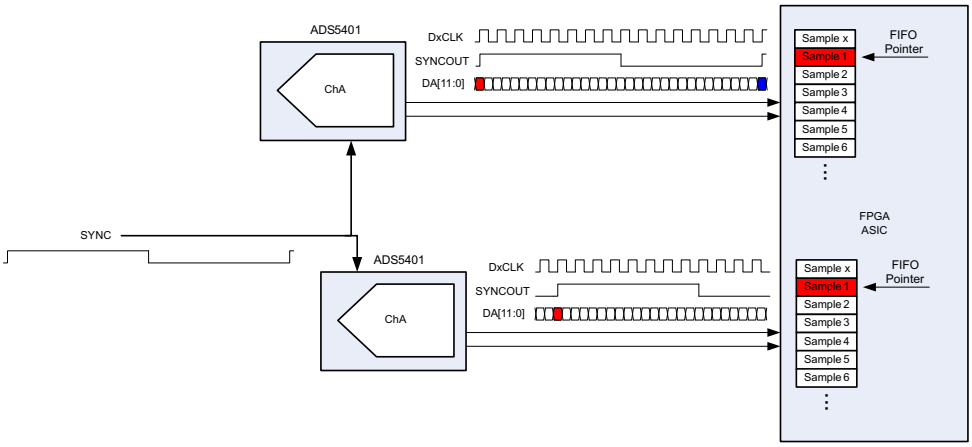


Figure 44. Multiple ADC Synchronization

The SYNC input signal should be a one time pulse to trigger the periodic 5-bit counter for SYNCOUT or a periodic signal repeating every 32 CLKIN clock cycles. It gets registered on the rising edge of the ADC input clock (CLKIN). Upon registering the initial rising edge of the SYNC signal, the internal clocks and logic get reset which results in invalid output data for 36 samples (1 complete sync cycle and 4 additional samples). The SYNCOUT signal starts with the next output clock (DACLK) rising edge and operates on a 5-bit counter. If a SYNCIN rising edge gets registered at a new position, the counter gets reset and SYNCOUT starts from the new position.

Because the ADS5401 output interface operates with a DDR clock, the synchronization can happen on the rising edge or falling edge sample. Synchronization on the falling edge sample will result in a half cycle clock stretch of DACLK. For convenience the SYNCOUT signal is available on the ChA output LVDS bus. When using decimation the SYNCOUT signal still operates on 32 clock cycles of CLKIN but since the output data is decimated by 2, only the first 18 samples should be discarded.

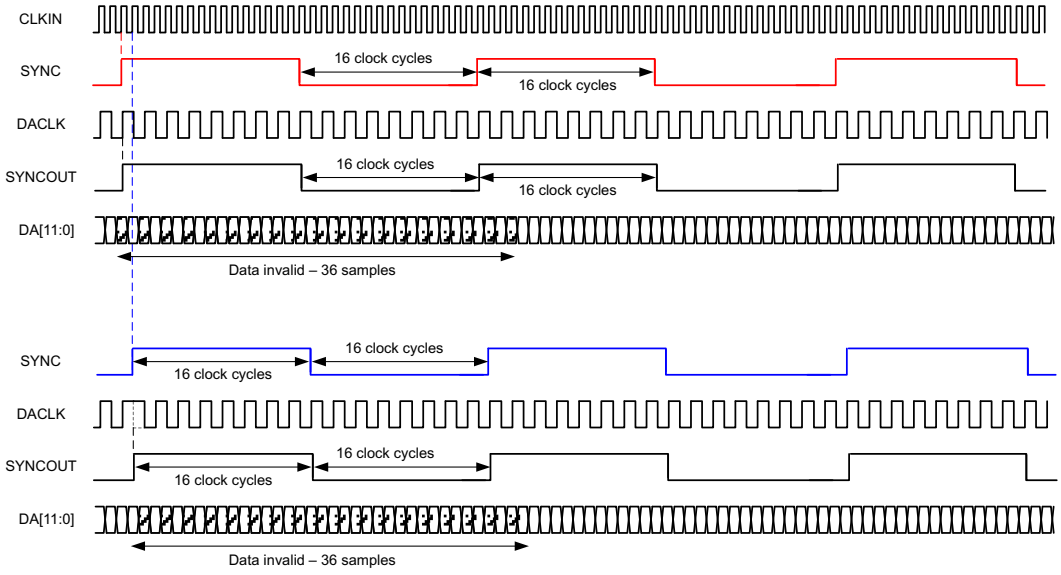


Figure 45. Multiple Device Synchronization Timing Diagram

8.4 Device Functional Modes

The ADS5401 has two main functional modes. The ADC can operate in Bypass mode in which sample rate and data-rate is the same or it can be programmed to operate in Decimate by 2x mode in which data rate is half of the sampling rate.

8.4.1 Power-Down Modes

The ADS5401 can be configured through SPI write (address x37) to a standby, light or deep sleep power mode which is controlled by the ENABLE pin. The sleep modes are active when the ENABLE pin goes low. Different internal functions stay powered up which results in different power consumption and wake up time between the two sleep modes.

Table 3. Power-Down Modes

SLEEP MODE	WAKE-UP TIME	POWER CONSUMPTION AUTO CORRECTION DISABLED	POWER CONSUMPTION AUTO CORRECTION ENABLED
Complete Shut Down	2.5 ms	7mW	7mW
Stand-by	100µs	7mW	7mW
Deep Sleep	20µs	465mW	530mW
Light Sleep	2µs	295mW	360mW

8.5 Programming

The serial interface (SIF) included in the ADS5401 is a simple 3 or 4 pin interface. In normal mode, 3 pins are used to communicate with the device. There is an enable (SDENB), a clock (SCLK) and a bidirectional IO port (SDIO). If the user would like to use the 4 pin interface one write must be implemented in the 3 pin mode to enable 4 pin communications. In this mode, the SDO pin becomes the dedicated output. The serial interface has an 8-bit address word and a 16-bit data word. The first rising edge of SCLK after SDENB goes low will latch the read/write bit. If a high is registered then a read is requested, if it is low then a write is requested. SDENB must be brought high again before another transfer can be requested. The signal diagram is shown below:

8.5.1 Device Initialization

After power up, TI recommends using the device through a hardware reset by applying a logic low pulse on the SRESETb pin (of width greater than 20ns), as shown in Figure 2. This resets all internal digital blocks (including SPI registers) to their default condition.

Recommended Device Initialization Sequence:

1. Power up
2. Reset ADS5401 using hardware reset.
3. Apply clock and input signal.
4. Set register 0x01 bit D15 to 1 (ChA Corr EN) to enable gain/offset correction circuit and other desired registers.
5. Set register 0x03 bit D14 to 1 (Start Auto Corr ChA). This clears and resets the accumulator values in the DC and gain correction loop.
6. Set register 0x03 bit D14 to 0 (Start Auto Corr ChA). This starts the DC and gain auto-correction loop.

8.5.2 Serial Register Write

The internal register of the ADS5401 can be programmed following these steps:

1. Drive SDENB pin low
2. Set the R/W bit to 0 (bit A7 of the 8 bit address)
3. Initiate a serial interface cycle specifying the address of the register (A6 to A0) whose content has to be written
4. Write 16bit data which is latched on the rising edge of SCLK

Programming (continued)

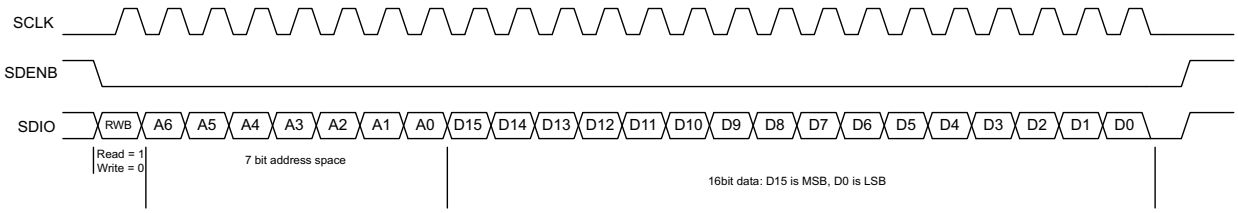


Figure 46. Serial Register Write Timing Diagram

8.5.3 Serial Register Readout

The device includes a mode where the contents of the internal registers can be read back using the SDO/SDIO pins. This read-back mode may be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC.

1. Drive SDENB pin low
2. Set the RW bit (A7) to 1. This setting disables any further writes to the registers
3. Initiate a serial interface cycle specifying the address of the register (A6 to A0) whose content has to be read.
4. The device outputs the contents (D15 to D0) of the selected register on the SDO/SDIO pin
5. The external controller can latch the contents at the SCLK rising edge.
6. To enable register writes, reset the RW register bit to 0.

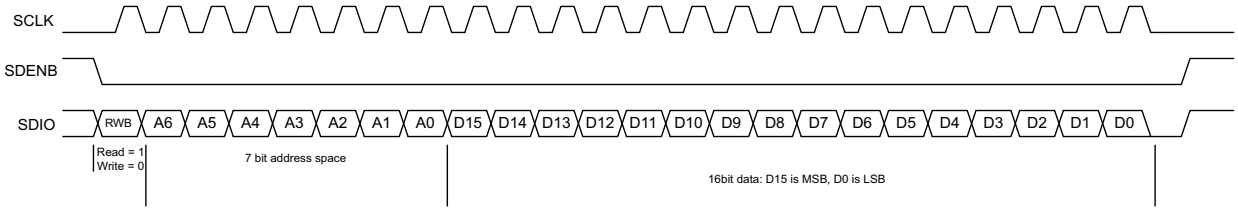


Figure 47. Serial Register Read Timing Diagram

8.6 Register Maps

Table 4. Serial Register Map(1)

Register Address	Register Data															
A7–A0 IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	3- / 4-wire SPI	Decimation Filter EN	0	ChA High/ Lowpass	0	0	0	0	0	0	0	0	0	0	0	0
1	ChA Corr EN	0	0	0	0	0	0	0	0	0	0	0	Data Format	0	Hp Mode1	0
2	0	0	0	0	0	Overrange threshold				0	0	0	0	0	0	0
3	0	Start Auto Corr ChA	0	0	1	0	1	1	0	0	0	1	1	0	0	0
E	Sync Select														0	0
F	Sync Select				0	0	0	0	0	VREF Set			0	0	0	0
2B	0	0	0	0	0	0	0	Temp Sensor								
2C	Reset															
37	Sleep Modes						0	0	0	0	0	0	0	0	0	0
38	HP Mode2									BIAS EN	SYNC EN	LP Mode 1	1	1	1	1
3A	LVDS Current Strength			LVDS SW		Internal LVDS Termination		0	0	0	0	DACLK EN	LP Mode 2	0	OVRA EN	LP Mode 3
66	LVDS Output Bus A EN															

(1) Multiple functions in a register can be programmed in a single write operation.

8.6.1 Register Name: Config0 - Address: 0×00, Default = 0×00

Figure 48. Register Config0 Format

Register Address	Register Data															
A7-A0 in hex	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	3-/4-wire SPI	Dec-ima-tion Filter EN	0	ChA High/ Low Pass	0	0	0	0	0	0	0	0	0	0	0	0

D15 **3-/4-Wire SPI** Enables 4-bit serial interface when set
Default 0

0 3-wire SPI is used with SDIO pin operating as bidirectional I/O port

1 4-wire SPI is used with SDIO pin operating as data input and SDO pin as data output port.

D14 **Decimation Filter EN** 2x decimation filter is enabled when bit is set
Default 0

0 Normal operation with data output at full sampling rate

1 2x decimation filter enabled

D12 **ChA Highpass or Lowpass** (Decimation filter must be enabled first: set bit D14)
Default 0

0 Lowpass

1 Highpass

8.6.2 Register Name: Config1 - Address: 0×01, Default = 0×00

Figure 49. Register Config1 Format

Register Address	Register Data															
A7-A0 in hex	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	ChA Corr EN	0	0	0	0	0	0	0	0	0	0	0	Data Format	0	HP Mode1	0

D15 **ChA Corr EN (should be enabled for maximum performance)**
Default 0

0 Auto correction disabled

1 Auto correction enabled

D3 **Data Format**
Default 0

0 Two's complement

1 Offset Binary

D2 **SYNCOUT Enable**

Default 0

1 Must be set to 1 to enable SYNCOUT signal

D1 **HP Mode 1**
Default 0

1 Must be set to 1 for optimum performance

8.6.3 Register Name: Config2 - Address: 0×02, Default = 0×780

Figure 50. Register Config2 Format

Register Address	Register Data															
A7-A0 in hex	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
2	0	0	0	0	0	Over-range threshold				0	0	0	0	0	0	0

D10-D7 **Over-range threshold** The over-range detection is triggered 12 output clock cycles after the overload condition occurs. The threshold at which the OVR is triggered = 1.0V x [decimal value of <Over-range threshold>]/16. After power up or reset, the default value is 15 (decimal) which corresponds to a OVR threshold of 0.56dB below fullscale (20*log(15/16)). This OVR threshold is applicable to both channels.

Default 1111

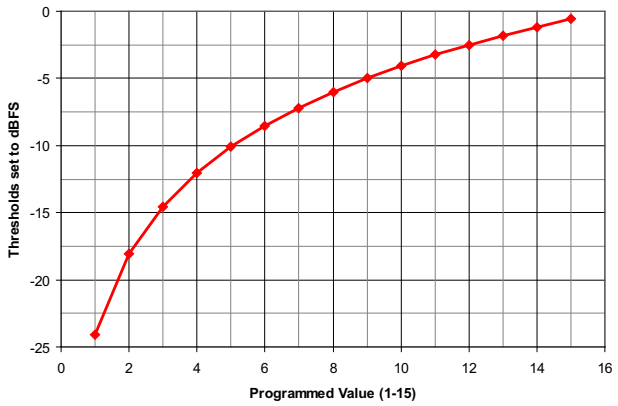


Figure 51. OVR Detection Threshold

8.6.4 Register Name: 3 - Address: 0x03

Figure 52. Register 3 Format

Register Address	Register Data															
A7-A0 in hex	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
3	0	Start Auto Coff ChA	0	0	1	0	1	1	0	0	0	1	1	0	0	0

D14	**Start Auto Corr ChA** Default 1	Starts DC offset and Gain correction loop for ChA
0	Starts the DC offset and Gain correction loops	
1	Clears DC offset correction value to 0 and Gain correction value to 1	
D11, 9, 8, 4, 3	Must be set to 1 for maximum performance Default 1	

8.6.5 Register Name: E - Address: 0x0E

Figure 53. Register E Format

Register Address	Register Data															
A7-A0 in hex	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
E	Sync Select														0	0

D15-D2	**Sync Select** Default 1010 1010 1010 10	Sync selection for the clock generator block (also need to see address 0x0F)
0000 0000 0000 00	Sync is disabled	
0101 0101 0101 01	Sync is set to one shot (one time synchronization only)	
1010 1010 1010 10	Sync is derived from SYNC input pins	
1111 1111 1111 11	not supported	

8.6.6 Register Name: F - Address: 0x0F

Figure 54. Register F Format

Register Address	Register Data															
A7-A0 in hex	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
F	Sync Select				0	0	0	0	0	VREF Sel			0	0	0	0

D15-D12	**Sync Select** Default 1010	Sync selection for the clock generator block
0000	Sync is disabled	
0101	Sync is set to one shot (one time synchronization only)	
1010	Sync is derived from SYNC input pins	
1111	not supported	
D6-D4	**VREF SEL** Default 000	Internal voltage reference selection
000	1.0V	
001	1.25V	
010	0.9V	
011	0.8V	
100	1.15V	
Others	external reference	

8.6.7 Register Name: 2B - Address: 0x2B

Figure 55. Register 2B Format

Register Address	Register Data															
A7-A0 in hex	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
2B	0	0	0	0	0	0	0	Temp Sensor								

D8-D0	**Temp Sensor**	Internal temperature sensor value – read only

8.6.8 Register Name: 2C - Address: 0x2C

Figure 56. Register 2C Format

Register Address	Register Data															
A7-A0 in hex	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
2C	Reset															

D15-D0	**Reset** Default 0000	This is a software reset to reset all SPI registers to their default value. Self clears to 0.
1101001011110000		Perform software reset

8.6.9 Register Name: 37 - Address: 0x37

Figure 57. Register 37 Format

Register Address	Register Data															
A7-A0 in hex	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
37	Sleep Modes						0	0	0	0	0	0	0	0	0	0

D15-D10	**Sleep Modes** Default 00	Sleep mode selection which is controlled by the ENABLE pin. Sleep modes are active when ENABLE pin goes low.
000000	Complete shut down	Wake up time 2.5 ms
100000	Stand-by mode	Wake up time 100 µs
110000	Deep sleep mode	Wake up time 20 µs
110101	Light sleep mode	Wake up time 2 µs

8.6.10 Register Name: 38 - Address: 0x38

Figure 58. Register 38 Format

Register Address	Register Data															
A7-A0 in hex	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
38	HP Mode 2									Bias EN	SYNC EN	LP Mode 1	1	1	1	1

D15-D7	**HP Mode 2** Default 111111111	
1	Set to 1 for normal operation	
D6	**BIAS EN** Default 1	Enables internal fuse bias voltages – can be disabled after power up to save power.
0	Internal bias powered down	
1	Internal bias enabled	
D5	**SYNC EN** Default 1	Enables the SYNC input buffer.
0	SYNC input buffer disabled	
1	SYNC input bffer enabled	
D4	**LP Mode 1** Default 1	Low power mode 1 to disable internal unused input buffer.
0	Internal input buffer disabled	
1	Internal input buffer enabled	
D3-D0	Reads back 1	

8.6.11 Register Name: 3A - Address: 0x3A

Figure 59. Register 3A Format

Register Address	Register Data															
A7-A0 in hex	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
3A	LVDS Current Strength			LVDS SW		Internal LVDS Termination		0	0	0	0	DACLK EN	LP Mode 2	0	OVRA EN	LP Mode 3

D15-D13	**LVDS Current Strength** Default 000		LVDS output current strength.
000	2 mA	100	3 mA
001	2.25 mA	101	3.25 mA
010	2.5 mA	110	3.5 mA
011	2.75 mA	111	3.75 mA
D12-D11	**LVDS SW** Default 01		LVDS driver internal switch setting – correct range must be set for setting in D15-D13
01	2 mA to 2.75 mA		
11	3mA to 3.75mA		
D10-D9	**Internal LVDS Termination** Default 00		Internal termination
00	2 kΩ		
01	200 Ω		
10	200 Ω		
11	100 Ω		
D4	**DACLK EN** Default 1		Enable DACLK output buffer
0	DACLK output buffer powered down		
1	DACLK output buffer enabled		
D3	**LP Mode 2** Default 1		Low power mode to disable unused internal output buffer
0	Internal output buffer disabled		
1	internal output buffer enabled		
D1	**OVRA EN** Default 1		Enable OVRA output buffer
0	OVRA output buffer powered down		
1	OVRA output buffer enabled		
D0	**LP Mode 3** Default 1		Low power mode to disable unused internal output buffer
0	Internal output buffer disabled		
1	Internal output buffer enabled		

8.6.12 Register Name: 66 - Address: 0x66

Figure 60. Register 66 Format

Register Address	Register Data															
A7-A0 in hex	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
66	LVDS Output Bus A EN															

D15-D0	**LVDS Output Bus A EN** Individual LVDS output pin power down for channel A Default FFFF
0	Output is powered down
1	Output is enabled
D15	Pins N7, P7 (no connect pins) which are not used and should be powered down for power savings
D14	Pins N6, P6 (no connect pins) which are not used and should be powered down for power savings
D13	SYNCOUTP/N (pins P9, N9)
D12	Pins P4, N4 (no connect pins) which are not used and should be powered down for power savings
D11-D0	corresponds to DA11-DA0

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

In the design of any application involving a high-speed data converter, particular attention should be paid to the design of the analog input, the clocking solution, and careful layout of the clock and analog signals. The ADS5401 evaluation module (EVM) is one practical example of the design of the analog input circuit and clocking solution, as well as a practical example of good circuit board layout practices around the ADC.

9.2 Typical Application

The analog inputs of the ADS5401 must be fully differential and biased to a desired common-mode voltage, VCM. Therefore, there will be a signal conditioning circuit for the analog input. If the amplitude of the input circuit is such that no gain is needed to make full use of the full-scale range of the ADC, then a transformer coupled circuit as in Figure 61 may be used with good results. The transformer coupling is inherently low-noise, and inherently AC-coupled so that the signal may be biased to VCM after the transformer coupling.

By using the simple drive circuit of Figure 61, uniform performance can be obtained over a wide frequency range. The buffers present at the analog inputs of the device help isolate the external drive source from the switching currents of the sampling circuit.

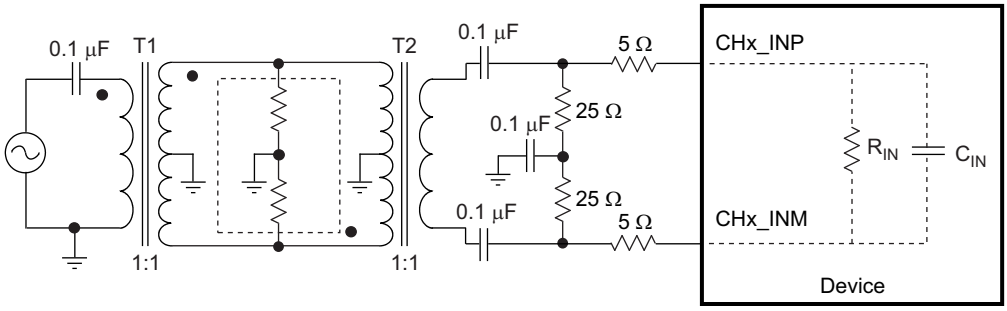


Figure 61. Input Drive Circuit

If signal gain is required, or the input bandwidth is to include the spectrum all the way down to DC such that AC coupling is not possible, then an amplifier-based signal conditioning circuit would be required. The figure below shows LMH3401 interfaced with ADS5401. LMH3401 is configured to have to Single-Ended input with a differential outputs follow by 1st Nyquist based low pass filter with 375MHz bandwidth. Power supply recommendations for the amplifier are also shown in Figure 62.

Typical Application (continued)

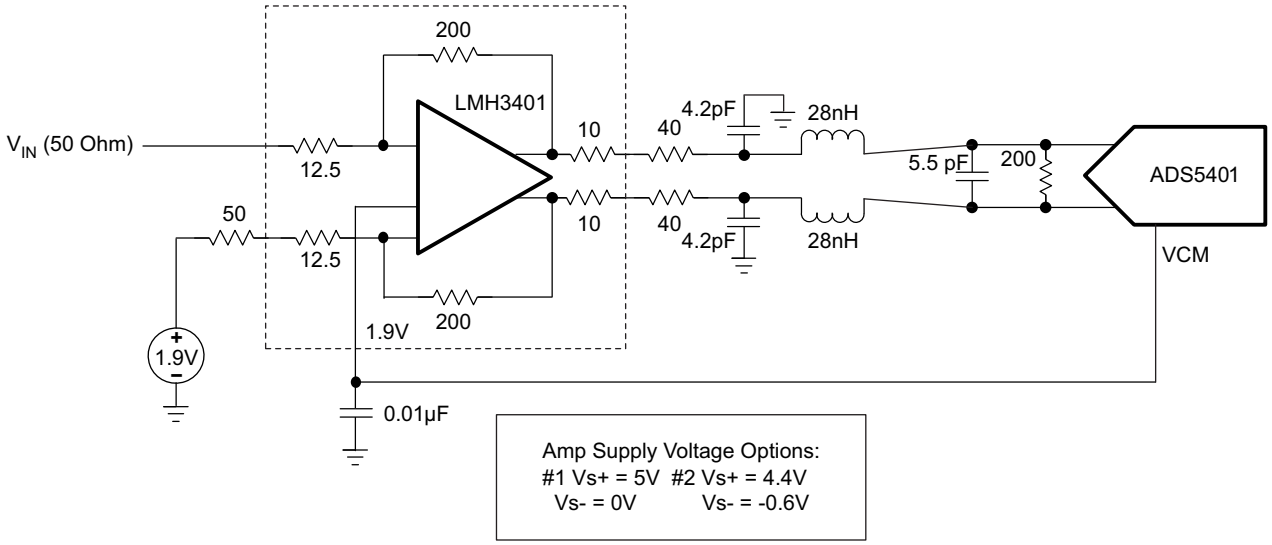


Figure 62. DC-Coupled Single-Ended to Differential Amplifier with 1st Nyquist Lowpass Filter

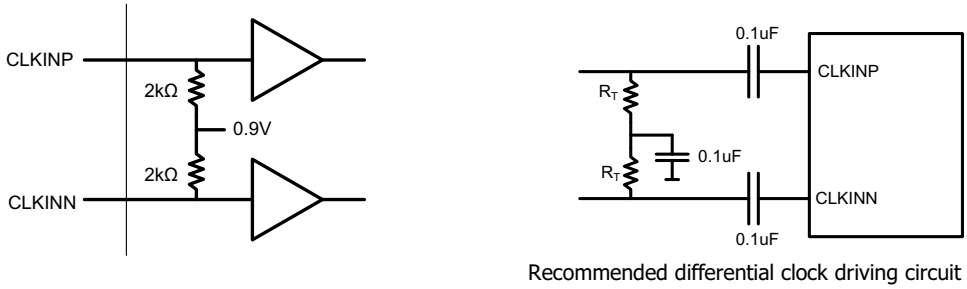


Figure 63. Recommended Differential Clock Driving Circuit

9.2.1 Design Requirements

The ADS5401 requires a fully differential analog input with a full-scale range not to exceed 1.0-V peak-to-peak, biased to a common-mode voltage of 1.9 V. In addition the input circuit must provide proper transmission line termination (or proper load resistors in an amplifier-based solution) so the input of the impedance of the ADC analog inputs should be considered as well.

The ADS5401 is capable of a typical SNR of 61.7 dBFS for input frequencies of about 100MHz. The amplifier and clocking solution will have a direct impact on performance in terms of SNR, so the amplifier and clocking solution should be selected such that the SNR performance of 61 dBFS is preserved.

9.2.2 Detailed Design Procedure

The ADS5401 has a max sample rate of 800 MHz and an input bandwidth of approximately 1200 MHz, but we will consider an application involving the first or second Nyquist zones, so we will limit the frequency bandwidth here to be under 375 MHz.

9.2.2.1 Clocking Source for ADC5401

The signal to noise ratio of the ADC is limited by three different factors: the quantization noise is typically not noticeable in pipeline converters and is 72 dB for a 12-bit ADC. The thermal noise limits the SNR at low input frequencies while the clock jitter sets the SNR for higher input frequencies.

Typical Application (continued)

$$SNR_{ADC}[dBc] = -20 \times \log \sqrt{\left(10 - \frac{SNR_{Quantization\_Noise}}{20}\right)^2 + \left(10 - \frac{SNR_{ThermalNoise}}{20}\right)^2 + \left(10 - \frac{SNR_{Jitter}}{20}\right)^2} \quad (1)$$

The SNR limitation due to sample clock jitter can be calculated as following:

$$SNR_{Jitter}[dBc] = -20 \times \log(2\pi \times f_{IN} \times t_{Jitter}) \quad (2)$$

The total clock jitter (TJitter) has three components – the internal aperture jitter (100fs for ADS5401) which is set by the noise of the clock input buffer, the external clock jitter and the jitter from the analog input signal. It can be calculated as following:

$$T_{Jitter} = \sqrt{(T_{Jitter,Ext.Clock\_Input})^2 + (T_{Aperture\_ADC})^2} \quad (3)$$

External clock jitter can be minimized by using high quality clock sources and jitter cleaners as well as bandpass filters at the clock input while a faster clock slew rate improves the ADC aperture jitter.

The ADS5401 has a thermal noise of 61.7 dBFS and internal aperture jitter of 100 fs. The SNR depending on amount of external jitter for different input frequencies is shown in Figure 64.

For the clock input, Figure 64 shows the SNR of the device above 100 MHz begins to degrade with external clock jitter of greater than 100 fs rms, so TI recommends the clock source be limited to approximately 100 fS of rms jitter.

9.2.2.2 Amplifier Selection

The amplifier should be selected to preserve the systems SNR performance of (61 dBFS). The SNR of the system can be calculated from Equation 4.

$$SNR_{System} = -20 \times \log \sqrt{\left(10^{\frac{-SNR_{ADC}}{20}}\right)^2 + \left(10^{\frac{-SNR_{AMP+Filter}}{20}}\right)^2} \quad (4)$$

The signal-to-noise ratio (SNR) of the amplifier and filter can be calculated from the amplitude of the signal and the bandwidth of the filter. The noise from the amplifier is band-limited by the filter with the equivalent brick-wall filter bandwidth. The amplifier and filter noise can be calculated using Equation 5.

$$SNR_{AMP+Filter} = 10 \times \log\left(\frac{V_O^2}{E_{FILTEROUT}^2}\right) = 20 \times \log\left(\frac{V_O}{E_{FILTEROUT}}\right)$$

Where

- $E_{FILTEROUT} = E_{NAMPOUT} \times \sqrt{ENB}$
- $E_{NAMPOUT}$ = the output noise density of the LMH3401 (3.4 nV/√Hz)
- ENB = the brick-wall equivalent noise bandwidth of the filter
- V_O = the amplifier output signal (5)

In this design we are using a 3rd order lowpass filter with 375MHz bandwidth, which gives brick-wall equivalent noise bandwidth of 431.25 MHz. Using the output noise density of LMH3401 and brick-wall equivalent bandwidth of the filter, EFILTEROUT can be calculated, equal to be 70.6 µVRMS. Substituting the values of EFILTEROUT and VO in Equation 4, SNRAMP+Filter equals 73.45 dBFS which is within our design requirements

Typical Application (continued)

9.2.3 Application Curve

Figure 64 shows the SNR vs input frequency and external clock signal; it can be used to estimate how much jitter on the clock signal is acceptable at a given input frequency to obtained specific SNR performance from the ADC.

Table 5. System SNR Based on ADC and Amplifier's SNR Calculations

SNR_{SYSTEM}	SNR_{ADC}	$SNR_{AMP + FILTER}$
57.7 dBFS	61.7 dBFS	60 dBFS
60.0 dBFS	61.7 dBFS	65 dBFS
61.1 dBFS	61.7 dBFS	70 dBFS
61.5 dBFS	61.7 dBFS	75 dBFS
61.6 dBFS	61.7 dBFS	80 dBFS

As seen in Table 5, to meet the design requirements and to have system SNR of 61 dBFS, the SNRAmp + Filter should be greater than 70 dB. Table 5 can be used to design the amplifier and filter stage of the ADC. The SNR of amplifier and filter should be greater than 70 dB to get the 61dBFS SNR for the system.

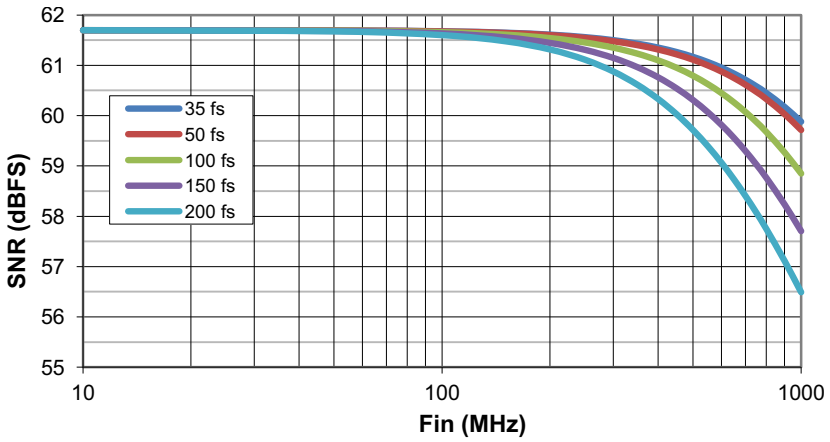


Figure 64. SNR vs Input Frequency and External Clock Jitter

10 Power Supply Recommendations

The device requires a 1.8-V nominal supply for AVDDC, AVDD18, IOVDD, DVDDLVDS, and DVDD. The device also requires a 3.3-V supply for AVDD33. There are no specific sequence power-supply requirements during device power-up. AVDD, DVDD, IOVDD, DVDDLVDS, AVDD18 and AVDD33 can power up in any order.

11 Layout

11.1 Layout Guidelines

The Device EVM layout can be used as a reference layout to obtain the best performance. A layout diagram of the EVM top layer is provided in Figure 65. Some important points to remember during laying out the board are:

- Analog input is located on opposite sides of the device pinout to ensure minimum crosstalk on the package level. To minimize crosstalk on-board, the analog input should exit the pinout in opposite directions, as shown in the reference layout of Figure 65 as much as possible.
- Digital outputs should be kept away from the analog inputs. When these digital outputs exit the pinout, the digital output traces should not be kept parallel to the analog input traces because this configuration may result in coupling from digital outputs to analog inputs and degrade performance.
- At each power-supply pin, a 0.1-µF decoupling capacitor should be kept close to the device. A separate decoupling capacitor group consisting of a parallel combination of 10-µF, 1-µF, and 0.1-µF capacitors can be kept close to the supply source.
- In the device pinout, the sampling clock is located on a side perpendicular to the analog inputs in order to minimize coupling between them. This configuration is also maintained on the reference layout of Figure 66 as much as possible.

11.2 Layout Example

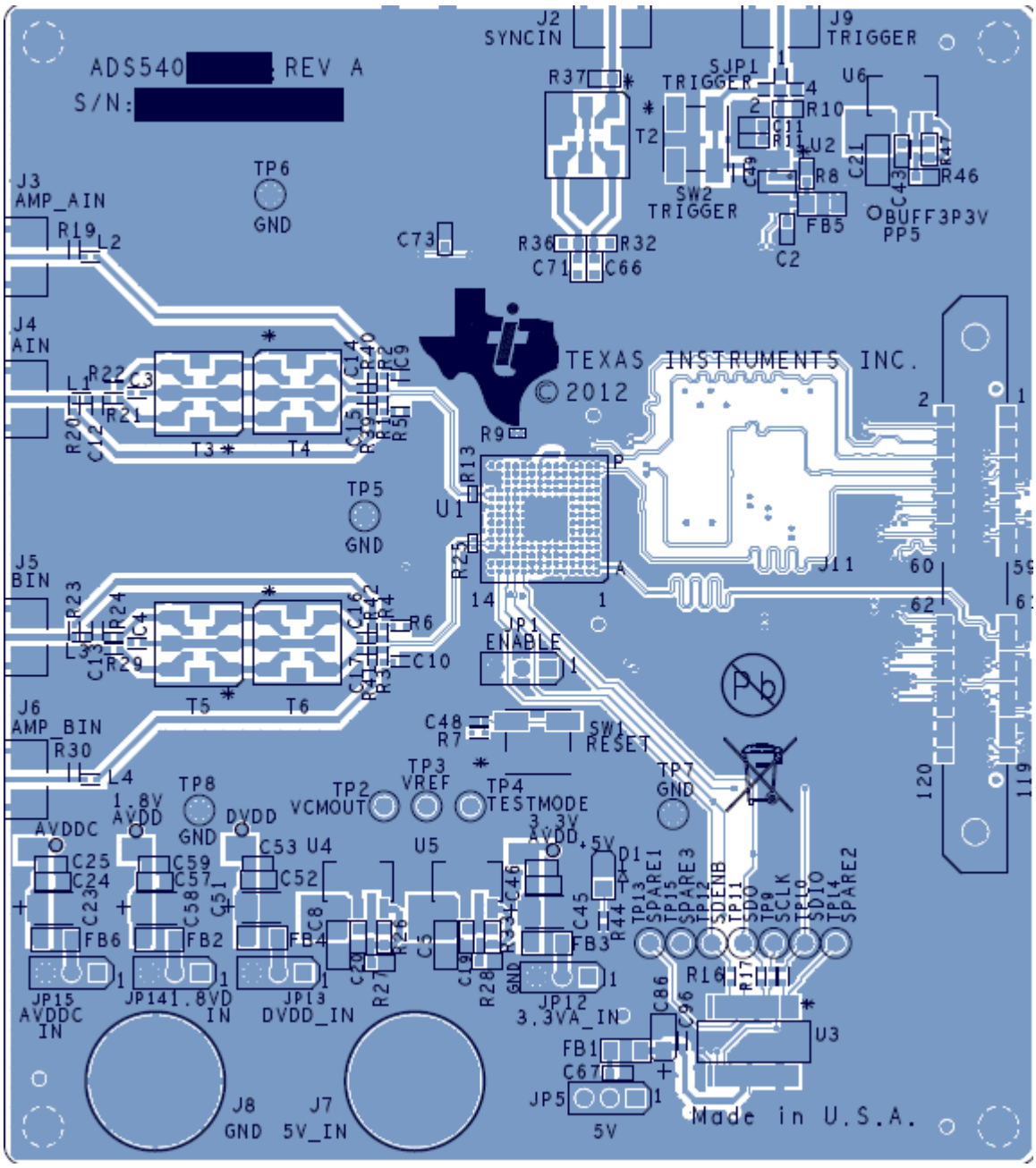


Figure 65. Top Layer

Layout Example (continued)

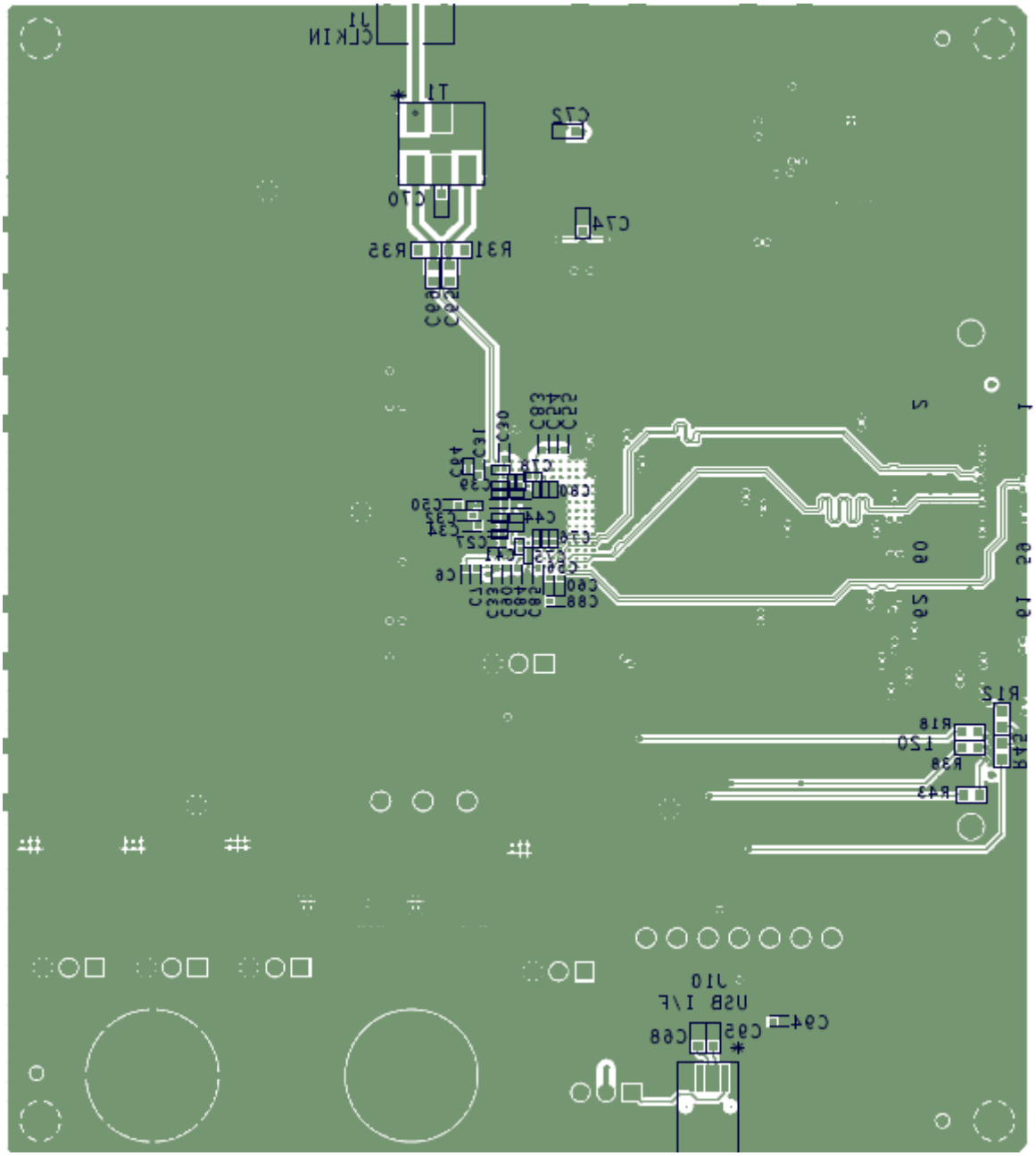


Figure 66. Bottom Layer

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS5401IZAY	ACTIVE	NFBGA	ZAY	196	160	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85	ADS5401I	Samples
ADS5401IZAYR	ACTIVE	NFBGA	ZAY	196	1000	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85	ADS5401I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

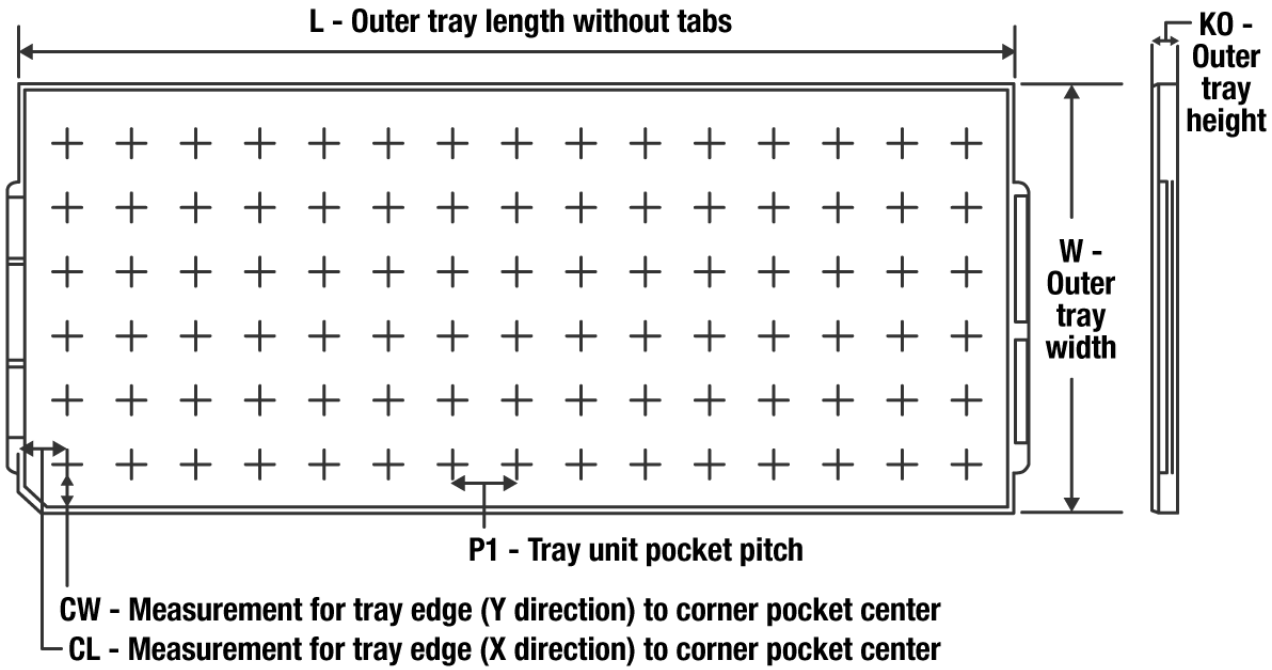
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

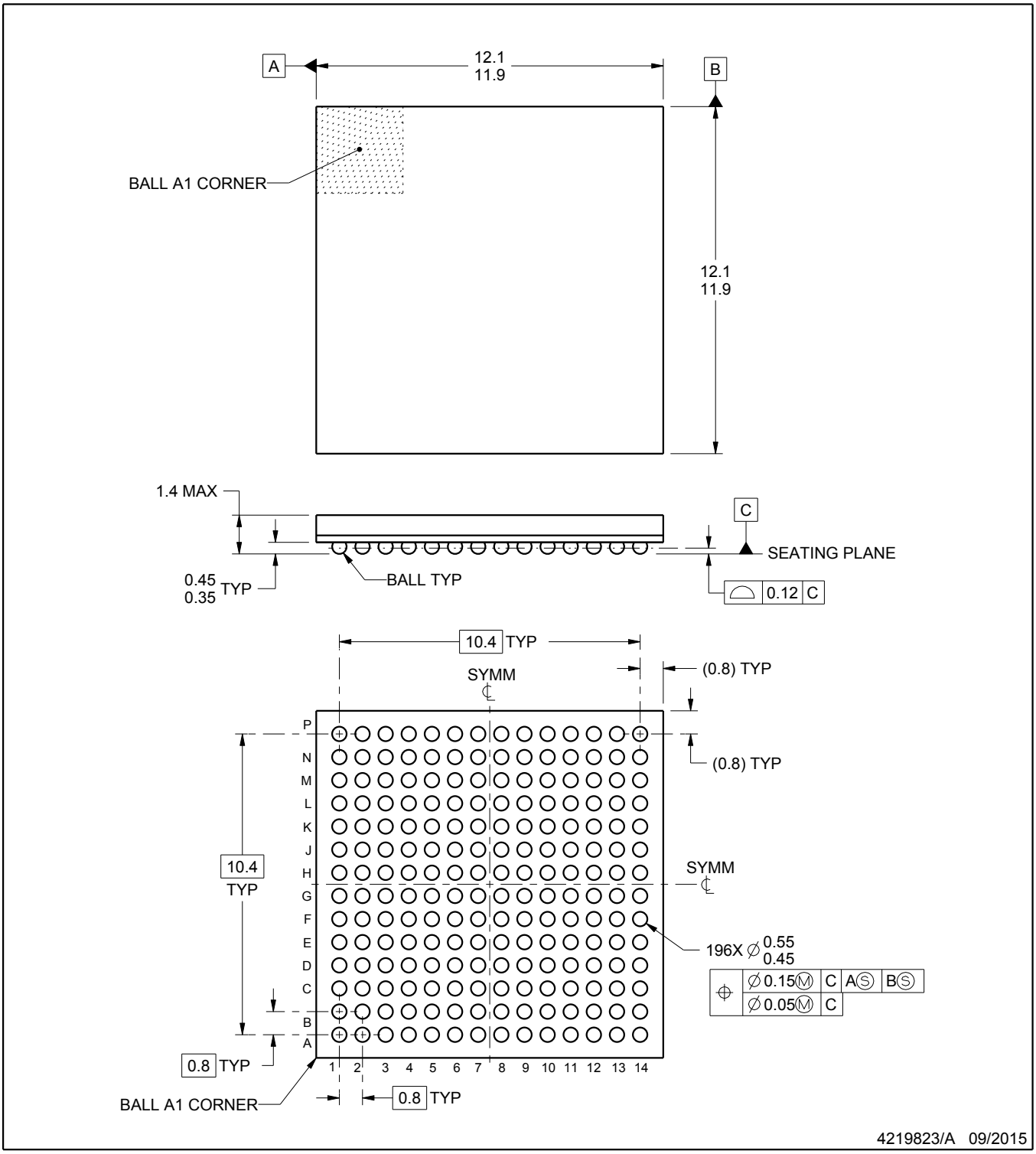
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
ADS5401IZAY	ZAY	NFBGA	196	160	8 x 20	150	315	135.9	7620	15.4	11.2	19.65

PACKAGE OUTLINE

ZAY0196A

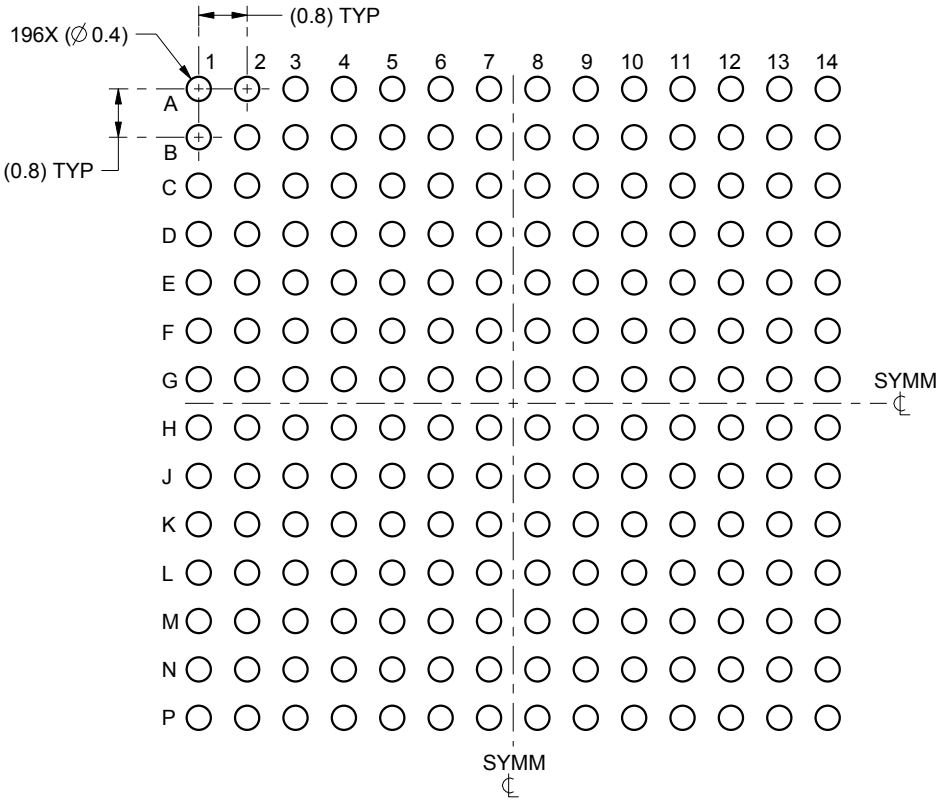
NFBGA - 1.4 mm max height

PLASTIC BALL GRID ARRAY

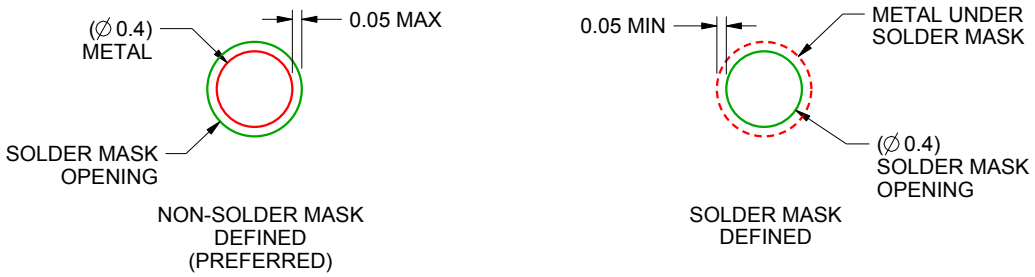


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS
NOT TO SCALE

4219823/A 09/2015

NOTES: (continued)

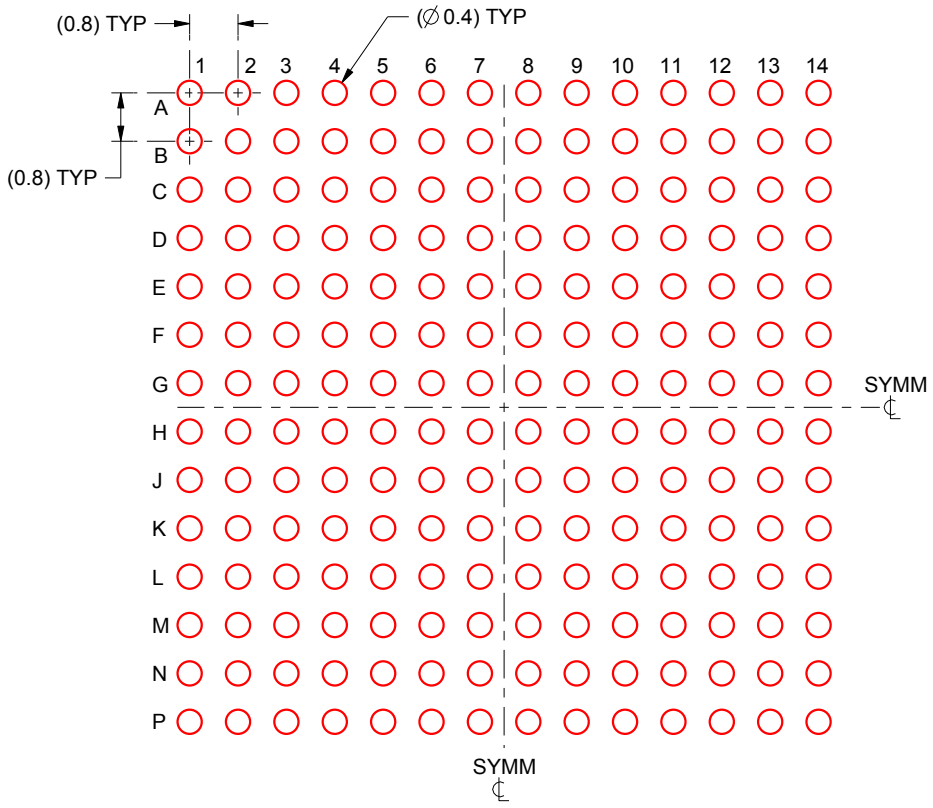
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).

EXAMPLE STENCIL DESIGN

ZAY0196A

NFBGA - 1.4 mm max height

PLASTIC BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:8X

4219823/A 09/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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