# LP3855-ADJ 1.5A Fast Response Ultra Low Dropout Linear Regulators

**Check for Samples: LP3855-ADJ**

## FEATURES

- **Ultra Low Dropout Voltage**
- **Stable with Selected Ceramic Capacitors**
- **Low Ground Pin Current**
- **Load Regulation of 0.06%**
- **10nA Quiescent Current in Shutdown Mode**
- **Specified Output Current of 1.5A DC**
- **Available in DDPAK/TO-263, TO-220 and SOT-223 Packages**
- **Overtemperature/Overcurrent Protection**
- **−40°C to +125°C Junction Temperature Range**

## APPLICATIONS

- **Microprocessor Power Supplies**
- **GTL, GTL+, BTL, and SSTL Bus Terminators**
- **Power Supplies for DSPs**
- **SCSI Terminator**
- **Post Regulators**
- **High efficiency linear regulators**
- **Battery chargers**
- **Other battery powered applications**

## DESCRIPTION

The LP3855-ADJ fast ultra low-dropout linear regulators operate from a +2.5V to +7.0V input supply. These ultra low dropout linear regulators respond very quickly to step changes in load, which makes them suitable for low voltage microprocessor applications. The LP3855-ADJ is developed on a CMOS process which allows low quiescent current operation independent of output load current. This CMOS process also allows the LP3855-ADJ to operate under extremely low dropout conditions.

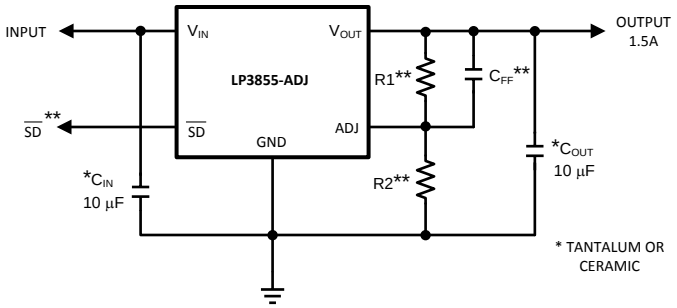
**Dropout Voltage:** Ultra low dropout voltage; typically 24mV at 150mA load current and 240mV at 1.5A load current.

**Ground Pin Current:** Typically 4mA at 1.5A load current.

**Shutdown Mode:** Typically 10nA quiescent current when the shutdown pin is pulled low.

**Adjustable Output Voltage:** The output voltage may be programmed via two external resistors.

## TYPICAL APPLICATION CIRCUIT




$$V_{OUT} = 1.216 \times \left(1 + \frac{R1}{R2}\right)$$

**See Application Hints.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## CONNECTION DIAGRAM

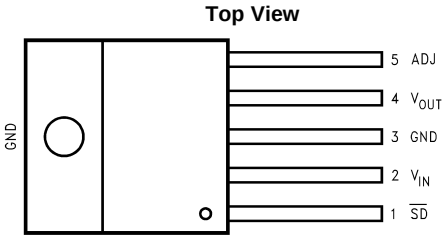


**Figure 1. TO-220-5 Package**
**Bent, Staggered Leads**
**See Package Number NDH0005D**

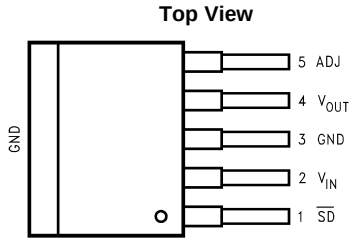


**Figure 2. DDPAK/TO-263-5 Package**
**See Package Number KTT0005B**

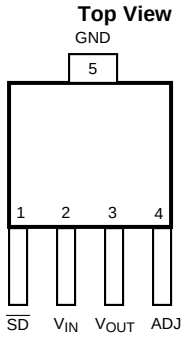


**Figure 3. SOT-223-5 Package**
**See Package Number NDC0005A**

**Table 1. PIN DESCRIPTIONS FOR TO-220-5 and DDPAK/TO-263-5 Packages**

| Pin # | LP3855-ADJ | |
|---|---|---|
| | Name | Function |
| 1 | $\overline{SD}$ | Shutdown |
| 2 | $V_{IN}$ | Input Supply |
| 3 | GND | Ground |
| 4 | $V_{OUT}$ | Output Voltage |
| 5 | ADJ | Set Output Voltage |

**Table 2. PIN DESCRIPTIONS for SOT-223-5 Package**

| Pin # | LP3855-ADJ | |
|---|---|---|
| | Name | Function |
| 1 | $\overline{SD}$ | Shutdown |
| 2 | $V_{IN}$ | Input Supply |
| 3 | $V_{OUT}$ | Output Voltage |
| 4 | ADJ | Set Output Voltage |
| 5 | GND | Ground |


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## BLOCK DIAGRAM

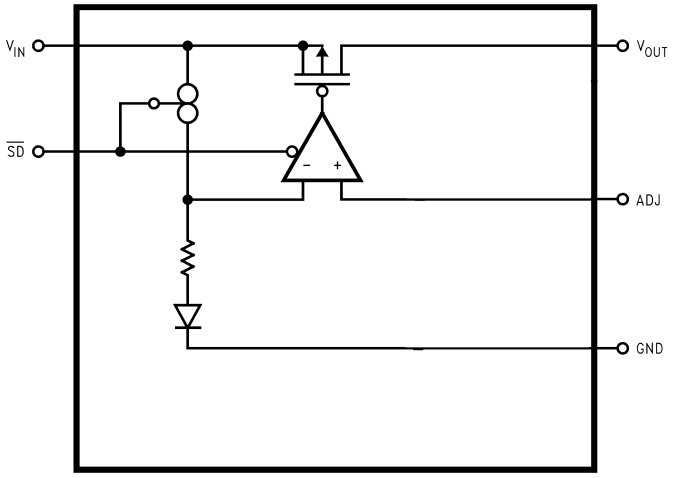


**Figure 4. LP3855-ADJ**

## ABSOLUTE MAXIMUM RATINGS (1)

**If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 5 sec.) | 260°C |
| ESD Rating (2) | 2 kV |
| Power Dissipation (3) | Internally Limited |
| Input Supply Voltage (Survival) | −0.3V to +7.5V |
| Shutdown Input Voltage (Survival) | −0.3V to 7.5V |
| Output Voltage (Survival), (4), (5) | −0.3V to +6.0V |
| $I_{OUT}$ (Survival) | Short Circuit Protected |

(1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions for which the device is intended to be functional, but does **not** ensure specific performance limits. For specifications and test conditions, see Electrical Characteristics. The specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.
(3) At elevated temperatures, devices must be derated based on package thermal resistance. The devices in TO-220 package must be derated at $\theta_{jA}$ = 50°C/W (with 0.5in$^2$, 1oz. copper area), junction-to-ambient (with no heat sink). The devices in the DDPAK/TO-263 surface-mount package must be derated at $\theta_{jA}$ = 60°C/W (with 0.5in$^2$, 1oz. copper area), junction-to-ambient. See Application Hints.
(4) If used in a dual-supply system where the regulator load is returned to a negative supply, the output must be diode-clamped to ground.
(5) The output PMOS structure contains a diode between the $V_{IN}$ and $V_{OUT}$ terminals. This diode is normally reverse biased. This diode will get forward biased if the voltage at the output terminal is forced to be higher than the voltage at the input terminal. This diode can typically withstand 200mA of DC current and 1Amp of peak current.

## RECOMMENDED OPERATING CONDITIONS

| | |
|---|---|
| Input Supply Voltage (Operating), (1) | 2.5V to 7.0V |
| Shutdown Input Voltage (Operating) | −0.3V to 7.0V |
| Maximum Operating Current (DC) | 1.5A |
| Operating Junction Temp. Range | −40°C to +125°C |

(1) The minimum operating value for $V_{IN}$ is equal to either [$V_{OUT(NOM)}$ + $V_{DROPOUT}$] or 2.5V, whichever is greater.

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## ELECTRICAL CHARACTERISTICS — LP3855-ADJ

Limits in standard typeface are for $T_J$ = 25°C, and limits in **boldface type** apply over the **full operating temperature range**. Unless otherwise specified: $V_{IN} = V_{O(NOM)}$ + 1V, $I_L$ = 10 mA, $C_{OUT}$ = 10µF, $V_{SD}$ = 2V.

| Symbol | Parameter | Conditions | Typ (1) | LP3855-ADJ (2) | | Units |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| $V_{ADJ}$ | Adjust Pin Voltage | $V_{OUT}$ +1V ≤ $V_{IN}$≤ 7V<br>10 mA ≤ $I_L$ ≤ 1.5A | 1.216 | 1.198<br>**1.180** | 1.234<br>**1.253** | V |
| $I_{ADJ}$ | Adjust Pin Input Current | $V_{OUT}$ +1V ≤ $V_{IN}$≤ 7V<br>10 mA ≤ $I_L$ ≤ 1.5A | 10 | | **100** | nA |
| $\Delta V_{OL}$ | Output Voltage Line Regulation (3) | $V_{OUT}$ +1V ≤ $V_{IN}$ ≤ 7.0V | 0.02<br>**0.06** | | | % |
| $\Delta V_O / \Delta I_{OUT}$ | Output Voltage Load Regulation (3) | 10 mA ≤ $I_L$ ≤ 1.5A | 0.06<br>**0.12** | | | % |
| $V_{IN}$ - $V_{OUT}$ | Dropout Voltage, DDPAK/TO-263 and TO-220 (4) | $I_L$ = 150 mA | 24 | | 35<br>**45** | mV |
| | | $I_L$ = 1.5A | 240 | | 310<br>**420** | |
| | Dropout Voltage, SOT 223 (4) (5) | $I_L$ = 150 mA | 26 | | 35<br>**45** | |
| | | $I_L$ = 1.5A | 260 | | 320<br>**435** | |
| $I_{GND}$ | Ground Pin Current In Normal Operation Mode | $I_L$ = 150 mA | 3 | | 9<br>**10** | mA |
| | | $I_L$ = 1.5A | 3 | | 9<br>**10** | |
| $I_{GND}$ | Ground Pin Current In Shutdown Mode | $V_{SD}$ ≤ 0.3V | 0.01 | | 10 | µA |
| | | -40°C ≤ $T_J$ ≤ 85°C | | | **50** | |
| $I_{O(PK)}$ | Peak Output Current | $V_O$ ≥ $V_{O(NOM)}$ - 4% | 1.8 | | | A |
| **Short Circuit Protection** | | | | | | |
| $I_{SC}$ | Short Circuit Current | | 3.2 | | | A |
| **Shutdown Input** | | | | | | |
| $V_{SDT}$ | Shutdown Threshold | $V_{SDT}$ Rising from 0.3V until Output = ON | 1.3 | **2** | | V |
| | | $V_{SDT}$ Falling from 2.0V until Output = OFF | 1.3 | | **0.3** | |
| $T_{dOFF}$ | Turn-off delay | $I_L$ = 1.5A | 20 | | | µs |
| $T_{dON}$ | Turn-on delay | $I_L$ = 1.5A | 25 | | | µs |
| $I_{SD}$ | $\overline{SD}$ Input Current | $V_{SD}$ = $V_{IN}$ | 1 | | | nA |
| **AC Parameters** | | | | | | |
| PSRR | Ripple Rejection | $V_{IN}$ = $V_{OUT}$ + 1V, $C_{OUT}$ = 10uF<br>$V_{OUT}$ = 3.3V, f = 120Hz | 73 | | | dB |
| | | $V_{IN}$ = $V_{OUT}$ + 0.5V, $C_{OUT}$ = 10uF<br>$V_{OUT}$ = 3.3V, f = 120Hz | 57 | | | |
| $\rho_{n(l/f)}$ | Output Noise Density | f = 120Hz | 0.8 | | | µV |
| $e_n$ | Output Noise Voltage | BW = 10Hz – 100kHz, $V_{OUT}$ = 2.5V | 150 | | | µV (rms) |
| | | BW = 300Hz – 300kHz, $V_{OUT}$ = 2.5V | 100 | | | |

(1) Typical numbers are at 25°C and represent the most likely parametric norm.
(2) Limits are specified by testing, design, or statistical correlation.
(3) Output voltage line regulation is defined as the change in output voltage from the nominal value due to change in the input line voltage. Output voltage load regulation is defined as the change in output voltage from the nominal value due to change in load current.
(4) Dropout voltage is defined as the minimum input to output differential voltage at which the output drops 2% below the nominal value. Dropout voltage specification applies only to output voltages of 2.5V and above. For output voltages below 2.5V, the drop-out voltage is nothing but the input to output differential, since the minimum input voltage is 2.5V.
(5) The SOT-223 package devices have slightly higher dropout due to increased bond wire resistance.


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## TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified: $T_J$ = 25°C, $C_{OUT}$ = 10µF, $C_{IN}$ = 10µF, S/D pin is tied to $V_{IN}$, $V_{OUT}$ = 2.5V, $V_{IN}$ = $V_{O(NOM)}$ + 1V, $I_L$ = 10 mA.

**Dropout Voltage vs Output Load Current**

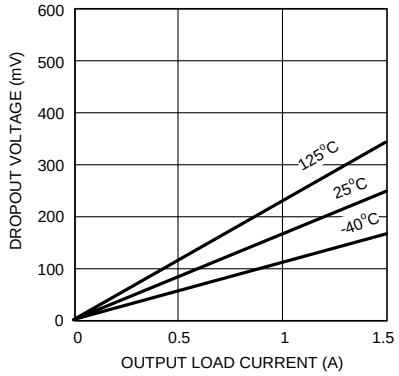


**Figure .**

**Ground Current vs Output Voltage**
**$I_L$ = 1.5A**

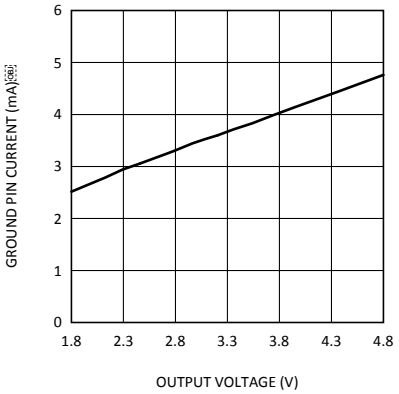


**Figure 5.**

**Shutdown $I_Q$ vs Junction Temperature**

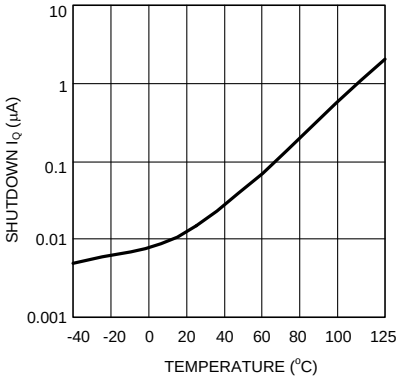


**Figure 6.**

**DC Load Reg. vs Junction Temperature**

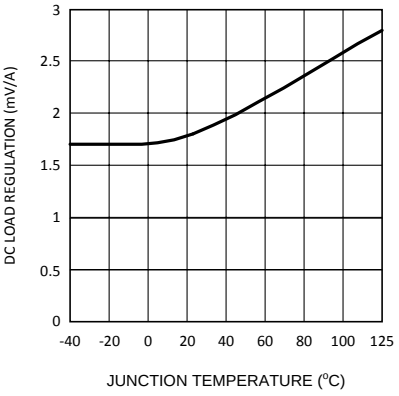


**Figure 7.**

**DC Line Regulation vs Temperature**

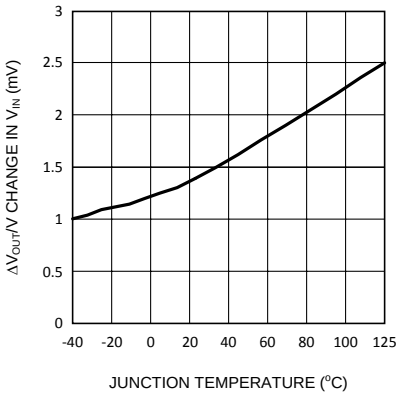


**Figure 8.**

**$V_{IN}$ vs $V_{OUT}$ Over Temperature**

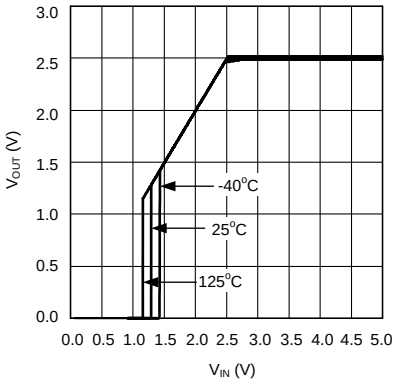


**Figure 9.**

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## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: $T_J$ = 25°C, $C_{OUT}$ = 10µF, $C_{IN}$ = 10µF, S/D pin is tied to $V_{IN}$, $V_{OUT}$ = 2.5V, $V_{IN}$ = $V_{O(NOM)}$ + 1V, $I_L$ = 10 mA.

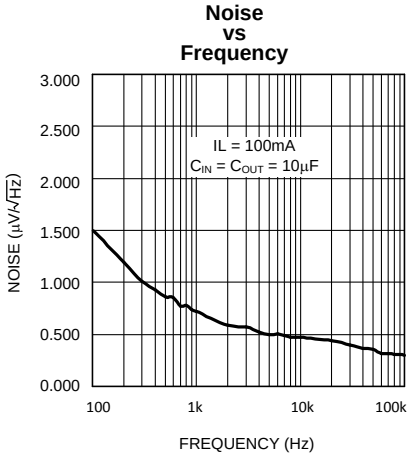


**Figure 10.**

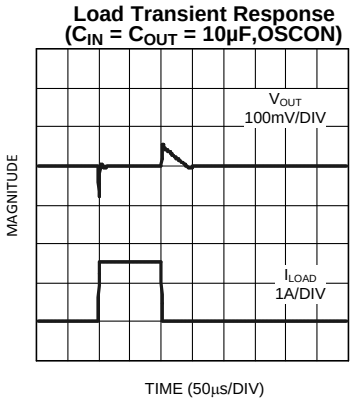


**Figure 11.**

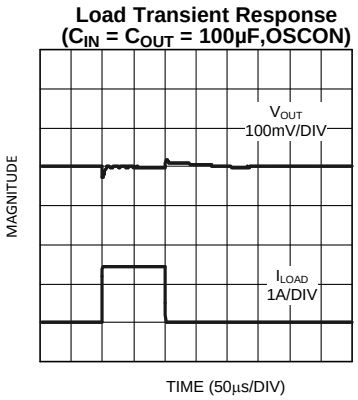


**Figure 12.**

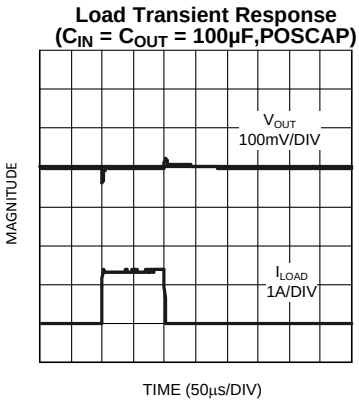


**Figure 13.**

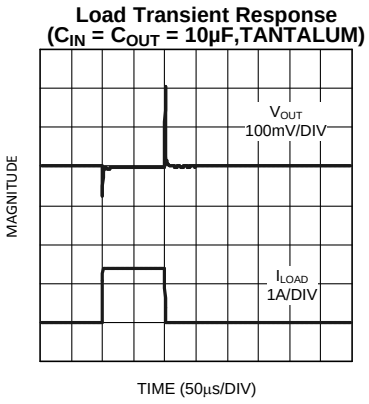


**Figure 14.**

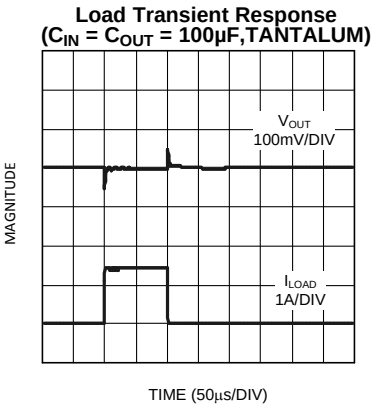


**Figure 15.**


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## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: $T_J$ = 25°C, $C_{OUT}$ = 10µF, $C_{IN}$ = 10µF, S/D pin is tied to $V_{IN}$, $V_{OUT}$ = 2.5V, $V_{IN}$ = $V_{O(NOM)}$ + 1V, $I_L$ = 10 mA.

**Load Transient Response**
**$C_{IN}$ = 2 x 10µF CERAMIC**
**$C_{OUT}$ = 2 x 10µF CERAMIC**

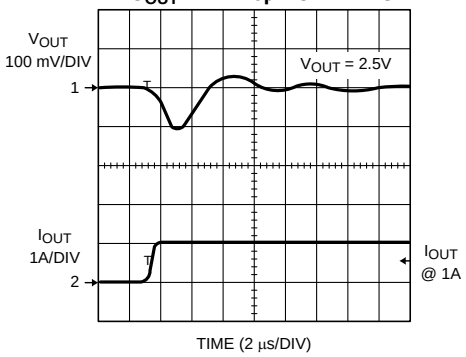


**Figure 16.**

**Load Transient Response**
**$C_{IN}$ = 2 x 10µF CERAMIC**
**$C_{OUT}$ = 2 x 10µF CERAMIC**

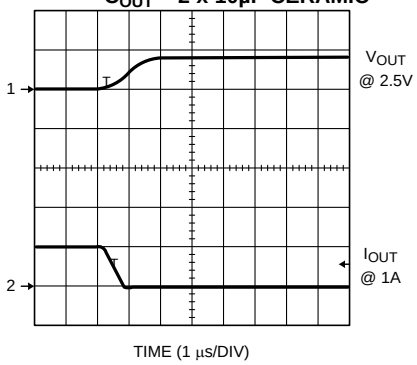


**Figure 17.**

## Application Hints

### SETTING THE OUTPUT VOLTAGE

The output voltage is set using the resistors R1 and R2 (see Typical Application Circuit). The output is also dependent on the reference voltage (typically 1.216V) which is measured at the ADJ pin. The output voltage is given by the equation:

$$V_{OUT} = V_{ADJ} \times ( 1 + R1 / R2) \quad (1)$$

This equation does not include errors due to the bias current flowing in the ADJ pin which is typically about 10 nA. This error term is negligible for most applications. If R1 is > 100kΩ , a small error may be introduced by the ADJ bias current.

The tolerance of the external resistors used contributes a significant error to the output voltage accuracy, with 1% resistors typically adding a total error of approximately 1.4% to the output voltage (this error is in addition to the tolerance of the reference voltage at $V_{ADJ}$).

### TURN-ON CHARACTERISTICS FOR OUTPUT VOLTAGES PROGRAMMED TO 2.0V OR BELOW

As Vin increases during start-up, the regulator output will track the input until Vin reaches the minimum operating voltage (typically about 2.2V). For output voltages programmed to 2.0V or below, the regulator output may momentarily exceed its programmed output voltage during start up. Outputs programmed to voltages above 2.0V are not affected by this behavior.

### EXTERNAL CAPACITORS

Like any low-dropout regulator, external capacitors are required to assure stability. these capacitors must be correctly selected for proper performance.

**INPUT CAPACITOR:** An input capacitor of at least 10µF is required. Ceramic or Tantalum may be used, and capacitance may be increased without limit

**OUTPUT CAPACITOR:** An output capacitor is required for loop stability. It must be located less than 1 cm from the device and connected directly to the output and ground pins using traces which have no other currents flowing through them (see PCB Layout section).

The minimum amount of output capacitance that can be used for stable operation is 10µF. For general usage across all load currents and operating conditions, the part was characterized using a 10µF Tantalum input capacitor. The minimum and maximum stable ESR range for the output capacitor was then measured which kept the device stable, assuming any output capacitor whose value is greater than 10µF (see Figure 18 below).

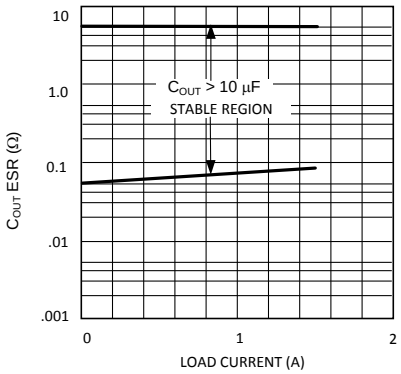


**Figure 18. ESR Curve for $C_{OUT}$ (with 10µF Tantalum Input Capacitor)**

It should be noted that it is possible to operate the part with an output capacitor whose ESR is below these limits, assuming that sufficient ceramic input capacitance is provided. This will allow stable operation using ceramic output capacitors (see next section).


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## OPERATION WITH CERAMIC OUTPUT CAPACITORS

LP385X voltage regulators can operate with ceramic output capacitors if the values of the input and output capacitors are selected appropriately. The total ceramic output capacitance must be equal to or less than a specified maximum value in order for the regulator to remain stable over all operating conditions. This maximum amount of ceramic output capacitance is dependent upon the amount of ceramic input capacitance used as well as the load current of the application. This relationship is shown in Figure 19, which graphs the maximum stable value of ceramic output capacitance as a function of ceramic input capacitance for load currents of 1.5A.

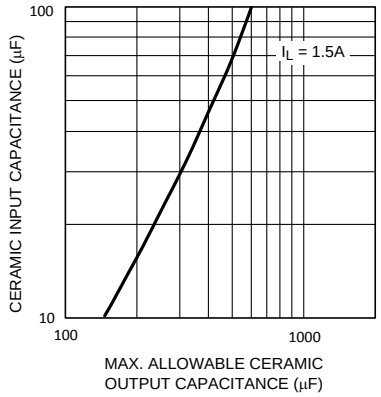


**Figure 19. Maximum Ceramic Output Capacitance vs Ceramic Input Capacitance**

If the maximum load current is 1.5A and a 10µF ceramic input capacitor is used, the regulator will be stable with ceramic output capacitor values from 10µF up to about 150µF. When calculating the total ceramic output capacitance present in an application, it is necessary to include any ceramic bypass capacitors connected to the regulator output.

### $C_{FF}$ (Feed Forward Capacitor)

The capacitor $C_{FF}$ is required to add phase lead and help improve loop compensation. The correct amount of capacitance depends on the value selected for R1 (see Typical Application Circuit). The capacitor should be selected such that the zero frequency as given by the equation shown below is approximately 45 kHz:

$$Fz = 45{,}000 = 1 / ( 2 \times \pi \times R1 \times C_{FF} ) \quad (2)$$

A good quality ceramic with X5R or X7R dielectric should be used for this capacitor.

## SELECTING A CAPACITOR

It is important to note that capacitance tolerance and variation with temperature must be taken into consideration when selecting a capacitor so that the minimum required amount of capacitance is provided over the full operating temperature range. In general, a good Tantalum capacitor will show very little capacitance variation with temperature, but a ceramic may not be as good (depending on dielectric type). Aluminum electrolytics also typically have large temperature variation of capacitance value.

Equally important to consider is a capacitor's ESR change with temperature: this is not an issue with ceramics, as their ESR is extremely low. However, it is very important in Tantalum and aluminum electrolytic capacitors. Both show increasing ESR at colder temperatures, but the increase in aluminum electrolytic capacitors is so severe they may not be feasible for some applications (see Capacitor Characteristics Section).

## CAPACITOR CHARACTERISTICS

**CERAMIC:** For values of capacitance in the 10 to 100 µF range, ceramics are usually larger and more costly than tantalums but give superior AC performance for bypassing high frequency noise because of very low ESR (typically less than 10 mΩ). However, some dielectric types do not have good capacitance characteristics as a function of voltage and temperature.

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Z5U and Y5V dielectric ceramics have capacitance that drops severely with applied voltage. A typical Z5U or Y5V capacitor can lose 60% of its rated capacitance with half of the rated voltage applied to it. The Z5U and Y5V also exhibit a severe temperature effect, losing more than 50% of nominal capacitance at high and low limits of the temperature range.

X7R and X5R dielectric ceramic capacitors are strongly recommended if ceramics are used, as they typically maintain a capacitance range within ±20% of nominal over full operating ratings of temperature and voltage. Of course, they are typically larger and more costly than Z5U/Y5U types for a given voltage and capacitance.

**TANTALUM:** Solid Tantalum capacitors are typically recommended for use on the output because their ESR is very close to the ideal value required for loop compensation.

Tantalums also have good temperature stability: a good quality Tantalum will typically show a capacitance value that varies less than 10-15% across the full temperature range of 125°C to −40°C. ESR will vary only about 2X going from the high to low temperature limits.

The increasing ESR at lower temperatures can cause oscillations when marginal quality capacitors are used (if the ESR of the capacitor is near the upper limit of the stability range at room temperature).

**ALUMINUM:** This capacitor type offers the most capacitance for the money. The disadvantages are that they are larger in physical size, not widely available in surface mount, and have poor AC performance (especially at higher frequencies) due to higher ESR and ESL.

Compared by size, the ESR of an aluminum electrolytic is higher than either Tantalum or ceramic, and it also varies greatly with temperature. A typical aluminum electrolytic can exhibit an ESR increase of as much as 50X when going from 25°C down to −40°C.

It should also be noted that many aluminum electrolytics only specify impedance at a frequency of 120 Hz, which indicates they have poor high frequency performance. Only aluminum electrolytics that have an impedance specified at a higher frequency (between 20 kHz and 100 kHz) should be used for the LP385X. Derating must be applied to the manufacturer's ESR specification, since it is typically only valid at room temperature.

Any applications using aluminum electrolytics should be thoroughly tested at the lowest ambient operating temperature where ESR is maximum.

## PCB LAYOUT

Good PC layout practices must be used or instability can be induced because of ground loops and voltage drops. The input and output capacitors must be directly connected to the input, output, and ground pins of the LP385X using traces which do not have other currents flowing in them (Kelvin connect).

The best way to do this is to lay out $C_{IN}$ and $C_{OUT}$ near the device with short traces to the $V_{IN}$, $V_{OUT}$, and ground pins. The regulator ground pin should be connected to the external circuit ground so that the regulator and its capacitors have a "single point ground".

It should be noted that stability problems have been seen in applications where "vias" to an internal ground plane were used at the ground points of the IC and the input and output capacitors. This was caused by varying ground potentials at these nodes resulting from current flowing through the ground plane. Using a single point ground technique for the regulator and it's capacitors fixed the problem.

Since high current flows through the traces going into $V_{IN}$ and coming from $V_{OUT}$, Kelvin connect the capacitor leads to these pins so there is no voltage drop in series with the input and output capacitors.

## RFI/EMI SUSCEPTIBILITY

RFI (radio frequency interference) and EMI (electromagnetic interference) can degrade any integrated circuit's performance because of the small dimensions of the geometries inside the device. In applications where circuit sources are present which generate signals with significant high frequency energy content (> 1 MHz), care must be taken to ensure that this does not affect the IC regulator.

If RFI/EMI noise is present on the input side of the regulator (such as applications where the input source comes from the output of a switching regulator), good ceramic bypass capacitors must be used at the input pin of the IC.


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If a load is connected to the IC output which switches at high speed (such as a clock), the high-frequency current pulses required by the load must be supplied by the capacitors on the IC output. Since the bandwidth of the regulator loop is less than 100 kHz, the control circuitry cannot respond to load changes above that frequency. The means the effective output impedance of the IC at frequencies above 100 kHz is determined only by the output capacitor(s).

In applications where the load is switching at high speed, the output of the IC may need RF isolation from the load. It is recommended that some inductance be placed between the output capacitor and the load, and good RF bypass capacitors be placed directly across the load.

PCB layout is also critical in high noise environments, since RFI/EMI is easily radiated directly into PC traces. Noisy circuitry should be isolated from "clean" circuits where possible, and grounded through a separate path. At MHz frequencies, ground planes begin to look inductive and RFI/EMI can cause ground bounce across the ground plane.

In multi-layer PCB applications, care should be taken in layout so that noisy power and ground planes do not radiate directly into adjacent layers which carry analog power and ground.

### OUTPUT NOISE

Noise is specified in two ways-

**Spot Noise** or **Output noise density** is the RMS sum of all noise sources, measured at the regulator output, at a specific frequency (measured with a 1Hz bandwidth). This type of noise is usually plotted on a curve as a function of frequency.

**Total output Noise** or **Broad-band noise** is the RMS sum of spot noise over a specified bandwidth, usually several decades of frequencies.

Attention should be paid to the units of measurement. Spot noise is measured in units μV/√Hz or nV/√Hz and total output noise is measured in μV(rms).

The primary source of noise in low-dropout regulators is the internal reference. In CMOS regulators, noise has a low frequency component and a high frequency component, which depend strongly on the silicon area and quiescent current. Noise can be reduced in two ways: by increasing the transistor area or by increasing the current drawn by the internal reference. Increasing the area will decrease the chance of fitting the die into a smaller package. Increasing the current drawn by the internal reference increases the total supply current (ground pin current). Using an optimized trade-off of ground pin current and die size, LP3855-ADJ achieves low noise performance and low quiescent current operation.

The total output noise specification for LP3855-ADJ is presented in the Electrical Characteristics table. The Output noise density at different frequencies is represented by a curve under typical performance characteristics.

### SHORT-CIRCUIT PROTECTION

The LP3855-ADJ is short circuit protected and in the event of a peak over-current condition, the short-circuit control loop will rapidly drive the output PMOS pass element off. Once the power pass element shuts down, the control loop will rapidly cycle the output on and off until the average power dissipation causes the thermal shutdown circuit to respond to servo the on/off cycling to a lower frequency. Please refer to the section on thermal information for power dissipation calculations.

### SHUTDOWN OPERATION

A CMOS Logic low level signal at the shutdown ($\overline{SD}$) pin will turn-off the regulator. Pin $\overline{SD}$ must be actively terminated through a 10kΩ pull-up resistor for a proper operation. If this pin is driven from a source that actively pulls high and low (such as a CMOS rail to rail comparator), the pull-up resistor is not required. This pin must be tied to Vin if not used.

The Shutdown ($\overline{SD}$) pin threshold has no voltage hysteresis. If the Shutdown pin is actively driven, the voltage transition must rise and fall cleanly and promptly.

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## DROPOUT VOLTAGE

The dropout voltage of a regulator is defined as the minimum input-to-output differential required to stay within 2% of the nominal output voltage. For CMOS LDOs, the dropout voltage is the product of the load current and the Rds(on) of the internal MOSFET.

## REVERSE CURRENT PATH

The internal MOSFET in LP3855-ADJ has an inherent parasitic diode. During normal operation, the input voltage is higher than the output voltage and the parasitic diode is reverse biased. However, if the output is pulled above the input in an application, then current flows from the output to the input as the parasitic diode gets forward biased. The output can be pulled above the input as long as the current in the parasitic diode is limited to 200mA continuous and 1A peak.

## POWER DISSIPATION/HEATSINKING

The LP3855-ADJ can deliver a continuous current of 1.5A over the full operating temperature range. A heatsink may be required depending on the maximum power dissipation and maximum ambient temperature of the application. Under all possible conditions, the junction temperature must be within the range specified under operating conditions. The total power dissipation of the device is given by:

$$P_D = (V_{IN} - V_{OUT})I_{OUT} + (V_{IN})I_{GND} \quad (3)$$

where $I_{GND}$ is the operating ground current of the device (specified under Electrical Characteristics).

The maximum allowable temperature rise ($T_{Rmax}$) depends on the maximum ambient temperature ($T_{Amax}$) of the application, and the maximum allowable junction temperature ($T_{Jmax}$):

$$T_{Rmax} = T_{Jmax} - T_{Amax} \quad (4)$$

The maximum allowable value for junction to ambient Thermal Resistance, $\theta_{JA}$, can be calculated using the formula:

$$\theta_{JA} = T_{Rmax} / P_D \quad (5)$$

The LP3855-ADJ is available in TO-220 and DDPAK/TO-263 packages. The thermal resistance depends on amount of copper area or heat sink, and on air flow. If the maximum allowable value of $\theta_{JA}$ calculated above is ≥ 60 °C/W for TO-220 package and ≥ 60 °C/W for DDPAK/TO-263 package no heatsink is needed since the package can dissipate enough heat to satisfy these requirements. If the value for allowable $\theta_{JA}$ falls below these limits, a heat sink is required.

## HEATSINKING TO-220 PACKAGE

The thermal resistance of a TO220 package can be reduced by attaching it to a heat sink or a copper plane on a PC board. If a copper plane is to be used, the values of $\theta_{JA}$ will be same as shown in next section for TO263 package.

The heatsink to be used in the application should have a heatsink to ambient thermal resistance,

$$\theta_{HA} \leq \theta_{JA} - \theta_{CH} - \theta_{JC}. \quad (6)$$

In this equation, $\theta_{CH}$ is the thermal resistance from the case to the surface of the heat sink and $\theta_{JC}$ is the thermal resistance from the junction to the surface of the case. $\theta_{JC}$ is about 3°C/W for a TO-220 package. The value for $\theta_{CH}$ depends on method of attachment, insulator, etc. $\theta_{CH}$ varies between 1.5°C/W to 2.5°C/W. If the exact value is unknown, 2°C/W can be assumed.

## HEATSINKING DDPAK/TO-263 PACKAGE

The DDPAK/TO-263 package uses the copper plane on the PCB as a heatsink. The tab of these packages are soldered to the copper plane for heat sinking. Figure 20 shows a curve for the $\theta_{JA}$ of DDPAK/TO-263 package for different copper area sizes, using a typical PCB with 1 ounce copper and no solder mask over the copper area for heat sinking.


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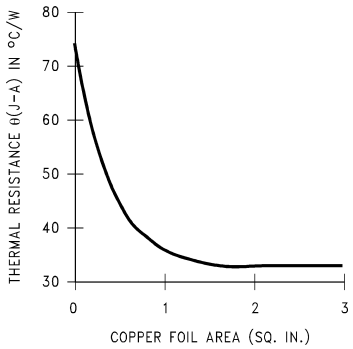


**Figure 20. $\theta_{JA}$ vs Copper (1 Ounce) Area for DDPAK/TO-263 Package**

As shown in the figure, increasing the copper area beyond 1 square inch produces very little improvement. The minimum value for $\theta_{JA}$ for the DDPAK/TO-263 package mounted to a PCB is 32°C/W.

Figure 21 shows the maximum allowable power dissipation for DDPAK/TO-263 packages for different ambient temperatures, assuming $\theta_{JA}$ is 35°C/W and the maximum junction temperature is 125°C.

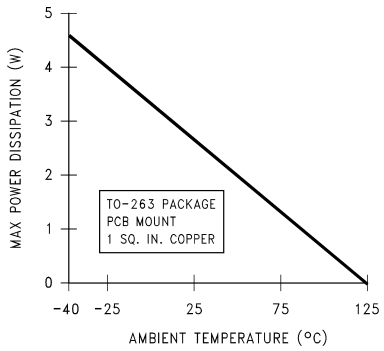


**Figure 21. Maximum Power Dissipation vs Ambient Temperature for DDPAK/TO-263 Package**

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## REVISION HISTORY

| Changes from Revision E (April 2013) to Revision F | Page |
|---|---|
| • Changed layout of National Data Sheet to TI format | 13 |


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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LP3855EMP-ADJ/NOPB | ACTIVE | SOT-223 | NDC | 5 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | LJ3B | Samples |
| LP3855EMPX-ADJ/NOPB | ACTIVE | SOT-223 | NDC | 5 | 2000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | LJ3B | Samples |
| LP3855ES-ADJ/NOPB | ACTIVE | DDPAK/ TO-263 | KTT | 5 | 45 | Pb-Free (RoHS Exempt) | CU SN | Level-3-245C-168 HR | -40 to 125 | LP3855ES -ADJ | Samples |
| LP3855ESX-ADJ/NOPB | ACTIVE | DDPAK/ TO-263 | KTT | 5 | 500 | Pb-Free (RoHS Exempt) | CU SN | Level-3-245C-168 HR | -40 to 125 | LP3855ES -ADJ | Samples |
| LP3855ET-ADJ/NOPB | ACTIVE | TO-220 | NDH | 5 | 45 | Green (RoHS & no Sb/Br) | CU SN | Level-1-NA-UNLIM | -40 to 125 | LP3855ET -ADJ | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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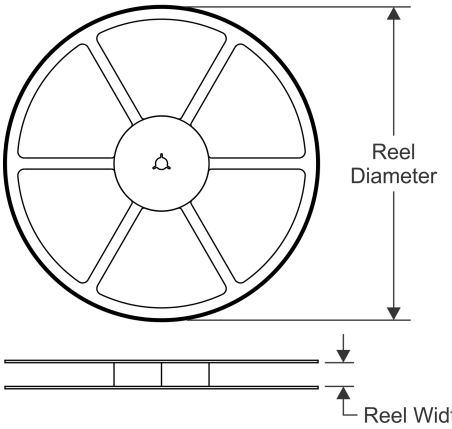
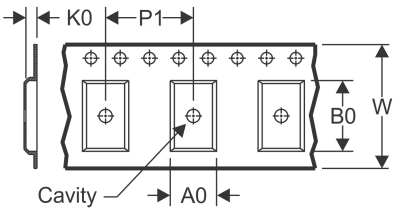
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

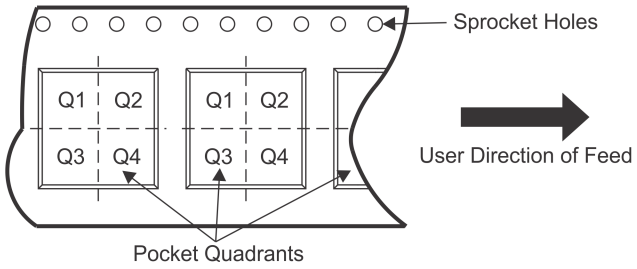



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

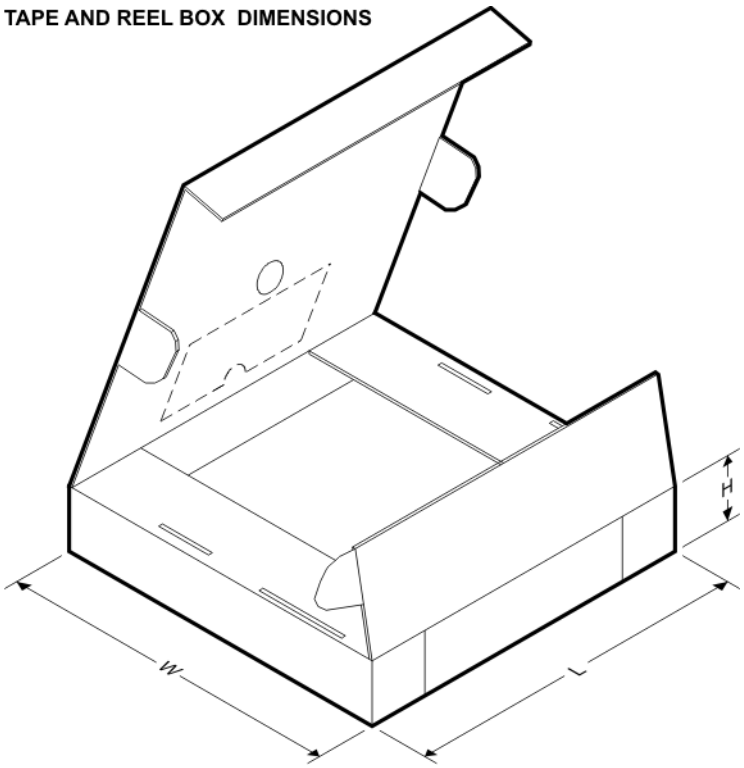
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LP3855EMP-ADJ/NOPB | SOT-223 | NDC | 5 | 1000 | 330.0 | 16.4 | 7.0 | 7.5 | 2.2 | 12.0 | 16.0 | Q3 |
| LP3855EMPX-ADJ/NOPB | SOT-223 | NDC | 5 | 2000 | 330.0 | 16.4 | 7.0 | 7.5 | 2.2 | 12.0 | 16.0 | Q3 |
| LP3855ESX-ADJ/NOPB | DDPAK/ TO-263 | KTT | 5 | 500 | 330.0 | 24.4 | 10.75 | 14.85 | 5.0 | 16.0 | 24.0 | Q2 |

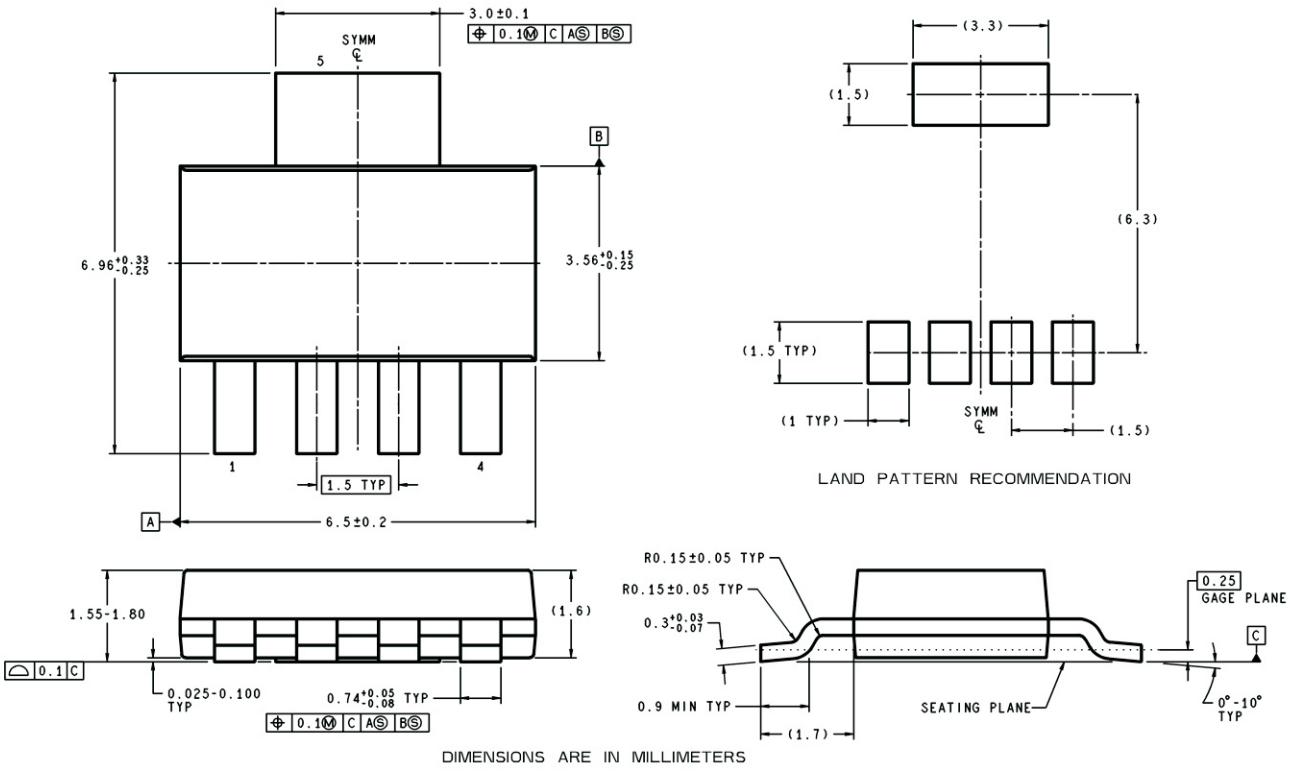
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LP3855EMP-ADJ/NOPB | SOT-223 | NDC | 5 | 1000 | 367.0 | 367.0 | 35.0 |
| LP3855EMPX-ADJ/NOPB | SOT-223 | NDC | 5 | 2000 | 367.0 | 367.0 | 35.0 |
| LP3855ESX-ADJ/NOPB | DDPAK/TO-263 | KTT | 5 | 500 | 367.0 | 367.0 | 45.0 |

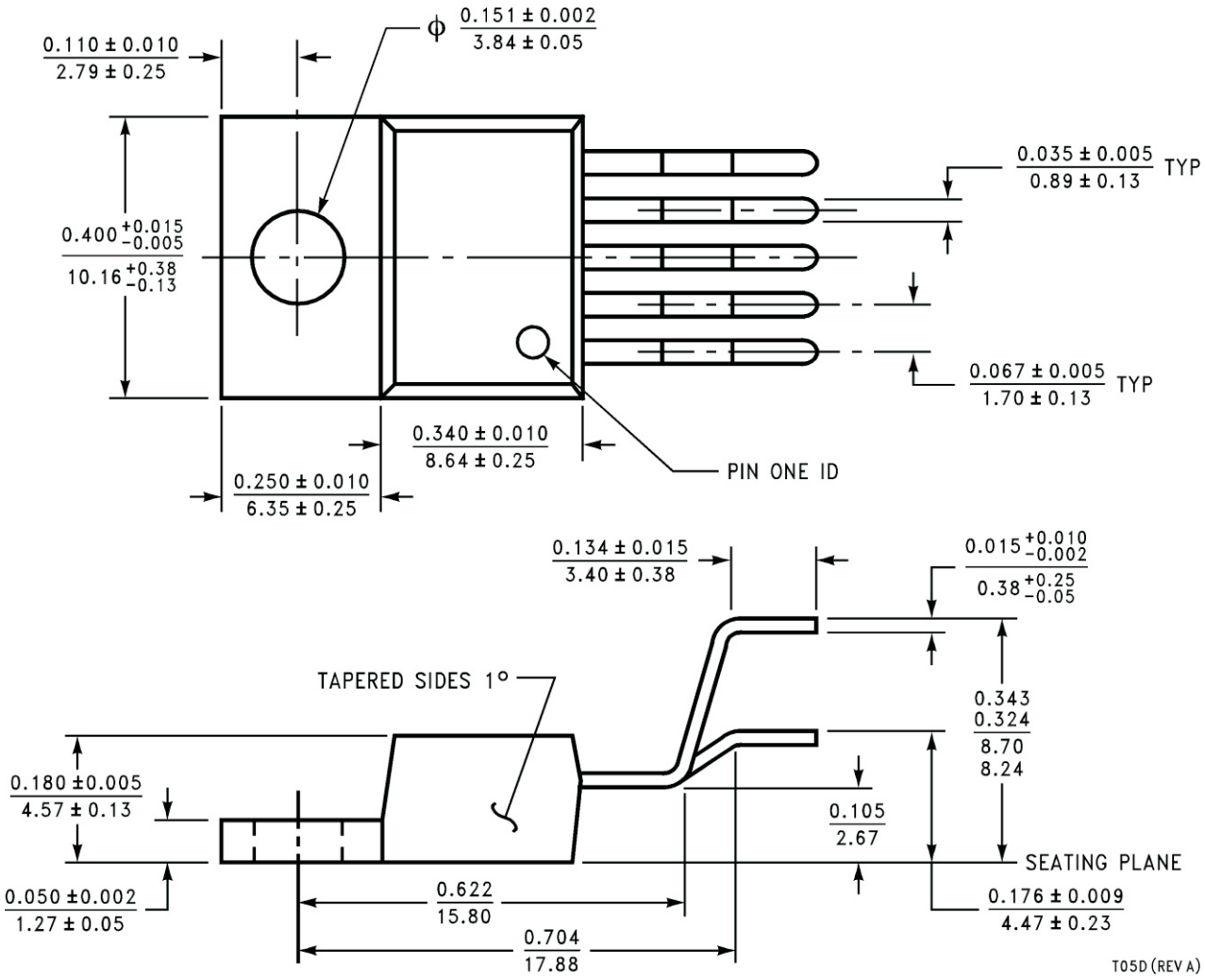
NDC0005A




DIMENSIONS ARE IN MILLIMETERS

MP05A (Rev A)

NDH0005D


0.110 ± 0.010
2.79 ± 0.25
ϕ 0.151 ± 0.002
3.84 ± 0.05
0.035 ± 0.005
0.89 ± 0.13 TYP
0.400 +0.015 −0.005
10.16 +0.38 −0.13
0.067 ± 0.005
1.70 ± 0.13 TYP
0.340 ± 0.010
8.64 ± 0.25
PIN ONE ID
0.250 ± 0.010
6.35 ± 0.25
0.134 ± 0.015
3.40 ± 0.38
0.015 +0.010 −0.002
0.38 +0.25 −0.05
TAPERED SIDES 1°
0.343
0.324
8.70
8.24
0.180 ±0.005
4.57 ± 0.13
0.105
2.67
SEATING PLANE
0.050 ±0.002
1.27 ± 0.05
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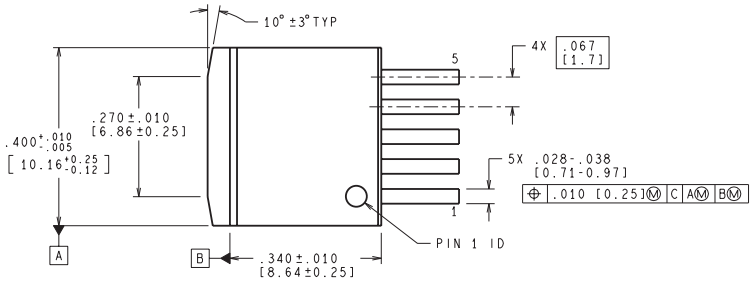
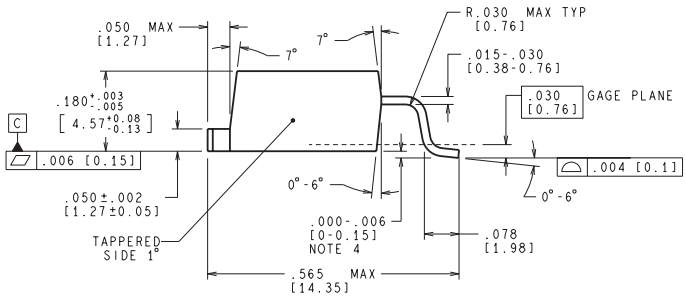
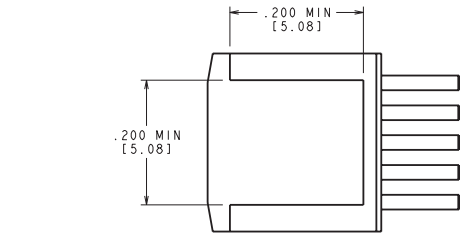
15.80
0.176 ± 0.009
4.47 ± 0.23
0.704
17.88
T05D (REV A)

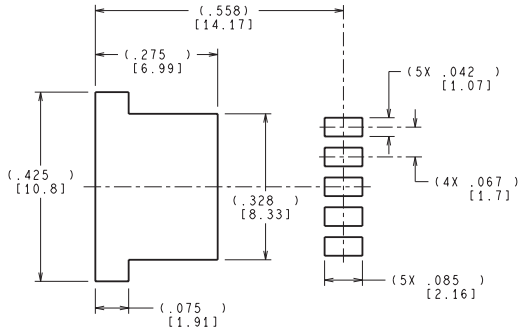
# KTT0005B




BOTTOM SIDE OF PACKAGE

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TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

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