Product/Process Change Notice - PCN 11_0267 Rev. -

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This notice is to inform you of a change that will be made to certain ADI products (see Material Report). Any issues with this PCN or requirements to qualify the change (additional data or samples) must be sent to ADI within 30 days of publication date. ADI contact information is listed below.

PCN Title: Minor Metal Mask Revision, Datasheet Changes and Test Manufacturing Site Change on the AD9557.

Publication Date: 11-Apr-2012

Effectivity Date: 10-Jul-2012 *(the earliest date that a customer could expect to receive changed material)*

Revision Description:

Initial Release

Description Of Change

Change#1:
The range of the system clock VCO has been extended from [765MHz-805MHz] to [750MHz-805MHz]

Change#2:
The default VCO calibration voltage for the output PLL (PLL2) has been increased by about 80mV
The default value for the register 0x0405 has changed. Register 0x0405[5] = 1 binary (Enhances the low temp operation. Already recommended.)

Change#3:
The PLL2 default current and loop filter settings have changed.
- The charge pump current has been changed from 371uA to 451.5uA
The default value for the register 0x0400 has changed from 0x6A to 0x81 (Improves phase noise. Already recommended in the previous DS, now a default condition).

- The loop filter default Cpole has changed from 80pF to 120pF
The loop filter default Rzero has changed from 1 KOhm to 1.5 KOhm
The default value for the register 0x0403 has changed from 0x12 to 0x07 (Improves phase noise. Already recommended in the previous DS, now a default condition).

Change#4:
The Silicon Revision (Register 0x000A) has changed from 0x20 to 0x21
- Register 0x000A=0x21 (No performance impact.)

Change#5 : Test Manufacturing Site Change:
This is notification that ADI is transferring the AD9557 from our test facility in Analog Devices Greensboro, NC to StatsChippac Singapore, our Teradyne UltraFlex qualified site

Reason For Change

Change#1 allows a larger range of possible external oscillators.

Change#2 allows an extended VCO range over Temperature

Change#3 and #4 allows to provide an improved jitter performance for the default configuration.

Reason for the change#5:
The transfer to test subcontractor, StatsChippac Singapore will increase tester capacity.

Impact of the change (positive or negative) on fit, form, function & reliability

The changes described above will not have any impact on the quality or reliability of the device.

Test Manufacturing Site change: there will be no impact on the form, fit, function, quality or reliability of these devices.

Summary of Supporting Information

Test correlation and validation has been performed, see attached report.

Supporting Documents

Attachment 1: Type: Test Correlation Report

ADI_PCN_11_0267_Rev_-_AD9557 Test Product Transfer Qualification.pdf

For questions on this PCN, send email to the regional contacts below or contact your local ADI sales representative					
Americas:	PCN_Americas@analog.com	**Europe:**	PCN_Europe@analog.com	**Japan:**	PCN_Japan@analog.com
				Rest of Asia:	PCN_ROA@analog.com

Appendix A - Affected ADI Models				
Added Parts On This Revision - Product Family / Model Number (3)				
AD9557 / AD9557/PCBZ	AD9557 / AD9557BCPZ	AD9557 / AD9557BCPZ-REEL7		

Appendix B - Revision History		
Rev	**Publish Date**	**Rev Description**
Rev. -	11-Apr-2012	Initial Release

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