AM26LV31E Low-Voltage High-Speed Quadruple Differential Line Driver With ±15-kV IEC ESD Protection

1 Features

- Meets or Exceeds Standards TIA/EIA-422-B and ITU Recommendation V.11
- Operates From a Single 3.3-V Power Supply
- ESD Protection for RS422 Bus Pins
  - ±15-kV Human-Body Model (HBM)
  - ±8-kV IEC61000-4-2, Contact Discharge
  - ±15-kV IEC61000-4-2, Air-Gap Discharge
- Switching Rates Up to 32 MHz
- Propagation Delay Time: 8 ns Typical
- Pulse Skew Time: 500 ps Typical
- High Output-Drive Current: ±30 mA
- Controlled Rise and Fall Times: 5 ns Typical
- Differential Output Voltage With 100-Ω Load: 2.6 V Typical
- Accepts 5-V Logic Inputs With 3.3-V Supply
- I_{off} Supports Partial-Power-Down Mode Operation
- Driver Output Short-Protection Circuit
- Glitch-Free Power-Up and Power-Down Protection
- Package Options: SO, SOIC, TSSOP, VQFN

2 Applications

- Motor Drives
- Space Avionics and Defense
- Medical Healthcare and Fitness
- Wireless Infrastructure
- Factory Automation and Control

3 Description

The AM26LV31E is a quadruple differential line driver with 3-state outputs. This driver has ±15-kV ESD (HBM and IEC61000-4-2, Air-Gap Discharge) and ±8-kV ESD (IEC61000-4-2, Contact Discharge) protection. This device is designed to meet TIA/EIA-422-B and ITU Recommendation V.11 drivers with reduced supply voltage.

The device is optimized for balanced-bus transmission at switching rates up to 32 MHz. The outputs have high current capability for driving balanced lines, such as twisted-pair transmission lines, and provide a high impedance in the power-off condition.

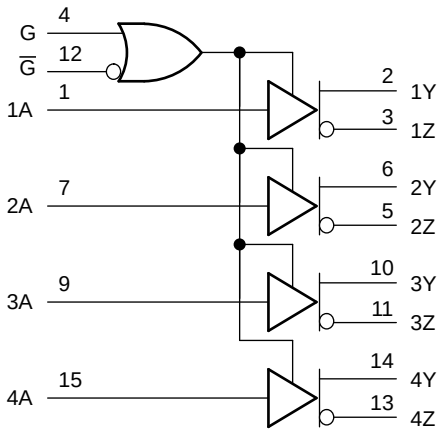
The AM26LV31EI is characterized for operation from –40°C to +85°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
AM26LV31EID	SOIC (16)	9.90 mm × 3.91 mm
AM26LV31EINS	SO (16)	10.30 mm × 5.30 mm
AM26LV31EIPW	TSSOP (16)	5.00 mm × 4.40 mm
AM26LV31EIRGY	VQFN (16)	4.00 mm × 3.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram



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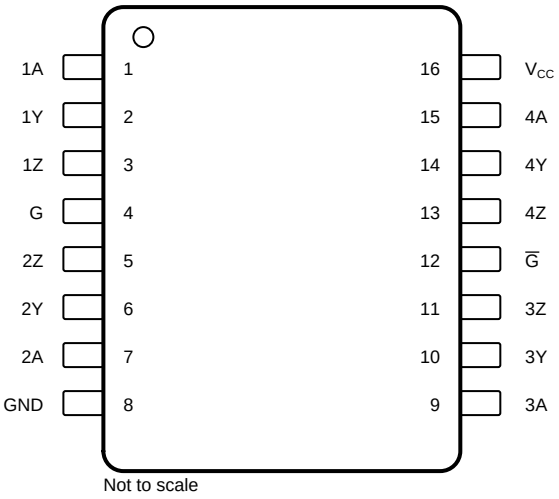
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May 2008) to Revision B	Page
• Added *Applications* section, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Deleted *Ordering Information* table, see *Mechanical, Packaging, and Orderable Information* at the end of the datasheet	1
• Changed *ESD PROTECTION* to *ESD Ratings* table	4
• Changed $R_{\theta JA}$ for PW package from 108°C/W: to 99.5°C/W	5
• Changed $R_{\theta JA}$ for NS package from 64°C/W: to 74.5°C/W	5
• Changed $R_{\theta JA}$ for RGY package from 39°C/W: to 39.3°C/W	5

5 Pin Configuration and Functions

D, NS, or PW Package
16-Pin SOIC, SO, TSSOP
Top View



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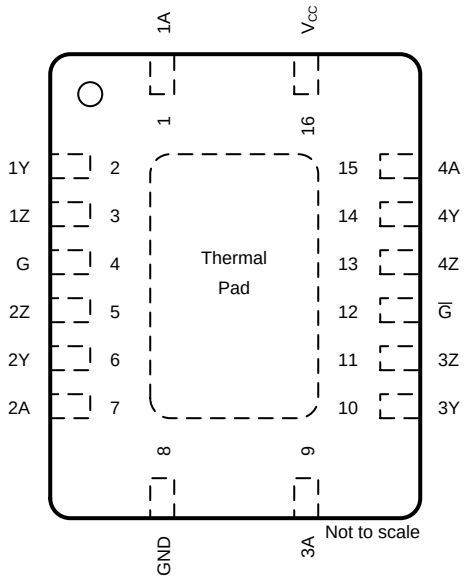
RGY Package
16-Pin VQFN With Thermal Pad
Top View



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Pin Functions

PIN		I/O	DESCRIPTION
NAME	SOIC, SO, TSSOP, VQFN		
1A	1	I	Logic data input to RS422 driver 1
1Y	2	O	RS-422 data line for driver 1
1Z	3	O	RS-422 data line for driver 1
2A	7	I	Logic data input to RS422 driver 2
2Y	6	O	RS-422 data line for driver 2
2Z	5	O	RS-422 data line for driver 2
3A	9	I	Logic data input to RS422 driver 3
3Y	10	O	RS-422 data line for driver 3
3Z	11	O	RS-422 data line for driver 3
4A	15	I	Logic data input to RS422 driver 4
4Y	14	O	RS-422 data line for driver 4
4Z	13	O	RS-422 data line for driver 4
G	4	I	Driver enable (active high)
$\overline{G}$	12	I	Driver enable (active low)
GND	8	—	Device ground pin
V_{CC}	16	—	Power input (5 V)

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		–0.5	6	V
V_I	Input voltage		–0.5	6	V
V_O	Output voltage		–0.5	6	V
I_{IK}	Input clamp current	$V_I < 0$		–20	mA
I_{OK}	Output clamp current	$V_O < 0$		–20	mA
I_O	Continuous output current			±150	mA
	Continuous current through V_{CC} or GND			±200	mA
T_J	Operating virtual junction temperature			150	°C
T_A	Operating free-air temperature		–40	85	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential input voltage are with respect to the network GND.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Bus pins 2, 3, 5, 6, 10, 11, 13, and 14	±15000	V
			All pins except 2, 3, 5, 6, 10, 11, 13, and 14	±2000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1000	
		IEC 61000-4-2 contact discharge	Bus pins 2, 3, 5, 6, 10, 11, 13, and 14	±8000	
		IEC 61000-4-2 air-gap discharge	Bus pins 2, 3, 5, 6, 10, 11, 13, and 14	±15000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_I	Input voltage	0		5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			–30	mA
I_{OL}	Low-level output current			30	mA
T_A	Operating free-air temperature	–40		85	°C

6.4 Thermal Information

THERMAL METRIC[1]		AM26LV31E				UNIT
		D (SOIC)	PW (TSSOP)	NS (SO)	RGY (VQFN)	
		16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	73.0	99.5	74.5	39.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.8	34.9	31.6	31.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31.0	44.4	35.3	14.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.1	2.4	5.3	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	30.7	43.8	35.0	14.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	3.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
V_{OH}	High-level output voltage	V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = –20 mA	2.4	3		V
V_{OL}	Low-level output voltage	V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA		0.2	0.4	V
$\lvert V_{OD1}\rvert$	Differential output voltage	I_O = 0 mA	2		4	V
$\lvert V_{OD2}\rvert$	Differential output voltage	R_L = 100 Ω (see Figure 3)	2	2.6		V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage	R_L = 100 Ω (see Figure 3)			±0.4	V
V_{OC}	Common-mode output voltage	R_L = 100 Ω (see Figure 3)		1.5	2	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage	R_L = 100 Ω (see Figure 3)			±0.4	V
$I_{O(OFF)}$	Output current with power off	V_{CC} = 0, V_O = –0.25 V or 5.5 V			±100	μA
I_{OZ}	High-impedance state output current	V_O = –0.25 V or 5.5 V, G = 0.8 V or $\overline{G}$ = 2 V			±100	μA
I_I	Input current	V_{CC} = 0 or 3.6 V, V_I = 0 or 5.5 V			±10	μA
I_{OS}	Short-circuit output current	V_O = V_{CC} or GND[2]	–30		–150	mA
I_{CC}	Supply current (total package)	V_I = V_{CC} or GND, No load, enable			100	μA
C_{pd}	Power dissipation capacitance	No load[3]		160		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
(3) C_{pd} determines the no-load dynamic current consumption. $I_S = C_{pd} \times V_{CC} \times f + I_{CC}$

6.6 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	See Figure 4	4	8	12	ns
t_{PLH}	Propagation delay time, low- to high-level output		4	8	12	ns
t_t	Transition time (t_r or t_f)	See Figure 4		5	10	ns
t_{PZH}	Output-enable time to high level	See Figure 5		10	20	ns
t_{PZL}	Output-enable time to low level	See Figure 6		10	20	ns
t_{PHZ}	Output-disable time from high level	See Figure 5		10	20	ns
t_{PLZ}	Output-disable time from low level	See Figure 6		10	20	ns
$t_{sk(p)}$	Pulse skew	See Figure 4(2)(3)		0.5	1.5	ns
$t_{sk(o)}$	Skew limit (pin to pin)				1.5	ns
$t_{sk(lim)}$	Skew limit (device to device)				3	ns
$f_{(max)}$	Maximum operating frequency	See Figure 4		32		MHz

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) Pulse skew is defined as the $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
(3) Skew limit (device to device) is the maximum difference in propagation delay times between any two channels of any two devices.

6.7 Typical Characteristics

Figure 1 and Figure 2 below show typical I_{CC} values at various frequencies/data rates for various termination conditions.

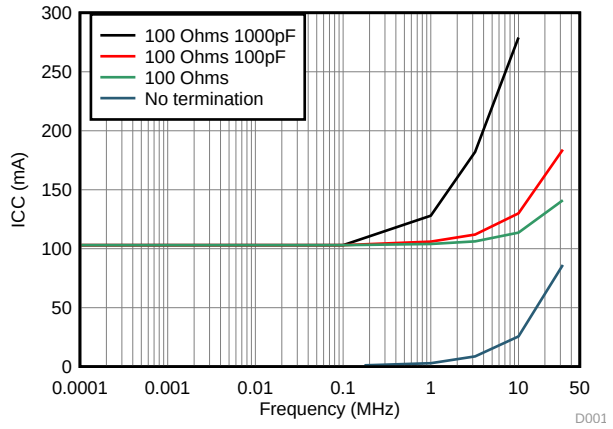


Figure 1. I_{CC} vs. Frequency

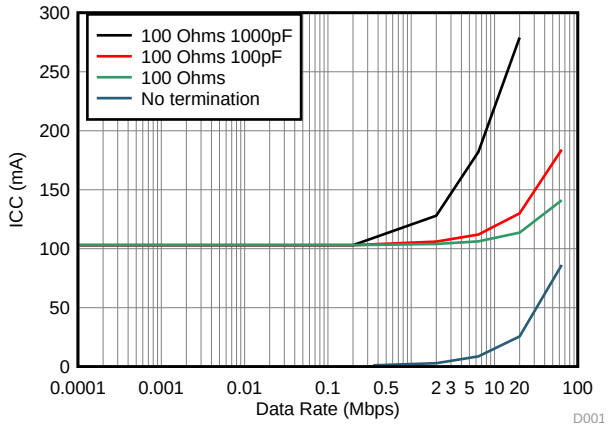


Figure 2. I_{CC} vs. Data Rate

7 Parameter Measurement Information

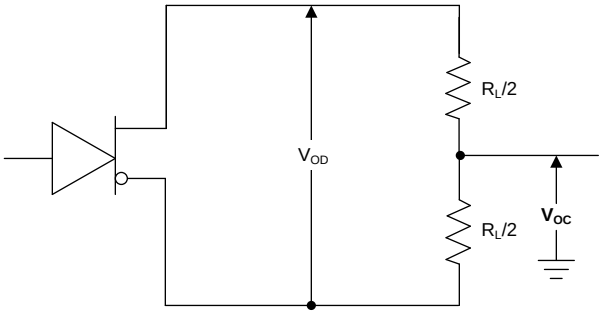
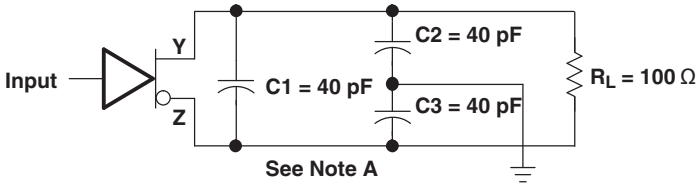
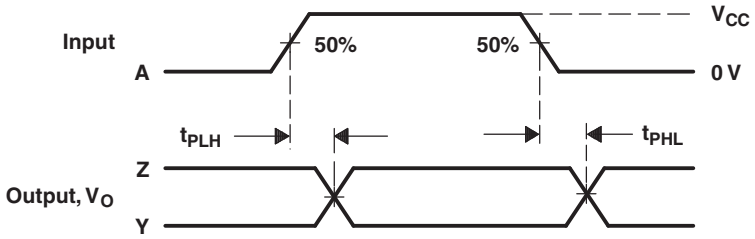
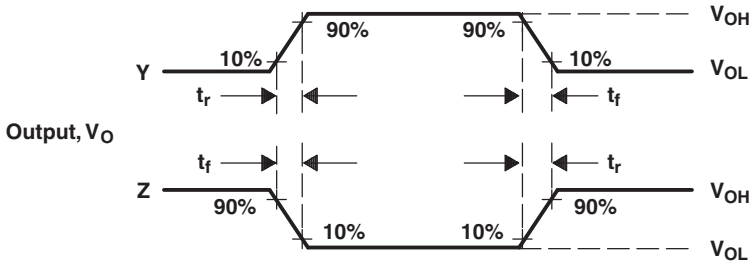


Figure 3. Test Circuit, V_{OD} and V_{OC}





PROPAGATION DELAY TIMES

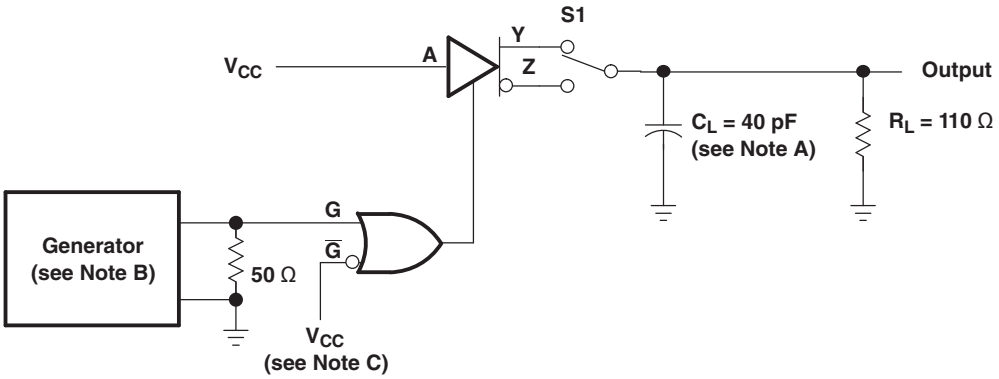


RISE AND FALL TIMES

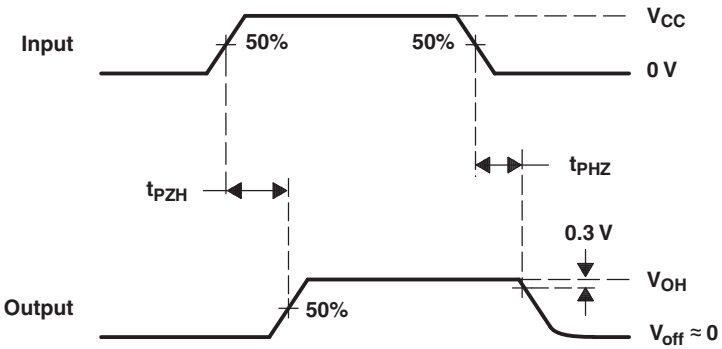
NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR = 32 MHz, 50% duty cycle, t_r and t_f ≤ 2 ns.

Figure 4. Test Circuit and Voltage Waveforms, t_{PHL} and t_{PLH}

Parameter Measurement Information (continued)



TEST CIRCUIT

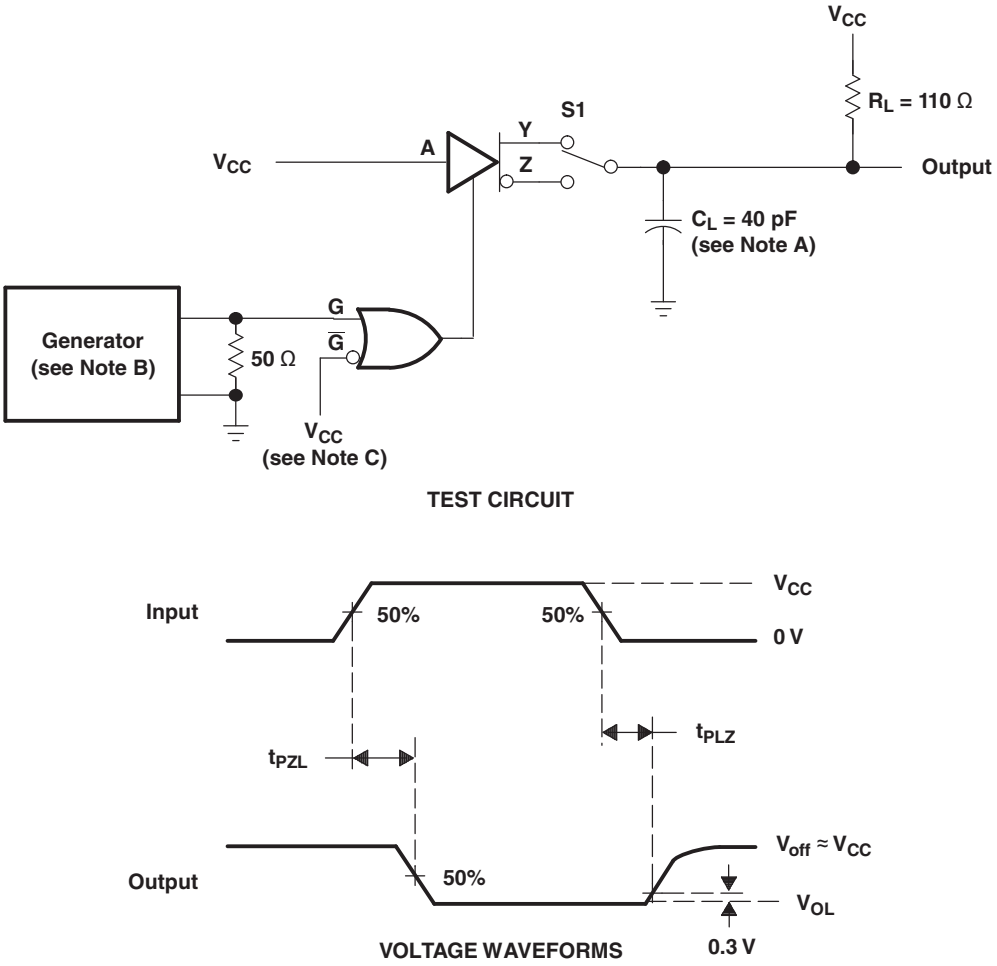


VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, t_r and t_f ≤ 2 ns.
C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform to $\overline{G}$

Figure 5. Test Circuit and Voltage Waveforms, t_{PZH} and t_{PHZ}

Parameter Measurement Information (continued)



NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, t_r and t_f ≤ 2 ns.
C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform to $\overline{G}$

Figure 6. Test Circuit and Voltage Waveforms, t_{PZL} and t_{PLZ}

8 Detailed Description

8.1 Overview

The AM26LV31E is a quadruple differential line driver with 3-state outputs. The device is designed to meet TIA/EIA-422-B and ITU Recommendation V.11 drivers with reduced supply voltage. The high current capability of the outputs allow for driving balanced lines, such as twisted-pair transmission lines, and proved a high impedance in the power-off condition. The AM26LV31E is optimized for balanced-bus transmission line at switching rates up to 32 MHz.

From a single 3.3-V power supply, the device operates four 3-state differential line drivers with integrated active high and active low enables for precise control. The device is capable of accepting 5-V logic inputs with a 3.3-V supply. The driver is designed to handle loads of a minimum of ±30 mA of sink or source current.

8.2 Functional Block Diagram

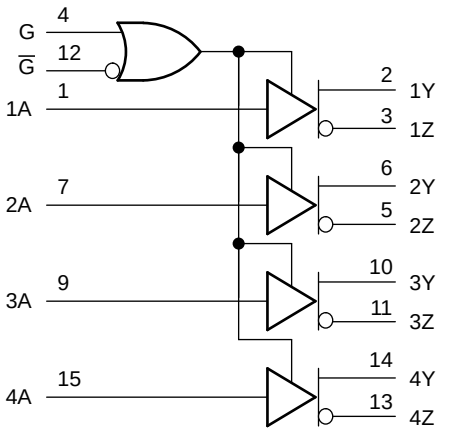


Figure 7. Logic Diagram

8.3 Feature Description

8.3.1 Complementary Out-Enable Inputs

The AM26LV31E transmitter outputs can be configured using the G and $\overline{G}$ logic inputs. The transmitter outputs are enabled when either G is set to logic HIGH or $\overline{G}$ is set to logic LOW. The reverse disables the outputs (G = LOW, $\overline{G}$ = HIGH). See Table 1 for the complete truth table.

8.3.2 High Output Impedance for Specific Driver Enable Inputs

When the AM26LV31E transmitter outputs are disabled using G and $\overline{G}$ logic inputs, the outputs are set to a high impedance state.

8.4 Device Functional Modes

Table 1 lists the functional modes of the AM26LV31E.

Table 1. Function Table(1)

INPUT A	ENABLES		OUTPUTS	
	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off)

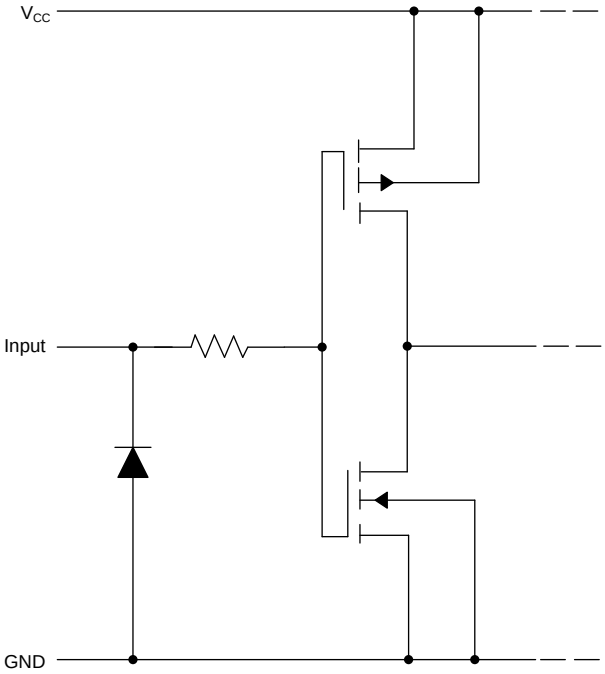


Figure 8. Equivalent of Each Input (A, G, or $\overline{G}$) Schematic

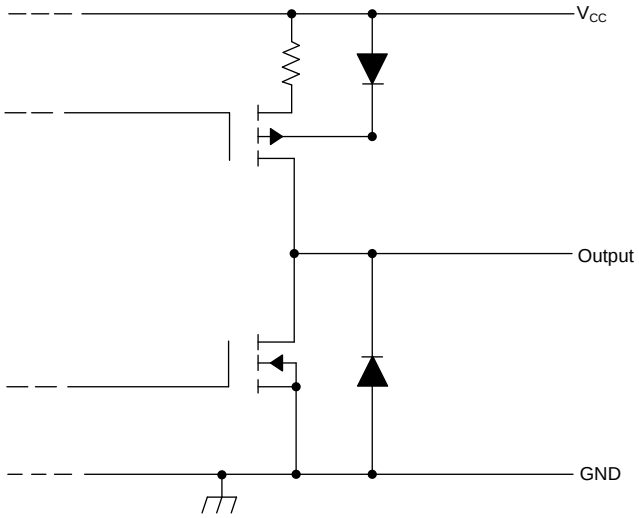


Figure 9. Typical of Each Driver Output Schematic

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

When designing a system that uses drivers, receivers, and transceivers that comply with RS-422 or RS-485, proper cable termination is essential for highly reliable applications with reduced reflections in the transmission line. Because RS-422 allows only one driver on the bus, if termination is used, it is placed only at the end of the cable near the last receiver. In general, RS-485 requires termination at both ends of the cable. Factors to consider when determining the type of termination usually are performance requirements of the application and the ever-present factor, cost. The different types of termination techniques discussed are unterminated lines, parallel termination, AC termination, and multipoint termination. Laboratory waveforms for each termination technique (except multipoint termination) illustrate the usefulness and robustness of RS-422 (and indirectly, RS-485). Similar results can be obtained if 485-compliant devices and termination techniques are used. For laboratory experiments, 100 feet of 100-Ω, 24-AWG, twisted-pair cable (Bertek) was used. A single driver and receiver, TI AM26LV31E and AM26LV32E, respectively, were tested at room temperature with a 3.3-V supply voltage. To show voltage waveforms related to transmission-line reflections, the first plot shows output waveforms from the driver at the start of the cable (A/B); the second plot shows input waveforms to the receiver at the far end of the cable (Y).

9.2 Typical Application

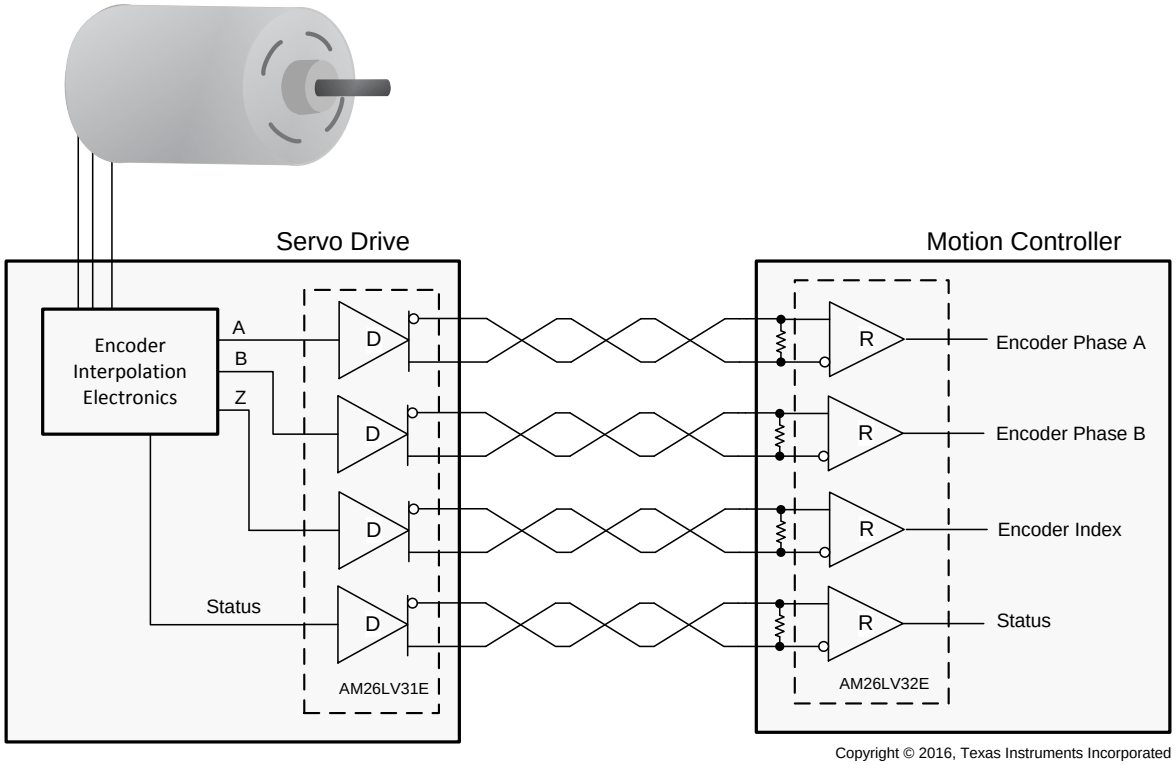


Figure 10. Encoder Application

Typical Application (continued)

9.2.1 Design Requirements

This example requires the following:

- 3.3-V power source
- RS-485 bus operating at speed compatible with cable length
- Connector that ensures the correct polarity for port pins

9.2.2 Detailed Design Procedure

Place the device close to bus connector to keep traces (stub) short to prevent adding reflections to the bus line. If desired, add external fail-safe biasing to ensure 200 mV on the A-B port, if the drive is in high impedance state (see *Failsafe in RS-485 data buses*, SLYT080).

9.2.3 Application Curve

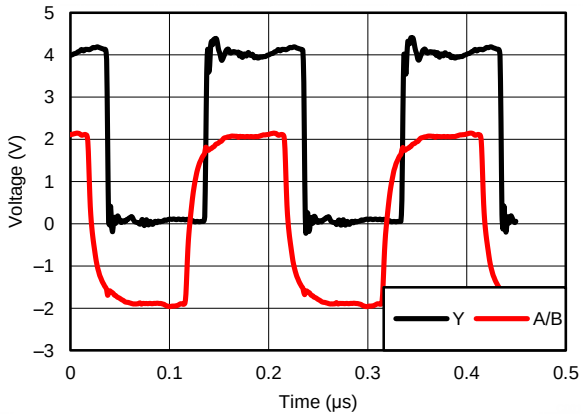


Figure 11. Differential 120-Ω Terminated Output Waveforms (Cat 5E Cable)

10 Power Supply Recommendations

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can often propagate into analog circuitry through the power supply of the circuit. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.

11.2 Layout Example

For all Y and Z outputs, make sure the traces are impedance matched to cable used.

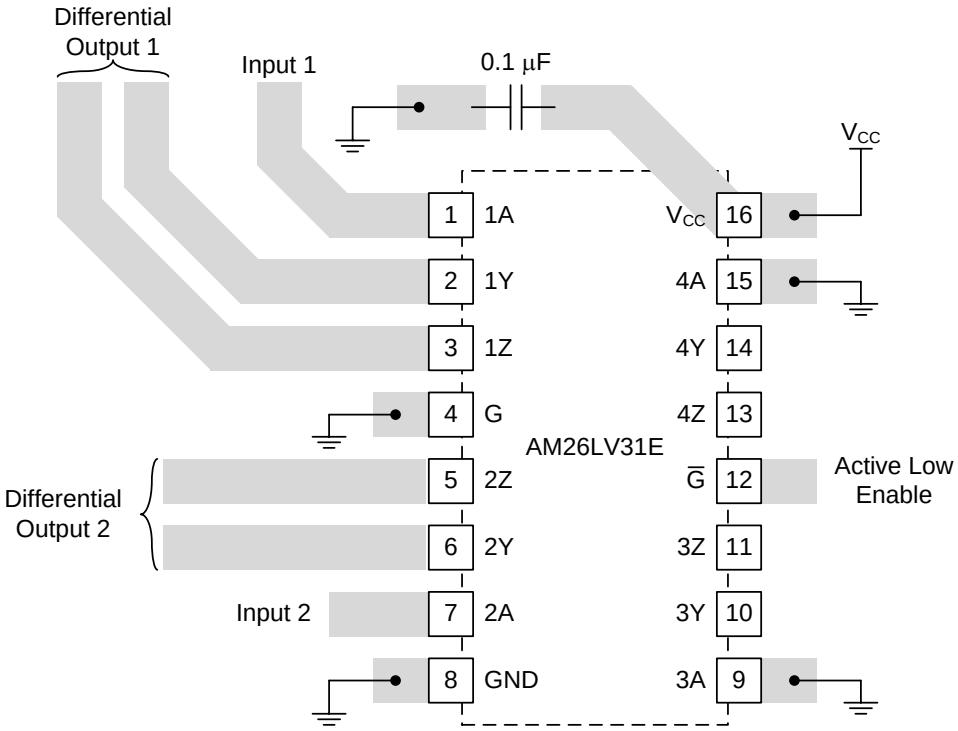


Figure 12. Layout Recommendation

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

Failsafe in RS-485 data buses, SLYT080

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AM26LV31EIDR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AM26LV31EI	Samples
AM26LV31EIDRG4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AM26LV31EI	Samples
AM26LV31EINSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	26LV31EI	Samples
AM26LV31EIPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SB31	Samples
AM26LV31EIPWRG4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SB31	Samples
AM26LV31EIRGYR	ACTIVE	VQFN	RGY	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SB31	Samples
AM26LV31EIRGYRG4	ACTIVE	VQFN	RGY	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SB31	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF AM26LV31E :

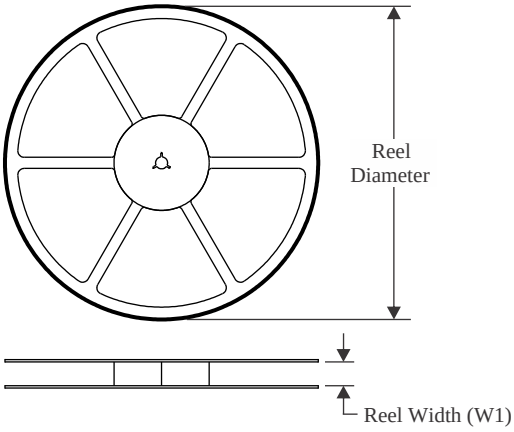
- Enhanced Product : AM26LV31E-EP

NOTE: Qualified Version Definitions:

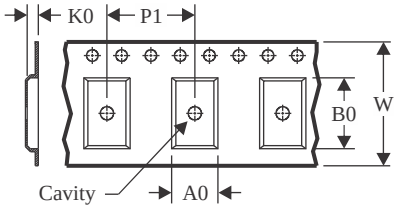
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

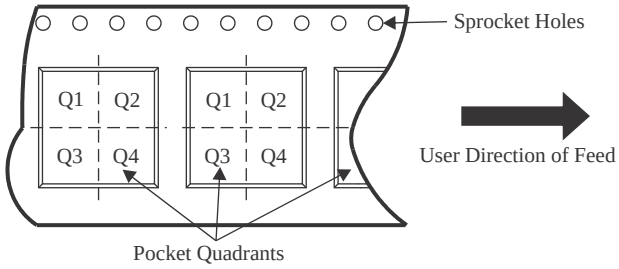


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

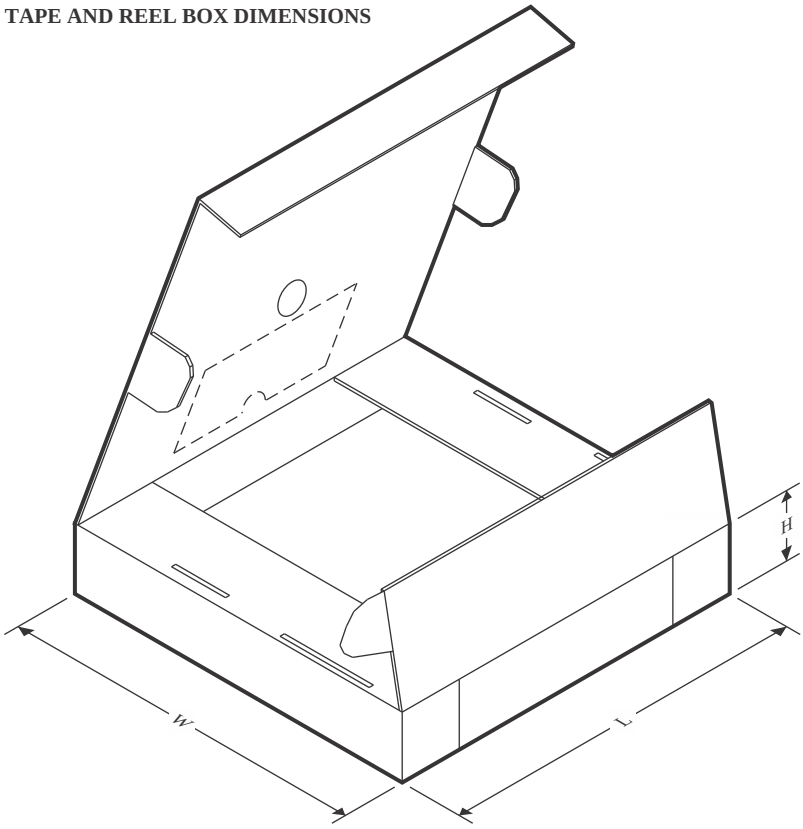
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AM26LV31EIDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26LV31EINSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
AM26LV31EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
AM26LV31EIRGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

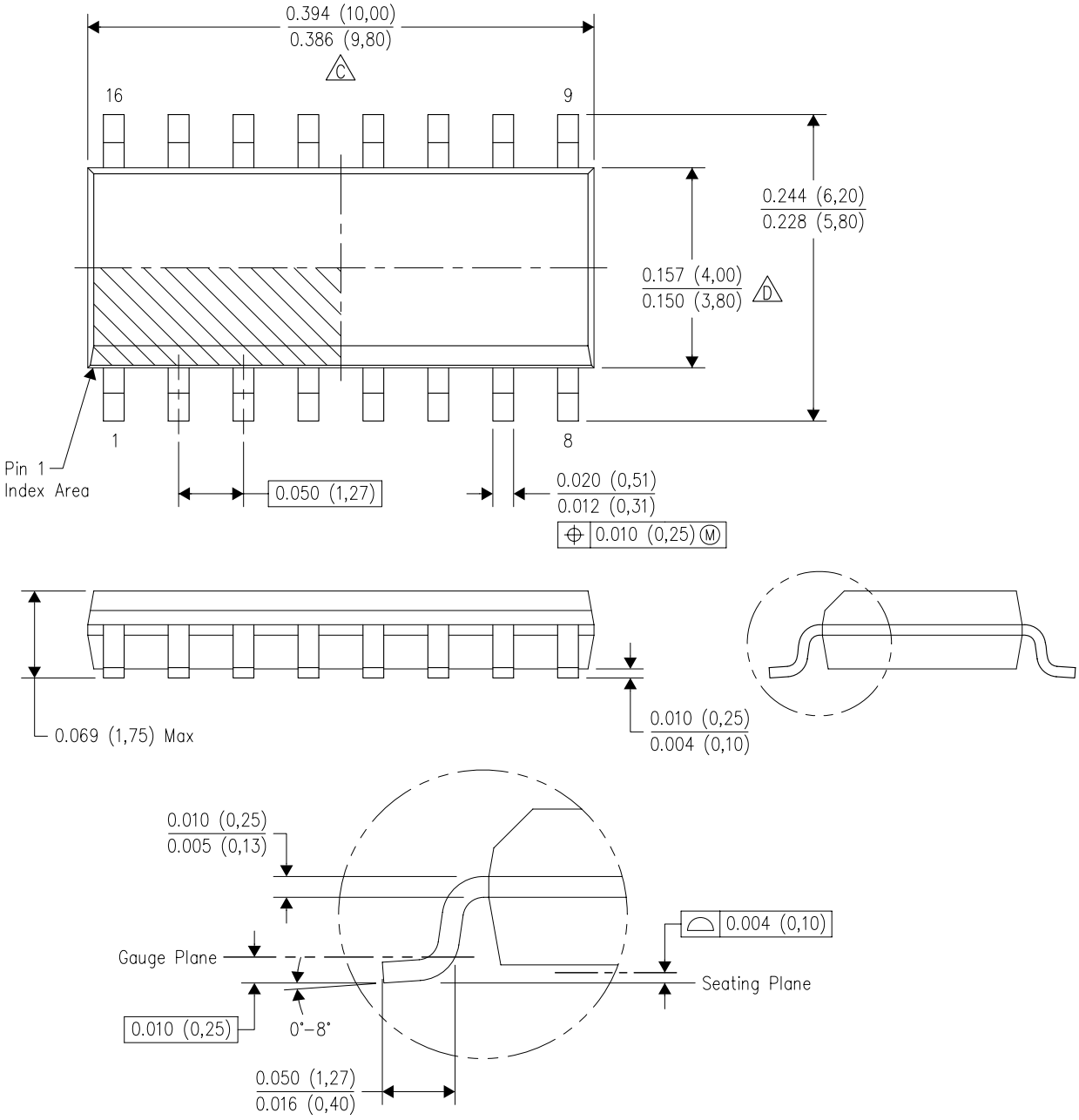
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AM26LV31EIDR	SOIC	D	16	2500	356.0	356.0	35.0
AM26LV31EINSR	SO	NS	16	2000	367.0	367.0	38.0
AM26LV31EIPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
AM26LV31EIRGYR	VQFN	RGY	16	3000	367.0	367.0	35.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



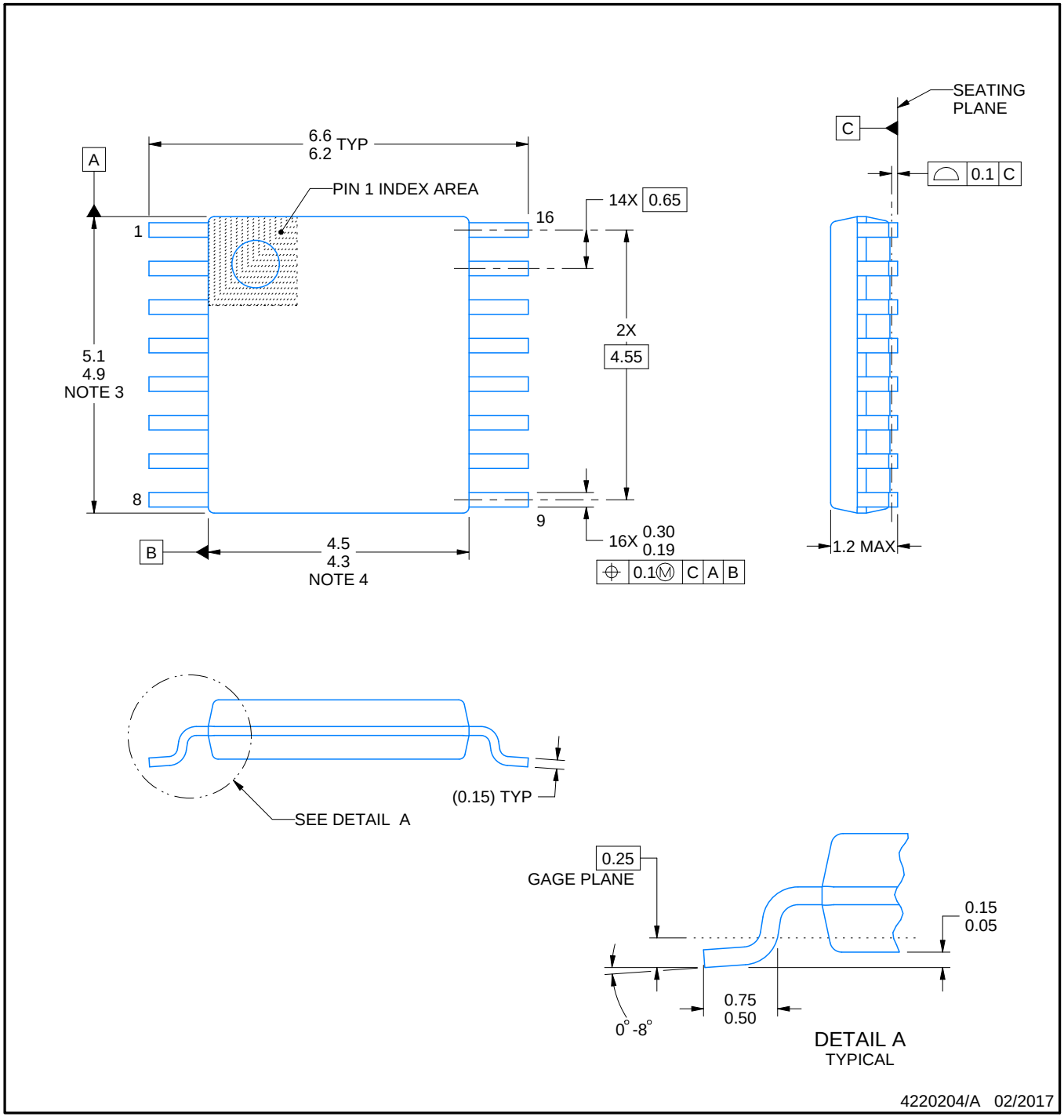
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

PACKAGE OUTLINE

PW0016A

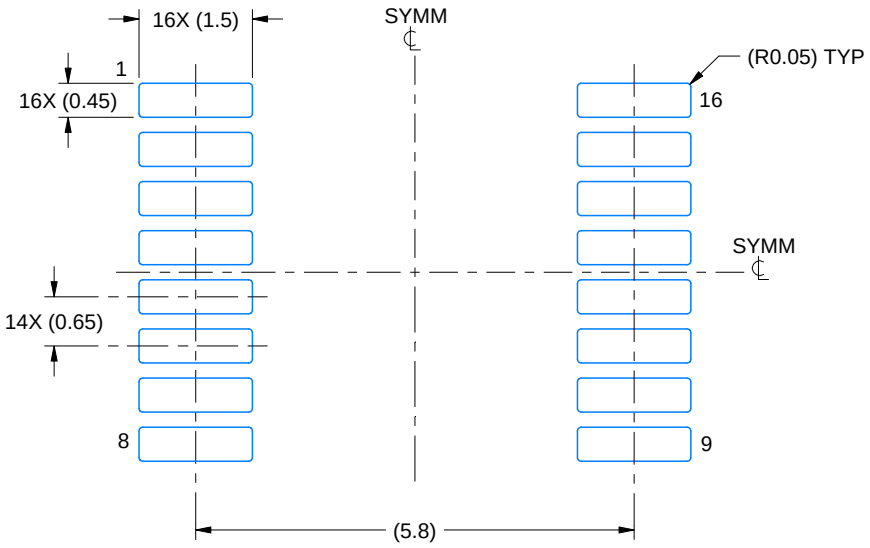
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

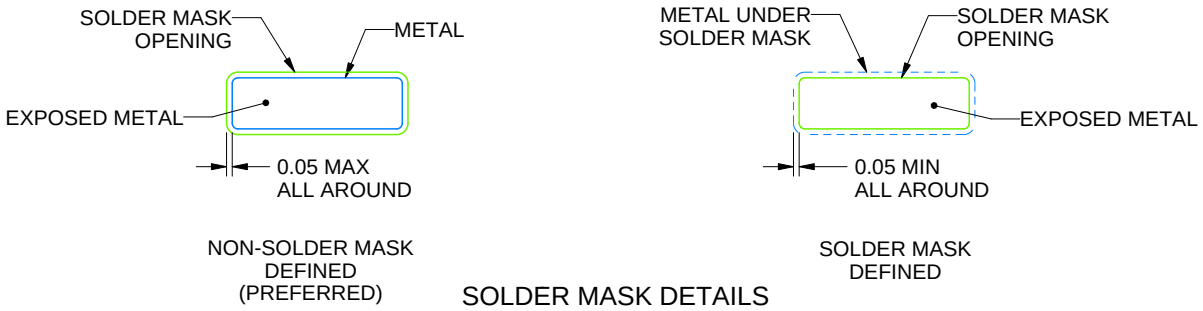


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

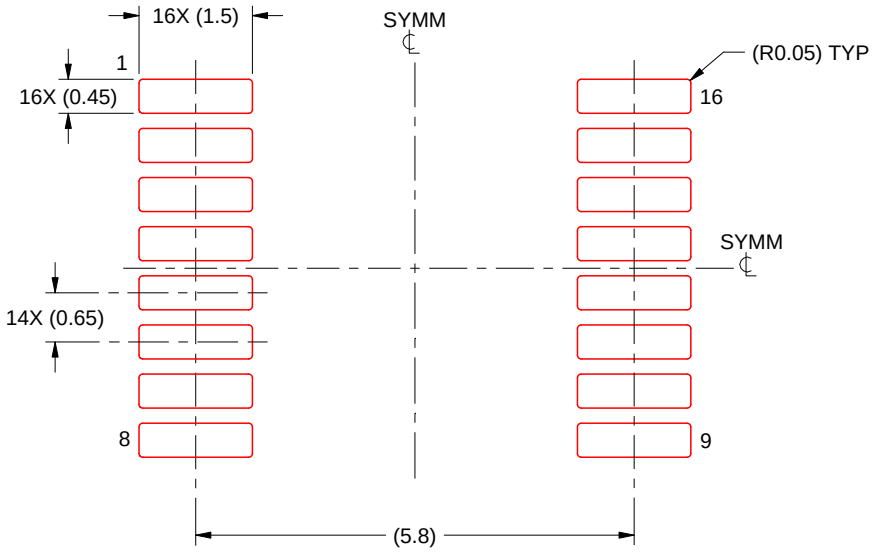


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

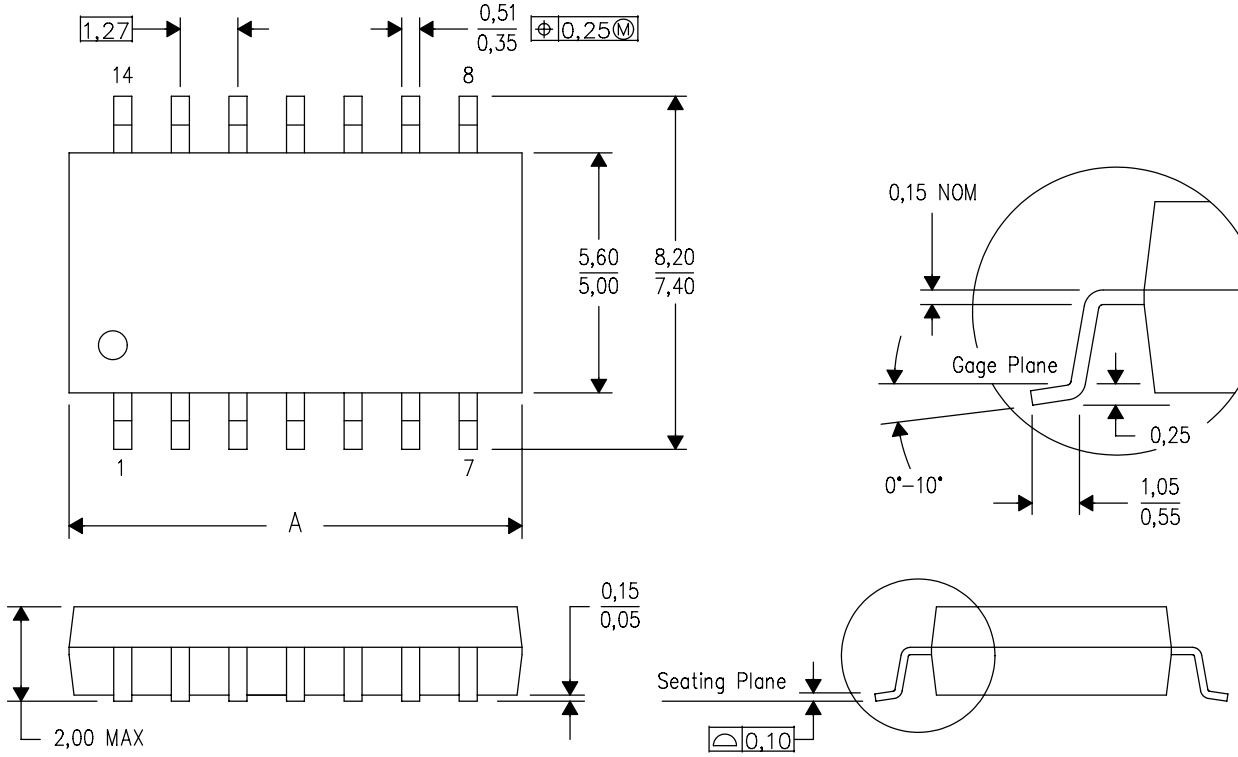
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

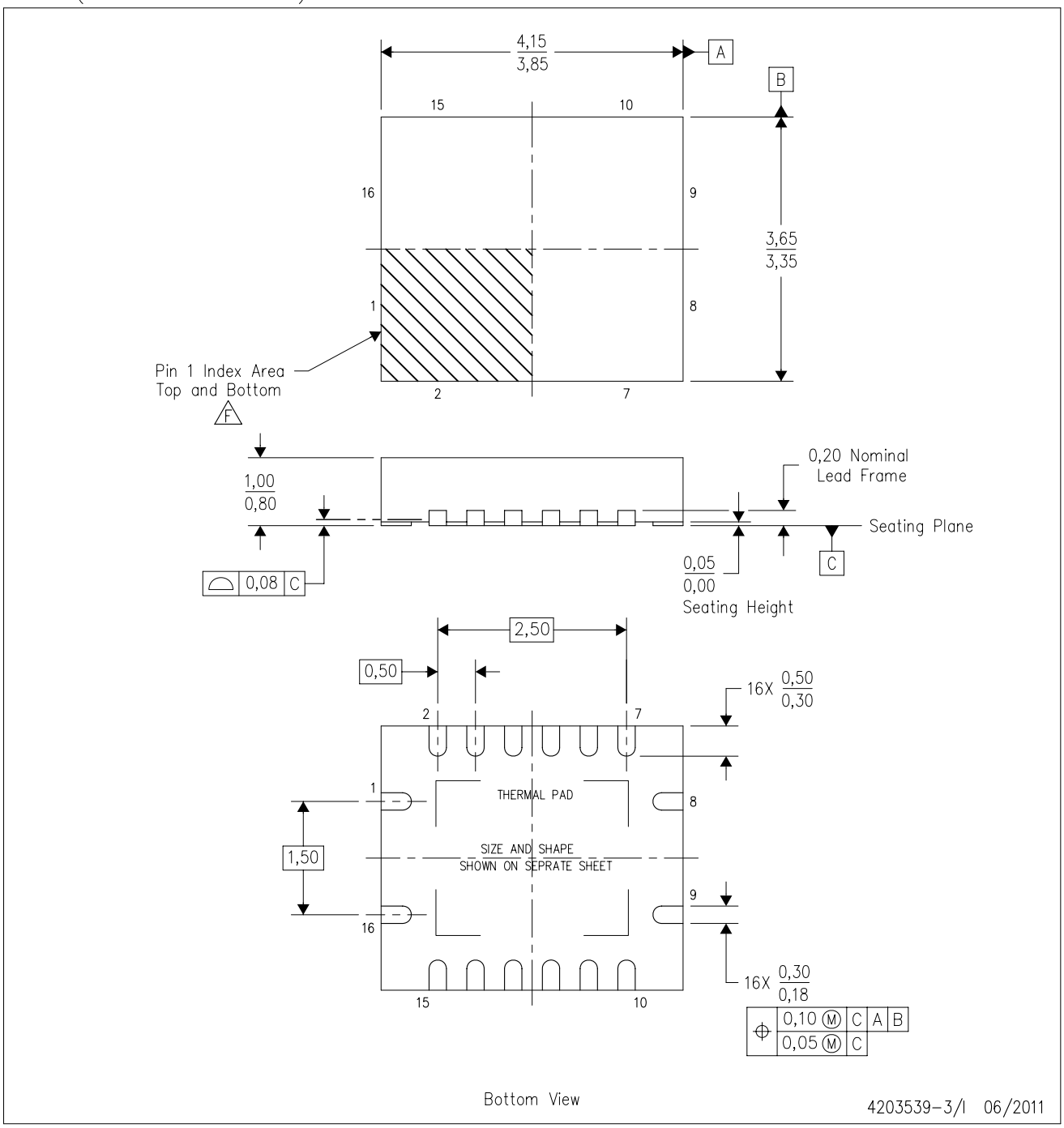


DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

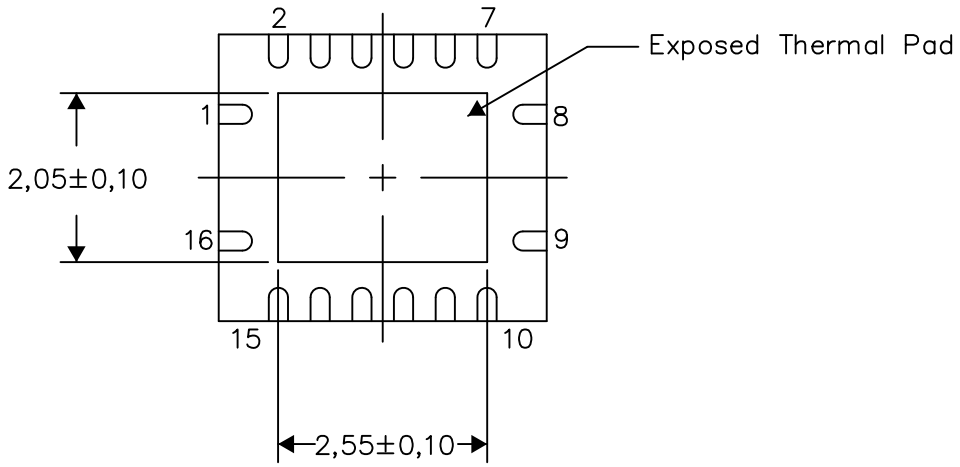
RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



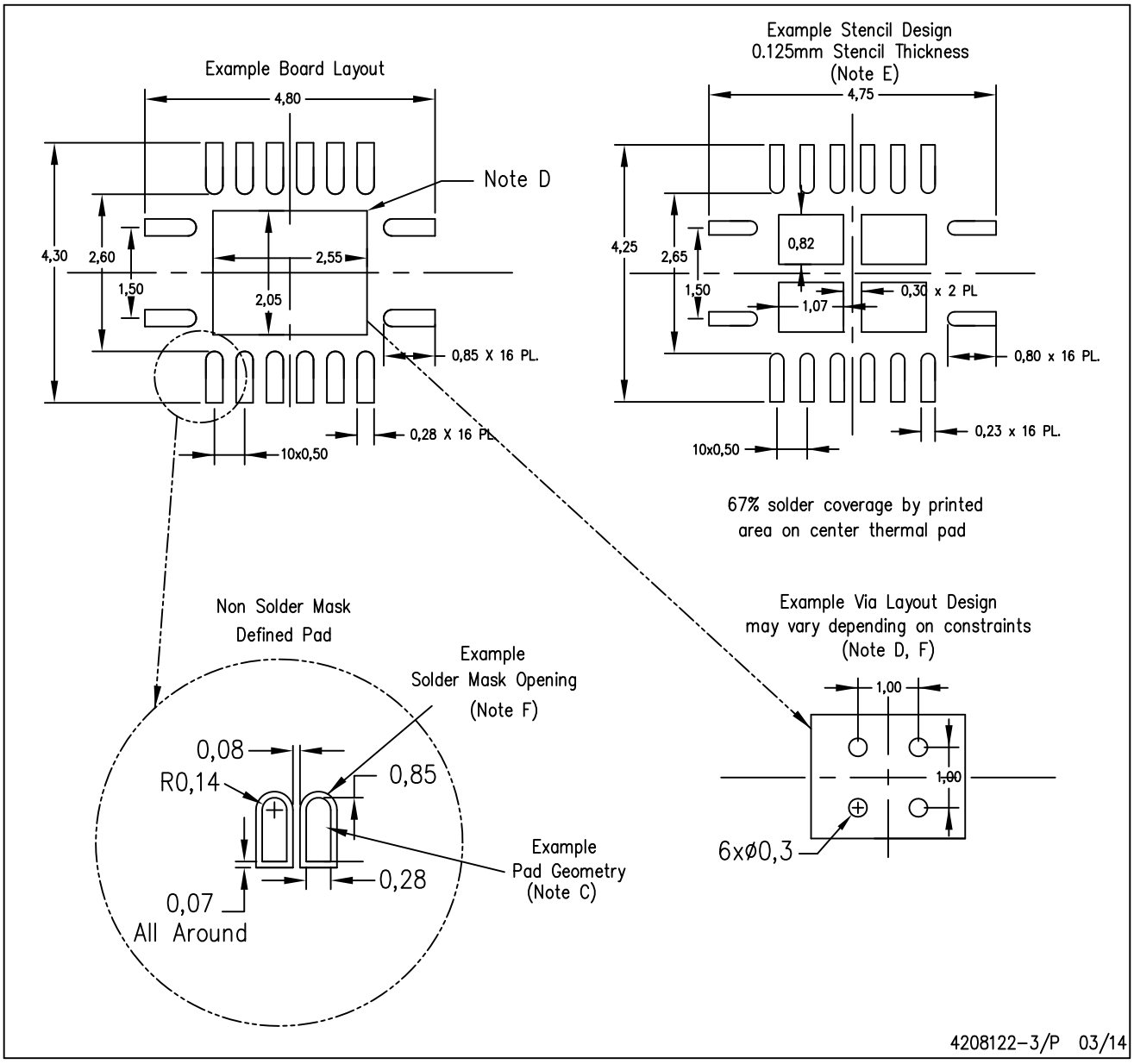
Bottom View

Exposed Thermal Pad Dimensions

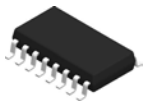
4206353–3/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

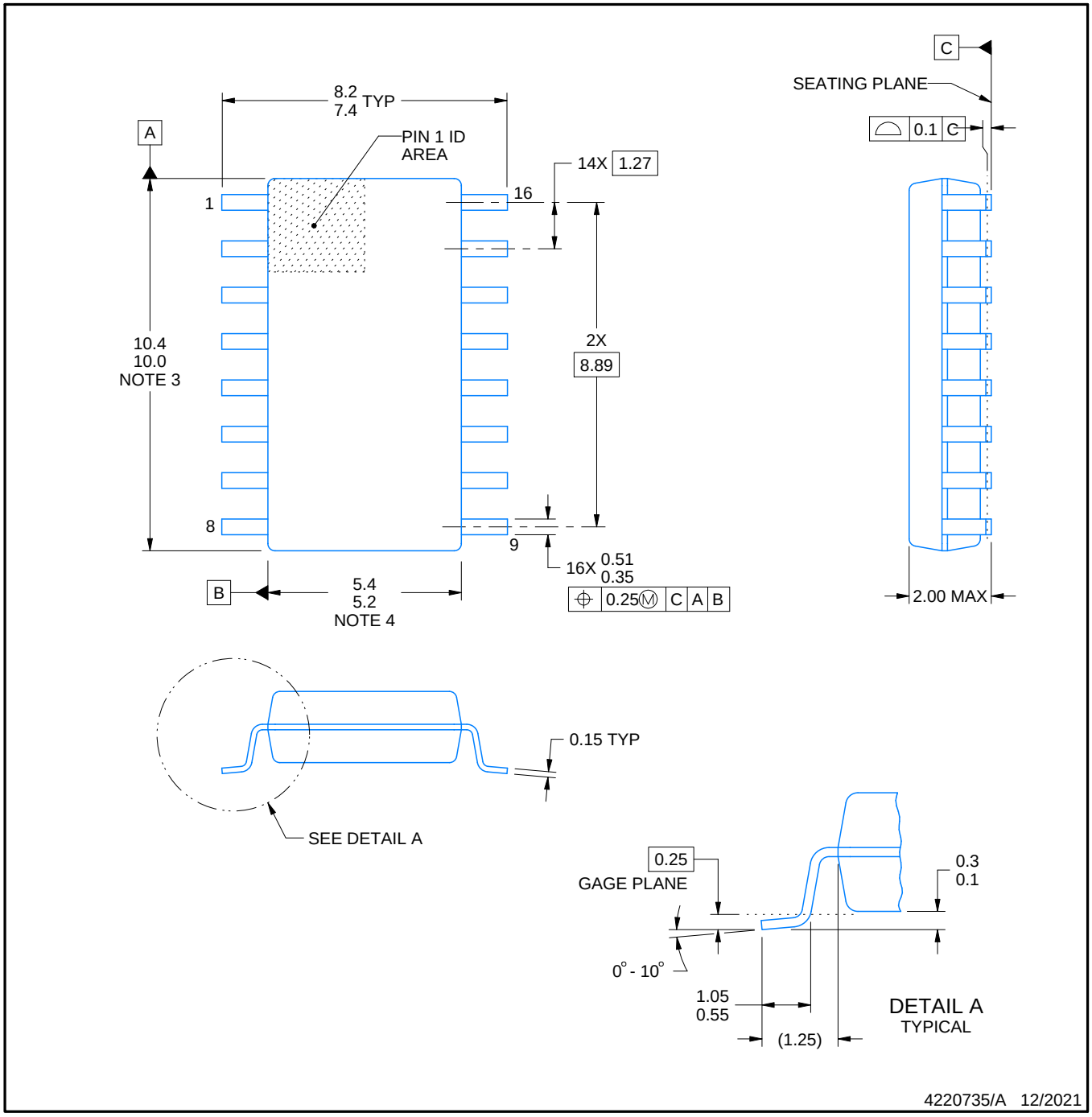


PACKAGE OUTLINE

NS0016A

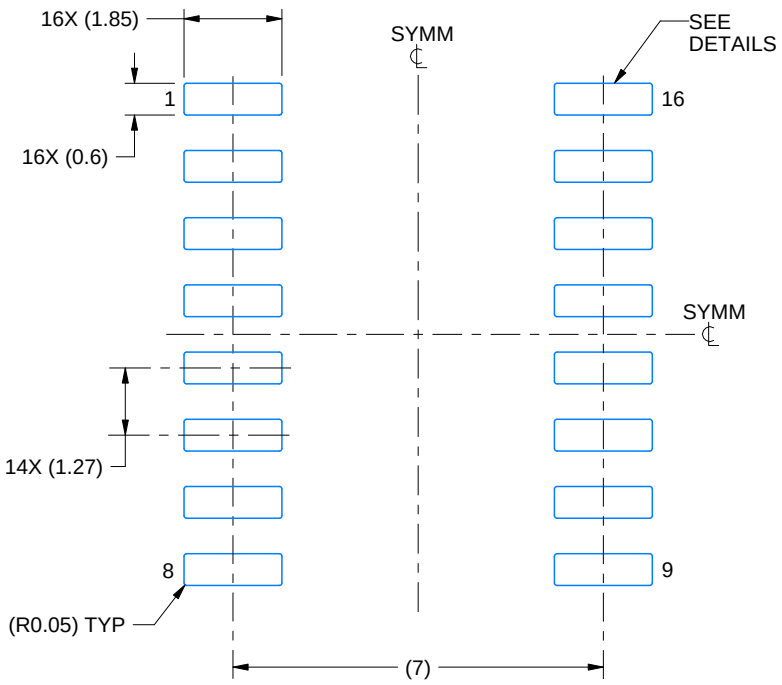
SOP - 2.00 mm max height

SOP

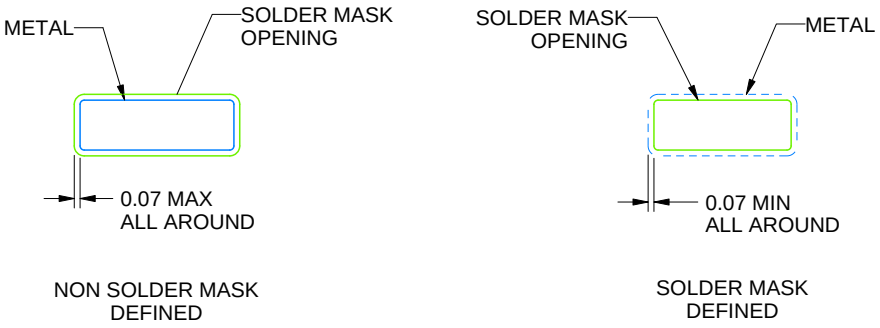


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

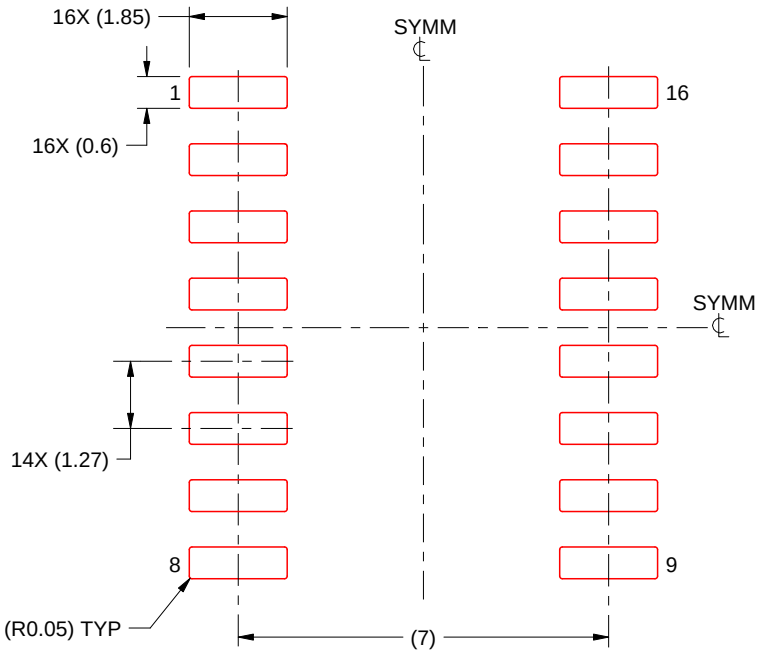
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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