August 1, 2016

Subject: PCN# 11A-16 Notification of Changes to the iCE40 Ultra and iCE40 UltraLite Data Sheets

Dear Lattice Customer,

Lattice Semiconductor is providing this notification of changes to the iCE40Ultra™ and iCE40UltraLite™ Data Sheets.

Change Description

The new iCE40 Ultra Family Data Sheet (DS1048 Version 2.0 released dated June 2016) and new iCE40 UltraLite Family Data Sheet (DS1050 Version 1.3 released dated July 2016) updates.

The key changes include the following:

1. DC and Switching Characteristics added the following sections:
    - Power-On Reset
    - Power-Up Supply Sequencing
    - External Reset
2. Recommended Operating Conditions
    - Updated V_{PP_2V5} Supply details
3. Master SPI Setup Time

See the data sheet revision history for other clarifications.

There is no change to any device bit stream design or iCEcube™ software.

Affected Products

The Ordering Part Numbers (OPNs) affected by this PCN are as follows:

ICE40UL1K

ICE40UL640

iCE5LP1K

iCE5LP2K

iCE5LP4K

Note: This PCN also affects all package, grade and tape / reel options (see appendix A for list) and any custom devices (i.e. factory programmed, special test, etc.) which are derived from any of the devices listed above.

Datasheet Specifications

The updated new iCE40 Ultra™ Family Data Sheet (DS1048 Version 2.0 dated June 2016) and new iCE40 UltraLite™ Family Data Sheet (DS1050 Version 1.3 dated July 2016) clarification described above and are available on the Lattice website.

Lattice Semiconductor Home Page: http://www.latticesemi.com

Recommended Action

Customers should check their designs with the three key changes described above, and take appropriate actions with the recommendations provided below:

1. **DC and Switching Characteristics added the following sections:**

   - Power-On Reset
   - Power-Up Supply Sequencing
   - External Reset

   Affected designs: This section specifies the power-up sequence to be V_{CC}/V_{CCPLL} -> SPI_V_{CCIO} -> V_{PP_2V5}, with CRESET_B kept LOW until all supplies are up or toggled CRESET_B from HIGH -> LOW -> HIGH. System designs that do not follow this sequence would be affected.

   Recommended Action: Customer will need to modify the power-up sequence on the board. If the customer's system design cannot meet the required sequence, please contact Lattice local field support listed below for additional help.

2. **Recommended Operating Conditions**

   - Updated V_{PP_2V5} Supply details

   Affected designs: In the Slave SPI Configuration Mode, designs that use any of the following function with VPP_2V5 set to 1.8V supply voltage would be affected:

   - HFOSC
   - LFOSC
   - RGB LED Driver
   - IR LED Driver
   - Barcode LED Driver (for iCE40UltraLite™)

   Recommended Action: Customer will need to provide V_{PP_2V5} with 2.5V or higher. If customer's board does not have any additional supply voltage other than 1.8V, please contact Lattice local field support listed below. A work-around can be provided with a design wrapper that uses some FPGA gates, with some degradation in accuracy of the OSC frequency or LED drive current.

3. **Master SPI Setup Time**

   Affected designs: MCLK setup time (t_{MTSU}) requirement is 9.9ns. Customer's designs that do not meet this timing in Master SPI Mode would be affected.

   Recommended Action: Customer will need to re-evaluate the system level timing on the MCLK sent out from the iCE40 device to fetch data from external SPI Flash, the arrival time of the SPI Flash data would meet this t_{MTSU} requirement or not. If this timing is not met, customer needs to modify this signal path to reduce the flight time to meet this timing parameter, including possibly adding a pipeline register, or reducing the MCLK frequency.

Customers who have further questions regarding this specification change are encouraged to contact local field support or at sales@latticesemi.com. It is not necessary to recompile the Lattice Diamond design in response to this notification.

PCN Timing

The datasheet changes are effective immediately and retroactively. There are no changes to the silicon and therefore samples are not applicable to these data sheet changes.

Lattice PCNs are available on the Lattice website. Please sign up to receive e-mail PCN alerts by registering here. If you already have a Lattice web account and wish to receive PCN alerts, you can do so by logging into your account and making edits to your subscription options.

Sincerely,

Lattice PCN Administration

Appendix A OPNs Affected

Product Line	Ordering Part Number (OPN)	Product Line	Ordering Part Number (OPN)	Product Line	Ordering Part Number (OPN)
ICE40UL640	ICE40UL640-CM36AI	**ICE40UL1K**	ICE40UL1K-CM36AI		
	ICE40UL640-CM36AITR		ICE40UL1K-CM36AITR		
	ICE40UL640-CM36AITR1K		ICE40UL1K-CM36AITR1K		
	ICE40UL640-SWG16ITR		ICE40UL1K-SWG16ITR		
	ICE40UL640-SWG16ITR1K		ICE40UL1K-SWG16ITR1K		
	ICE40UL640-SWG16ITR50		ICE40UL1K-SWG16ITR50		
ICE5LP1K	ICE5LP1K-SWG36ITR	**ICE5LP2K**	ICE5LP2K-SWG36ITR	**ICE5LP4K**	ICE5LP4K-SWG36ITR
	ICE5LP1K-SWG36ITR50		ICE5LP2K-SWG36ITR50		ICE5LP4K-SWG36ITR50
	ICE5LP1K-SWG36ITR1K		ICE5LP2K-SWG36ITR1K		ICE5LP4K-SWG36ITR1K
	ICE5LP1K-CM36ITR		ICE5LP2K-CM36ITR		ICE5LP4K-CM36ITR
	ICE5LP1K-CM36ITR1K		ICE5LP2K-CM36ITR1K		ICE5LP4K-CM36ITR1K
	ICE5LP1K-CM36ITR50		ICE5LP2K-CM36ITR50		ICE5LP4K-CM36ITR50
	ICE5LP1K-SG48ITR		ICE5LP2K-SG48ITR		ICE5LP4K-SG48ITR
	ICE5LP1K-SG48ITR50		ICE5LP2K-SG48ITR50		ICE5LP4K-SG48ITR50