MACRONIX INTERNATIONAL CO., LTD.

Product/Process Change Notice

PCN # P-1909-0004
Date: 2019/10/18

Dear Customer:

Please be informed that Macronix is going to use die with RDL (Re-direction Layer, or Metal 4) for MX25U8035EM2I-10G and MX25U1635EZUI-10G products. The die with the RDL (Re-direction Layer, or Metal 4) layer vs. without, the only difference is it has an extra RDL layer to re-layout the pad locations for wire-bond of KGD option of Macronix 8Mb/16Mb SPI Flash MX25U8035E/MX25U1635E product. The die with RDL also kept original pad locations and can be used for MX25U8035EM2I-10G and MX25U1635EZUI-10G (without RDL) package, with the same wire-bonds and functionality. Other than the RDL layer, there is no other changes on the product design nor on the specifications.

The detailed information about this change is described in the following pages. This process change has passed Macronix' characterization; the characterization results is attached.

If you have any questions, concerns, or requests about this change, please contact your local Macronix Sales Representatives within 30 days, otherwise Macronix will assume customer received the PCN with no comments and the change is acceptable to the customer. Macronix follows JEDEC J-STD-046, it stipulates: ".....Lack of acknowledgement of the PCN within 30 days constitutes acceptance of the change".

Thank you.

Macronix International Co., Ltd.
旺宏電子股份有限公司

(Note: For the customers who receive Macronix PCNs via distributors, Macronix will assist the distributors to convey the PCNs to the customers. It is each distributor's responsibility to communicate and track the responses of each customers and report back to Macronix, the distributor shall assume full responsibilities if failed to do so.)

PCN No.: P-1909-0004

Issue Date : 2019/10/18

Subject: To use die with RDL (metal 4) for MX25U8035EM2I-10G/MX25U1635EZUI-10G products..

Affected Macronix Part No.: MX25U8035EM2I-10G
MX25U1635EZUI-10G

Change Category : Product option

Reason of Change: To increase production capacity of MX25U8035EM2I-10G/MX25U1635EZUI-10G products.

Before Change :

MX25U8035EM2I-10G/MX25U1635EZUI-10G with standard die

After Change :

1) MX25U8035EM2I-10G/MX25U1635EZUI-10G with standard die
2) MX25U8035EM2I-10G/MX25U1635EZUI-10G with RDL die

Assessment of Change:

1. The purpose of the RDL is to re-layout the pad locations to allow wire-bond spacing for KGD product option, there is no other changes on the product design nor on the specifications.
2. With regards to the performance between standard die and RDL die, there is no impact on Fit, Form, Function, Quality and Reliability.

Schedule:

CS Sample available: 2019/11/18

Mass production: 2020/01/18.

Characterization Results of MX25U8035E/MX25U1635E with/without RDL

DC CHARACTERISTICS

SYMBOL	PARAMETER	NOTES	SPEC			UNITS	Standard die		Die with RDL	
			Min.	Typ.	Max.		Max.	Min.	Max.	Min.
ILI	Input Load Current	VCC= VCC Max, VIN= VCC or GND			±2	uA	0.001	0.001	0.001	0.001
ILO	Output Leakage Current	VCC= VCC Max, VOUT= VCC or GND			±2	uA	0.01	0.01	0.01	0.01
ISB1	VCC Standby Current	VIN= VCC or GND CS#= VCC		30	100	uA	61.20	36.80	28.50	18.58
ISB2	Deep Power-down Current	VIN= VCC or GND CS#= VCC		5	20	uA	2.33	0.52	1.39	0.31
ICC1	VCC Read	f= 104MHz,(4x I/O read) SCLK= 0.1VCC/0.9VCC, SO=Open			20	mA	15.60	11.91	14.42	11.59
		f=84MHz, SCLK= 0.1VCC/0.9VCC, SO=Open			15	mA	10.30	8.71	9.90	8.25
ICC2	VCC Program Current (PP)	Program in Progress CS#= VCC		20	25	mA	19.85	16.12	19.78	14.51
ICC3	VCC Write Status Register (WRSR) Current	Program status register in progress, CS#= VCC			20	mA	10.34	6.43	9.47	6.57
ICC4	VCC Sector/Block(32K/64K) Erase Current (SE/BE/BE32K)	Erase in Progress, CS#= VCC		20	25	mA	21.56	8.78	20.45	8.84
ICC5	VCC Chip Erase Current (CE)	Erase in Progress, CS#= VCC		20	25	mA	20.01	15.12	19.96	15.07
VIL	Input Low Voltage		-0.5		0.2VCC	V	0.90	0.60	0.90	0.70
VIH	Input High Voltage		0.8VCC		VCC+0.4	V	1.30	0.80	1.30	0.80
VOL	Output Low Voltage	IOL= 100uA			0.2	V	0.20	0.10	0.20	0.10
VOH	Output High Voltage	IOH=- 100uA	VCC-0.2			V	2.00	1.40	2.00	1.40

AC CHARACTERISTICS

Symbol	Alt.	Parameter		NOTES	SPEC			UNITS	Standard die		Die with RDL	
					Min.	Typ.	Max.		Max.	Min.	Max.	Min.
fSCLK	fC	Clock Frequency for the following instructions: FAST_READ,RDSFDP,PP, 4PP,SE, BE, CE, DP, RES, RDP WREN, WRDI, RDID, RDSR, WRSR			D.C.		104	MHz	200.00	169.49	200.00	166.67
fRSCLK	fR	Clock Frequency for READ instructions					33	MHz	61.34	51.28	60.61	51.02
fTSCLK	fT	Clock Frequency for 2READ instructions					84	MHz	161.29	121.95	163.93	136.99
	fQ	Clock Frequency for 4READ instructions					84/104	MHz	142.85	120.48	147.06	125.00
tCH	tCLH	Clock High Time	Others (fSCLK)		4.5			ns	1.00	1.00	1.00	1.00
			Normal Read (fRSCLK)		13			ns	1.90	1.00	1.80	1.00
tCL	tCLL	Clock Low Time	Others (fSCLK)		4.5			ns	1.80	1.30	1.70	1.30
			Normal Read (fRSCLK)		13			ns	1.60	1.40	1.50	1.40
tCLCH		Clock Rise Time (peak to peak)			0.1			V/ns	0.06	0.06	0.06	0.06
tCHCL		Clock Fall Time (peak to peak)			0.1			V/ns	0.06	0.06	0.06	0.06
tSLCH	tCSS	CS# Active Setup Time (relative to SCLK)			4			ns	1.80	1.20	1.80	1.20
tCHSL		CS# Not Active Hold Time (relative to SCLK)			4			ns	-2.000	-2.000	-2.000	-2.000
tDVCH	tDSU	Data In Setup Time			2			ns	1.200	1.100	1.200	1.100
tCHDX	tDH	Data In Hold Time			3			ns	0.800	0.200	0.800	0.200
tCHSH		CS# Active Hold Time(relative to SCLK)			5			ns	-2.000	-2.000	-2.000	-2.000
tSHCH		CS# Not Active Setup Time (relative to SCLK)			7			ns	0.90	0.50	0.90	0.50
tSHSL	tCSH	CS# Deselect Time	Read		12			ns	4.90	4.30	4.80	4.40
			Write/Erase/Program		30			ns	25.00	21.00	24.00	20.00
tSHQZ	tDIS	Output Disable Time					8	ns	2.00	2.00	2.00	2.00

AC CHARACTERISTICS

Symbol	Alt.	Parameter		NOTES	SPEC Min.	SPEC Typ.	SPEC Max.	UNITS	Standard die Max.	Standard die Min.	Die with RDL Max.	Die with RDL Min.
tCLQV	tV	Clock Low to Output Valid Loading:30pF/15pF	Loading:30pF				8	ns	8.00	5.00	8.00	5.00
			Loading:15pF				6	ns	4.80	2.90	4.50	2.50
tCLQX	tHO	Output Hold Time			0			ns	6.50	4.70	6.50	4.70
tWHSL		Write Protect Setup Time			20			ns	0.00	0.00	0.00	0.00
tSHWL		Write Protect Hold Time			100			ns	16.00	14.00	16.00	14.00
tDP		CS# High to Deep Power-down Mode					10	us	2.00	2.00	2.00	2.00
tRES1		CS# High to Standby Mode without Electronic Signature Read					10	us	0.01	0.00	0.01	0.00
tRES2		CS# High to Standby Mode with Electronic Signature Read					10	us	0.01	0.00	0.01	0.00
tRCR		CSRecovery Time from Read					20	us	0.03	0.02	0.03	0.02
tRCP		Recovery Time from Program					20	us	0.21	0.11	0.17	0.09
tRCE		Recovery Time from Erase					12	ms	5.10	3.90	4.80	3.80
tW		Write Status Register Cycle Time					40	ms	5.32	5.02	5.13	4.59
tBP		Byte-Program				8	30	us	12.52	11.38	11.76	10.89
tPP		Page Program Cycle Time				1.2	3	ms	1.33	1.09	1.31	1.11
tSE		Sector Erase Cycle Time				60	200	ms	40.02	36.52	39.54	35.31
tBE32		Block Erase(32K) Cycle Time				250	1000	ms	0.17	0.15	0.21	0.20
tBE		Block Erase(64K) Cycle Time				500	2000	ms	0.33	0.30	0.41	0.38
tCE		Chip Erase Cycle Time				9	20	s	8.19	6.95	9.53	7.89

Power-Up Timing and VWI Thresehold

Symbol	Parameter	NOTES	SPEC Min.	SPEC Typ.	SPEC Max.	UNITS	Standard die Max.	Standard die Min.	Die with RDL Max.	Die with RDL Min.
tVSL	VCC(min) to CS# low (VCC Rise Time)		300			us	60.00	60.00	60.00	60.00
tPUW	Time delay to Write instruction		1		10	ms	0.06	0.06	0.06	0.06
VWI	Command Inhibit Voltage		1		1.4	V	1.20	1.20	1.20	1.20