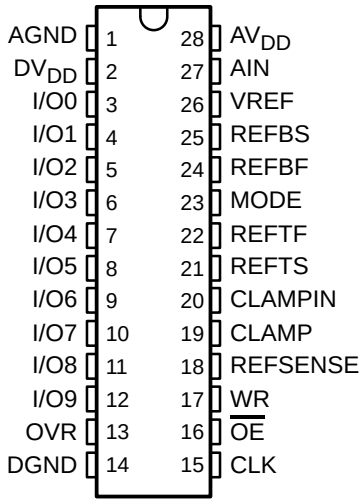
- **10-Bit Resolution, 30 MSPS Analog-to-Digital Converter**
- **Configurable Input Functions:**
  - **Single-Ended**
  - **Single-Ended With Analog Clamp**
  - **Single-Ended With Programmable Digital Clamp**
  - **Differential**
- **Built-In Programmable Gain Amplifier (PGA)**
- **Differential Nonlinearity: ±0.3 LSB**
- **Signal-to-Noise: 56 dB**
- **Spurious Free Dynamic Range: 60 dB**
- **Adjustable Internal Voltage Reference**
- **Straight Binary/2s Complement Output**
- **Out-of-Range Indicator**
- **Power-Down Mode**

28-PIN TSSOP/SOIC PACKAGE
(TOP VIEW)



description

The THS1031 is a CMOS, low-power, 10-bit, 30 MSPS analog-to-digital converter (ADC) that can operate with a supply range from 3 V to 5.5 V. The THS1031 has been designed to give circuit developers flexibility. The analog input to the THS1031 can be either single-ended or differential. This device has a built-in clamp amplifier whose clamp input level can be driven from an external dc source or from an internal high-precision 10-bit digital clamp level programmable via an internal CLAMP register. A 3-bit PGA is included to maintain SNR for small signals. The THS1031 provides a wide selection of voltage references to match the user's design requirements. For more design flexibility, the internal reference can be bypassed to use an external reference to suit the dc accuracy and temperature drift requirements of the application. The out-of-range output indicates any out-of-range condition in THS1031's input signal. The format of digital output can be coded in either unsigned binary or 2s complement.

The speed, resolution, and single-supply operation of the THS1031 are suited to applications in set-top-box (STB), video, multimedia, imaging, high-speed acquisition, and communications. The built-in clamp function allows dc restoration of video signal and is suitable for video applications. The speed and resolution ideally suit charge-couple device (CCD) input systems such as color scanners, digital copiers, digital cameras, and camcorders. A wide input voltage range between REFBS and REFTS allows the THS1031 to be applied in both imaging and communications systems.

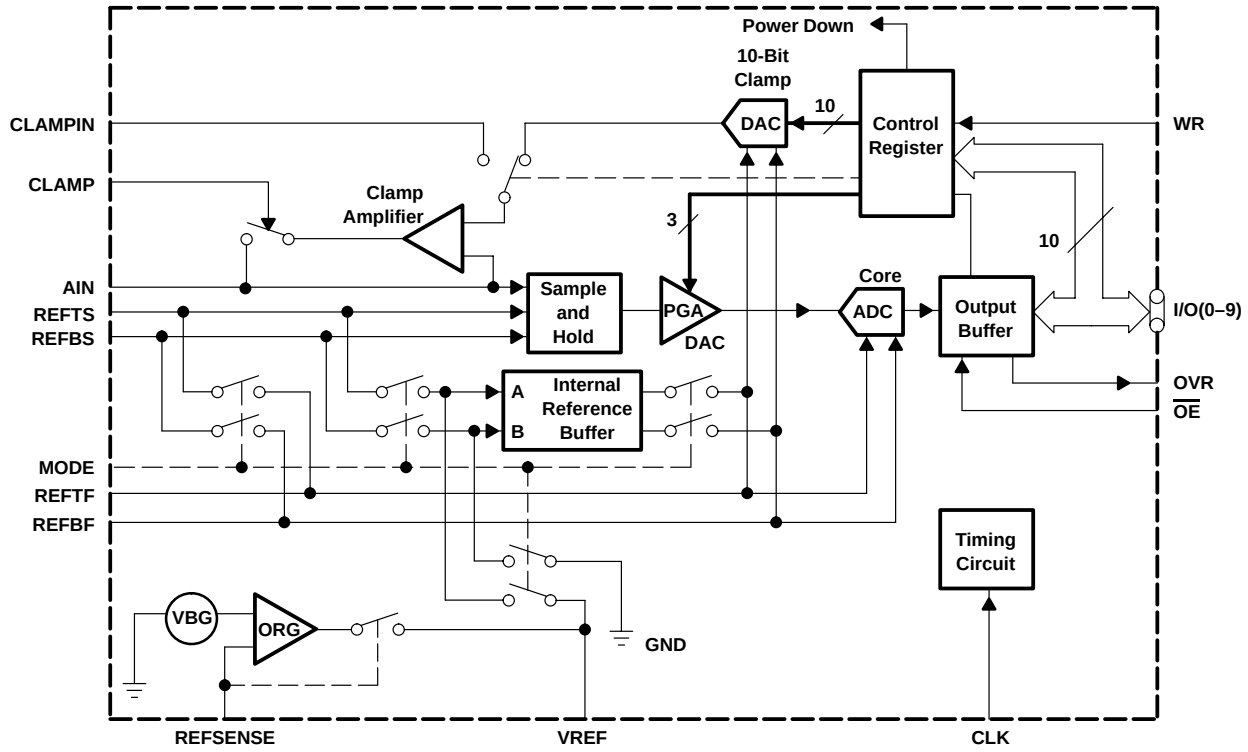
The THS1031C is characterized for operation from 0°C to 70°C, while the THS1031I is characterized for operation from –40°C to 85°C.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES	
	28-TSSOP (PW)	28-SOIC (DW)
0°C to 70°C	THS1031CPW	THS1031CDW
–40°C to 85°C	THS1031IPW	THS1031IDW

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	1	I	Analog ground
AIN	27	I	Analog input
AV_{DD}	28	I	Analog supply
CLAMP	19	I	High to enable clamp mode, low to disable clamp mode
CLAMPIN	20	I	Connect to an external analog clamp reference input.
CLK	15	I	Clock input
DGND	14	I	Digital ground
DV_{DD}	2	I	Digital driver supply
I/O0	3	I/O	Digital I/O bit 0 (LSB)
I/O1	4		Digital I/O bit 1
I/O2	5		Digital I/O bit 2
I/O3	6		Digital I/O bit 3
I/O4	7		Digital I/O bit 4
I/O5	8		Digital I/O bit 5
I/O6	9		Digital I/O bit 6
I/O7	10		Digital I/O bit 7
I/O8	11		Digital I/O bit 8
I/O9	12		Digital I/O bit 9 (MSB)
MODE	23	I	Mode input
$\overline{OE}$	16	I	High to 3-state the data bus, low to enable the data bus
OVR	13	O	Out-of-range indicator
REFBS	25	I	Reference bottom sense
REFBF	24	I	Reference bottom decoupling
REFSENSE	18	I	Reference sense
REFTF	22	I	Reference top decoupling
REFTS	21	I	Reference top sense
VREF	26	I/O	Internal and external reference
WR	17	I	Write strobe

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range: AV_{DD} to AGND, DV_{DD} to DGND . . . . . –0.3 V to 6.5 V
AGND to DGND . . . . . –0.3 V to 0.3 V
AV_{DD} to DV_{DD} . . . . . –6.5 V to 6.5 V
Mode input voltage range, MODE to AGND . . . . . –0.3 V to AV_{DD} + 0.3 V
Reference voltage input range, REFTF, REFTB, REFTS, REFBS to AGND . . . . . –0.3 V to AV_{DD} + 0.3 V
Analog input voltage range, AIN to AGND . . . . . –0.3 V to AV_{DD} + 0.3 V
Reference input voltage range, VREF to AGND . . . . . –0.3 V to AV_{DD} + 0.3 V
Reference output voltage range, VREF to AGND . . . . . –0.3 V to AV_{DD} + 0.3 V
Clock input voltage range, CLK to AGND . . . . . –0.3 V to AV_{DD} + 0.3 V
Digital input voltage range, digital input to DGND . . . . . –0.3 V to DV_{DD} + 0.3 V
Digital output voltage range, digital output to DGND . . . . . –0.3 V to DV_{DD} + 0.3 V
Operating junction temperature range, T_J . . . . . 0°C to 150°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 in) from case for 10 seconds . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

digital inputs

		MIN	NOM	MAX	UNIT
High-level input voltage, V_{IH}	Clock input	$0.8 \times AV_{DD}$			V
	All other inputs	$0.8 \times DV_{DD}$			
Low-level input voltage, V_{IL}	Clock input			$0.2 \times AV_{DD}$	V
	All other inputs			$0.2 \times DV_{DD}$	

analog inputs

	MIN	NOM	MAX	UNIT
Analog input voltage, $V_{I(AIN)}$ (PGA = 1x, top, bottom, or external reference mode)	REFBS		REFTS	V
Reference input voltage, $V_{I(VREF)}$	1		2	V
Clamp input voltage, $V_{I(CLAMPIN)}$	0.1		AV_{DD}–0.1	V

power supply

			MIN	NOM	MAX	UNIT
Supply voltage	Maximum sampling rate = 30 MSPS	AV_{DD}	3	3.3	5.5	V
		DV_{DD}	3	3.3	5.5	

REFTS, REFBS reference voltages (MODE = AV_{DD})

PARAMETER		MIN	NOM	MAX	UNIT
REFTS	Reference input voltage (top)	1		AV_{DD}	V
REFBS	Reference input voltage (bottom)	0		AV_{DD}–1	V
	Differential input voltage (REFTS – REFBS)	1		2	V
	Switched input capacitance on REFTS or REFBS		0.6		pF

sampling rate and resolution

PARAMETER		MIN	NOM	MAX	UNIT
f_S	Sample frequency	5		30	MHz
	Resolution		10		Bits

electrical characteristics over recommended operating conditions, AV_{DD} = 3 V, DV_{DD} = 3 V, f_S = 30 MSPS/50% duty cycle, MODE = AV_{DD}, 2-V input span from 0.5 V to 2.5 V, external reference, PGA = 1X, $T_A = T_{min}$ to T_{max} (unless otherwise noted)

analog inputs

PARAMETER		MIN	TYP	MAX	UNIT
$V_{I(AIN)}$	Analog input voltage	REFBS		REFTS	V
C_I	Switched sampling input capacitance		1.2		pF
BW	Full power bandwidth (–3 dB)		150		MHz
I_{lkg}	DC leakage current (input = ± FS)		100		µA

VREF reference voltages

PARAMETER	MIN	TYP	MAX	UNIT
Internal 1-V reference voltage (REFSENSE = VREF)	0.95	1	1.05	V
Internal 2-V reference voltage (REFSENSE = AV_{SS})	1.90	2	2.10	V
External reference voltage (REFSENSE = AV_{DD})	1		2	V
Reference input resistance (REFSENSE = AV_{DD}, MODE = AV_{DD}/2)		18		kΩ

REFTF, REFBF reference voltages

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Differential input voltage (REFTF – REFBF)			1		2	V
Input common mode voltage (REFTF + REFBF)/2		AV_{DD} = 3 V	1.3	1.5	1.7	V
		AV_{DD} = 5 V	2	2.5	3	
REFTF voltage (MODE = AV_{DD})	VREF = 1 V	AV_{DD} = 3 V		2		V
		AV_{DD} = 5 V		3		
	VREF = 2 V	AV_{DD} = 3 V		2.5		V
		AV_{DD} = 5 V		3.5		
REFBF voltage (MODE = AV_{DD})	VREF = 1 V	AV_{DD} = 3 V		1		V
		AV_{DD} = 5 V		2		
	VREF = 2 V	AV_{DD} = 3 V		0.5		V
		AV_{DD} = 5 V		1.5		
Input resistance between REFTF and REFBF				680		Ω

electrical characteristics over recommended operating conditions, AV_{DD} = 3 V, DV_{DD} = 3 V, f_S = 30 MSPS/50% duty cycle, MODE = AV_{DD}, 2-V input span from 0.5 V to 2.5 V, external reference, PGA = 1X, $T_A = T_{min}$ to T_{max} (unless otherwise noted) (continued)

dc accuracy

PARAMETER		MIN	TYP	MAX	UNIT
INL	Integral nonlinearity (see Note 1)		±1	±2	LSB
DNL	Differential nonlinearity (see Note 2)		±0.3	±1	LSB
	Offset error (see Note 3)		0.4	2	%FSR
	Gain error (see Note 4)		1.4	3.5	%FSR
	Missing code	No missing code assured			

NOTES: 1. Integral nonlinearity refers to the deviation of each individual code from a line drawn from zero to full scale. The point used as zero occurs 1/2 LSB before the first code transition. The full-scale point is defined as a level 1/2 LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line between these two endpoints.

2. An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Therefore this measure indicates how uniform the transfer function step sizes are. The ideal step size is defined here as the step size for the device under test (i.e., (last transition level – first transition level) ÷ (2^n – 2)). Using this definition for DNL separates the effects of gain and offset error. A minimum DNL better than –1 LSB ensures no missing codes.

3. Offset error is defined as the difference in analog input voltage – between the ideal voltage and the actual voltage – that will switch the ADC output from code 0 to code 1. The ideal voltage level is determined by adding the voltage corresponding to 1/2 LSB to the bottom reference level. The voltage corresponding to 1 LSB is found from the difference of top and bottom references divided by the number of ADC output levels (1024).

4. Gain error is defined as the difference in analog input voltage – between the ideal voltage and the actual voltage – that will switch the ADC output from code 1022 to code 1023. The ideal voltage level is determined by subtracting the voltage corresponding to 1.5 LSB from the top reference level. The voltage corresponding to 1 LSB is found from the difference of top and bottom references divided by the number of ADC output levels (1024).

dynamic performance (ADC and PGA)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ENOB	Effective number of bits	f = 3.5 MHz	8.2	9		Bits
		f = 3.5 MHz, AV_{DD} = 5 V		8.8		
		f = 15 MHz		7.7		
		f = 15 MHz, AV_{DD} = 5 V		7.64		
SFDR	Spurious free dynamic range	f = 3.5 MHz	55	60		dB
		f = 3.5 MHz, AV_{DD} = 5 V		63		
		f = 15 MHz		48		
		f = 15 MHz, AV_{DD} = 5 V		52.4		
THD	Total harmonic distortion	f = 3.5 MHz		–58.2	–54.7	dB
		f = 3.5 MHz, AV_{DD} = 5 V		–68.7		
		f = 15 MHz		–47		
		f = 15 MHz, AV_{DD} = 5 V		–51.9		
SNR	Signal-to-noise ratio	f = 3.5 MHz	51.2	56		dB
		f = 3.5 MHz, AV_{DD} = 5 V		55		
		f = 15 MHz		53		
		f = 15 MHz, AV_{DD} = 5 V		49.3		
SINAD	Signal-to-noise and distortion	f = 3.5 MHz	51.1	56		dB
		f = 3.5 MHz, AV_{DD} = 5 V		55		
		f = 15 MHz		48.1		
		f = 15 MHz, AV_{DD} = 5 V		47.7		

electrical characteristics over recommended operating conditions, AV_{DD} = 3 V, DV_{DD} = 3 V, f_S = 30 MSPS/50% duty cycle, MODE = AV_{DD}, 2-V input span from 0.5 V to 2.5 V, external reference, PGA = 1X, $T_A = T_{min}$ to T_{max} (unless otherwise noted) (continued)

PGA

PARAMETER	MIN	TYP	MAX	UNIT
Gain range (linear scale)	0.5		4	V/V
Gain step size (linear scale)		0.5		V/V
Gain error from nominal			3%	
Number of control bits		3		Bits

clamp amplifier and clamp DAC

PARAMETER	MIN	TYP	MAX	UNIT
Resolution		10		Bits
DAC output range	REFBF		REFTF	V
DAC differential nonlinearity	–1		1	LSB
DAC integral nonlinearity		±1		LSB
Clamping analog output voltage range	0.1		AV_{DD}–0.1	V
Clamping analog output voltage error	–40		40	mV

clock

PARAMETER		MIN	TYP	MAX	UNIT
t_c	Clock cycle	33			ns
$t_{w(CKH)}$	Pulse duration, clock high	15	16.5		ns
$t_{w(CKL)}$	Pulse duration, clock high	15	16.5		ns
$t_{d(o)}$	Clock to data valid, delay time			25	ns
	Pipeline latency		3		Cycles
$t_{d(AP)}$	Aperture delay time		4		ns
	Aperture uncertainty (jitter)		2		ps

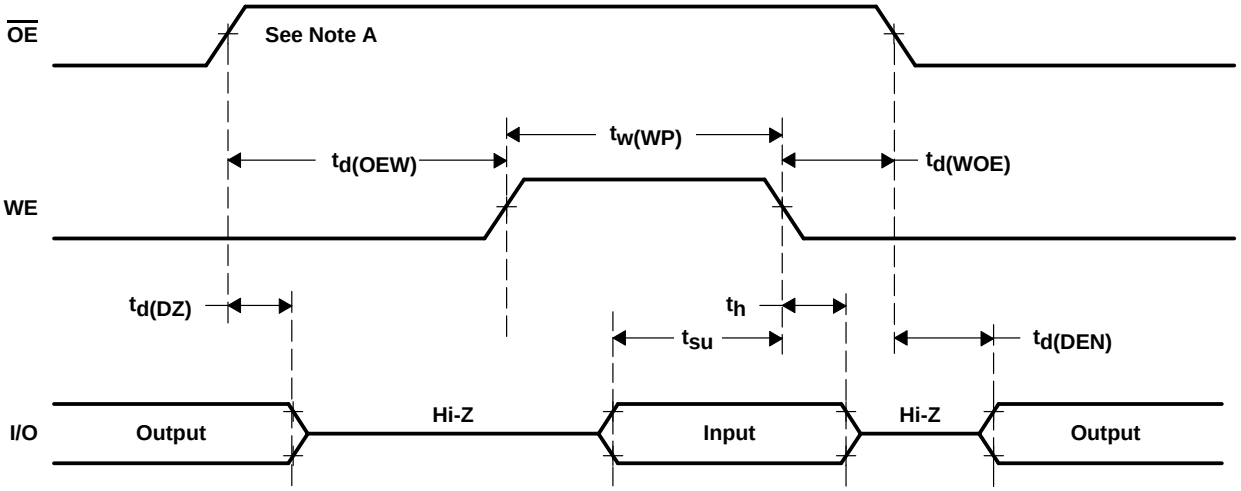
timing

PARAMETER		MIN	TYP	MAX	UNIT
$t_{d(DZ)}$	Output disable to Hi-Z output, delay time	0		20	ns
$t_{d(DEN)}$	Output enable to output valid, delay time	0		20	ns
$t_{d(OEW)}$	Output disable to write enable, delay time	12			ns
$t_{d(WOE)}$	Write disable to output enable, delay time	12			ns
$t_{w(WP)}$	Write pulse duration	15			ns
t_{su}	Input data setup time	5			ns
t_h	Input data hold time	5			ns

power supply

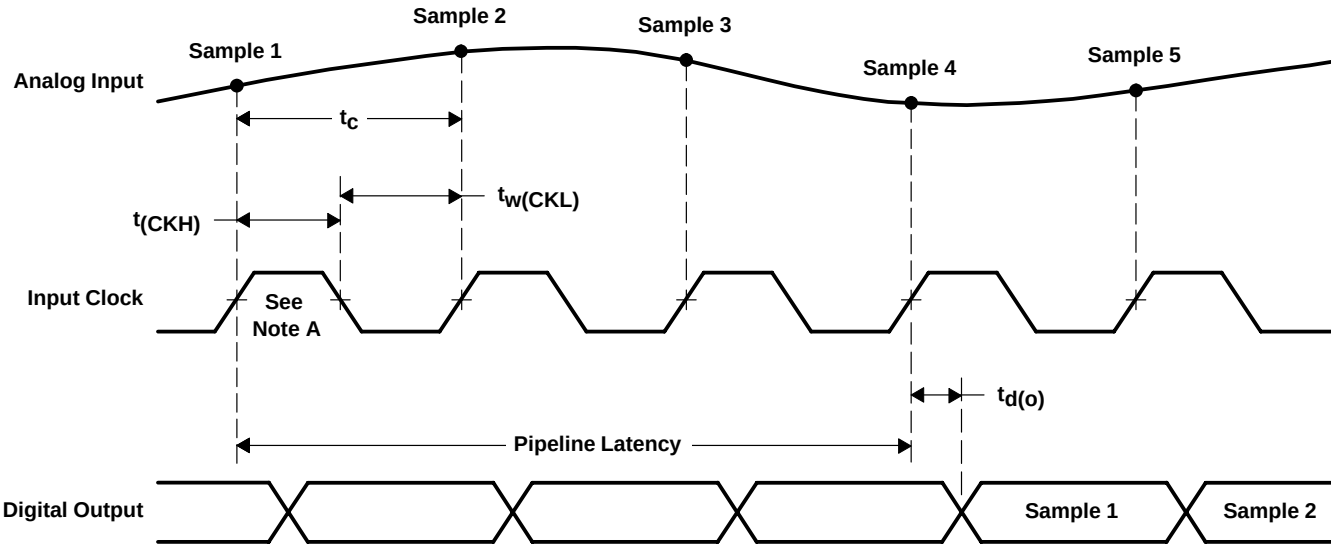
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Operating supply current	AV_{DD} = 3 V, MODE = AGND		30.6	45	mA
P_D	Power dissipation	$AV_{DD} = DV_{DD}$ = 3 V		94	135	mW
		$AV_{DD} = DV_{DD}$ = 5 V		160		
$P_{D(STBY)}$	Standby power	$AV_{DD} = DV_{DD}$ = 3 V, MODE = AGND		3	5	mW

PARAMETER MEASUREMENT INFORMATION



NOTE A: All timing measurements are based on 50% of edge transition.

Figure 1. Write Timing Diagram



NOTE A: All timing measurements are based on 50% of edge transition.

Figure 2. Digital Output Timing Diagram

TYPICAL CHARACTERISTICS

POWER DISSIPATION vs SAMPLING FREQUENCY

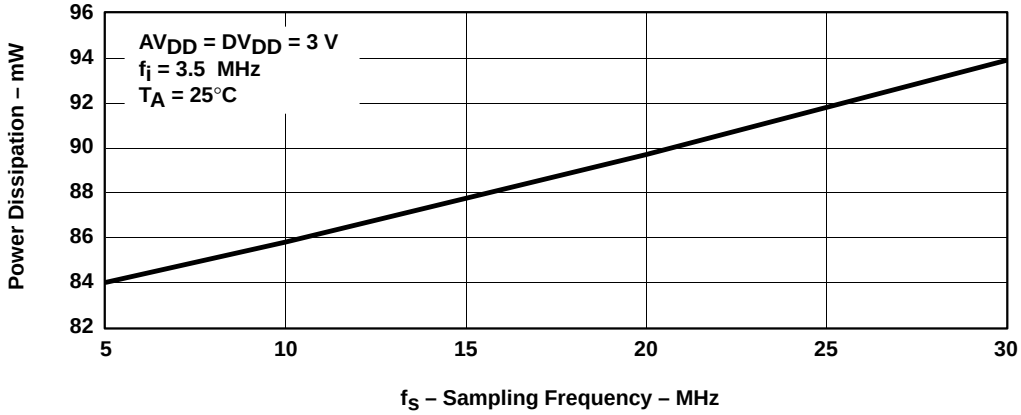


Figure 3

EFFECTIVE NUMBER OF BITS vs TEMPERATURE

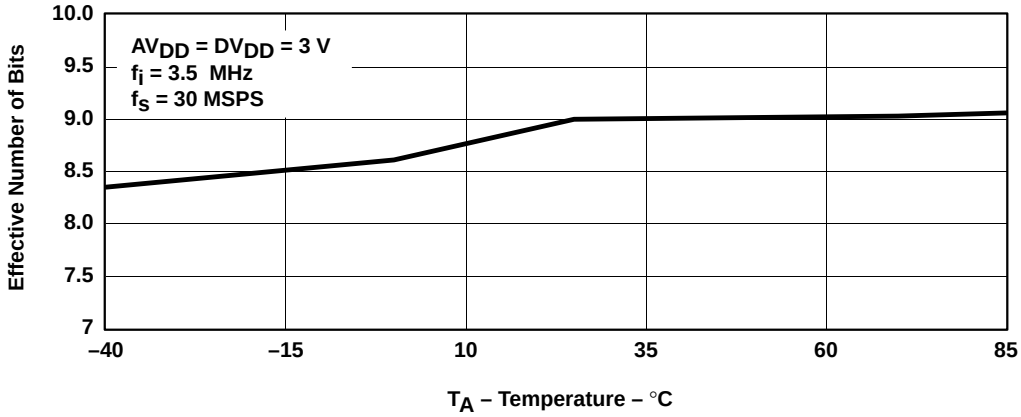


Figure 4

TYPICAL CHARACTERISTICS

EFFECTIVE NUMBER OF BITS vs SAMPLING FREQUENCY

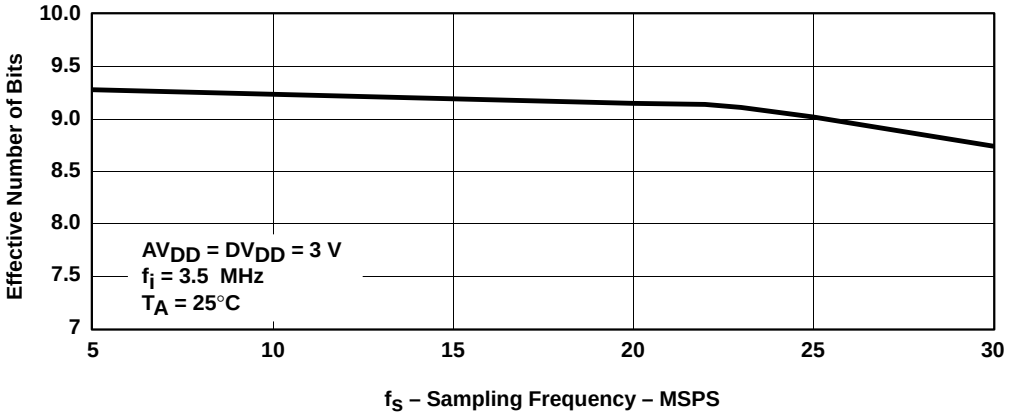


Figure 5

EFFECTIVE NUMBER OF BITS vs SAMPLING FREQUENCY

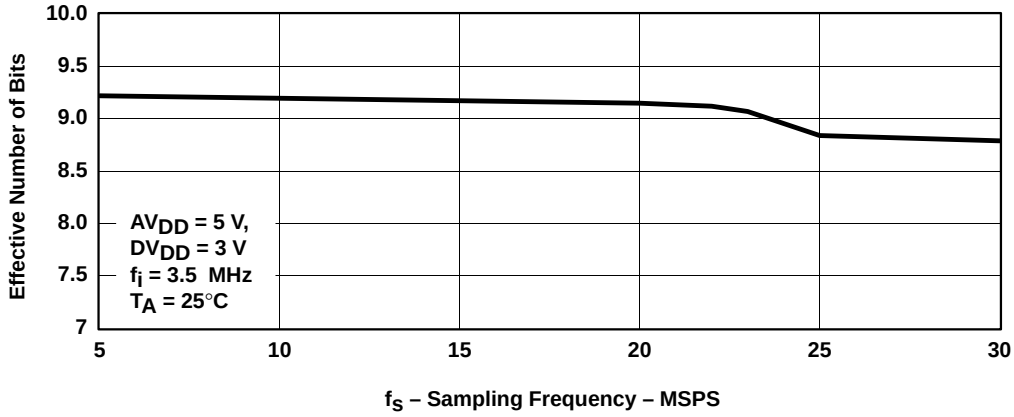


Figure 6

TYPICAL CHARACTERISTICS

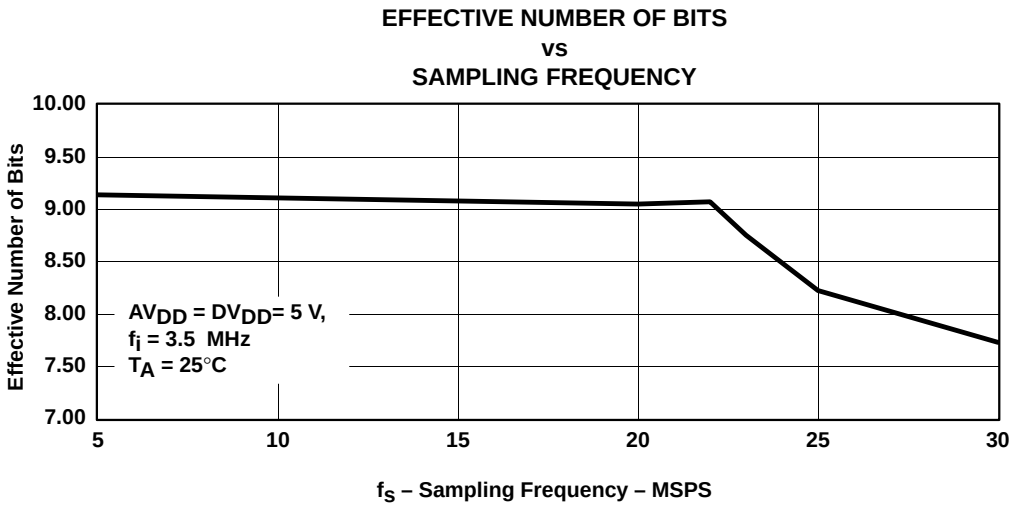


Figure 7

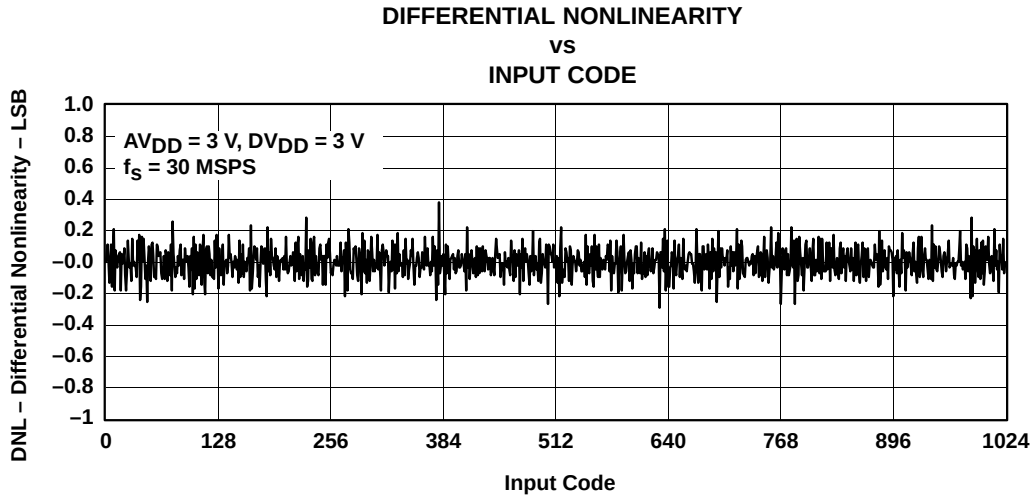


Figure 8

TYPICAL CHARACTERISTICS

INTEGRAL NONLINEARITY vs INPUT CODE

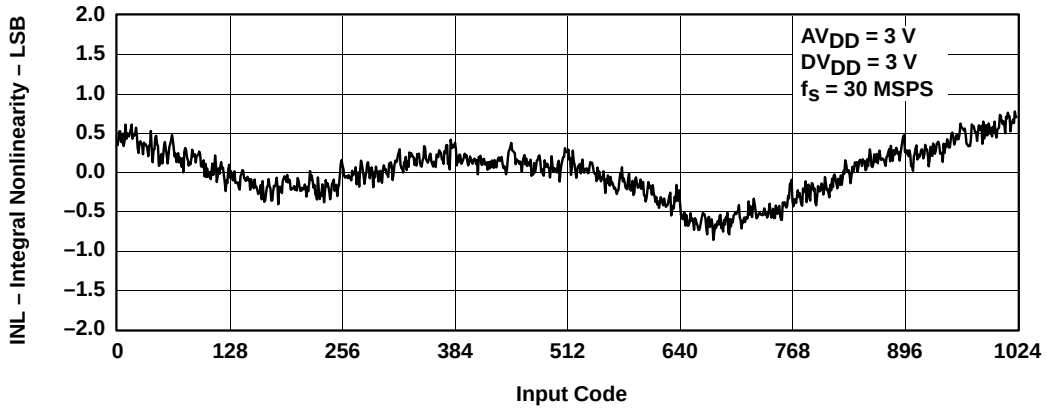


Figure 9

FFT vs FREQUENCY

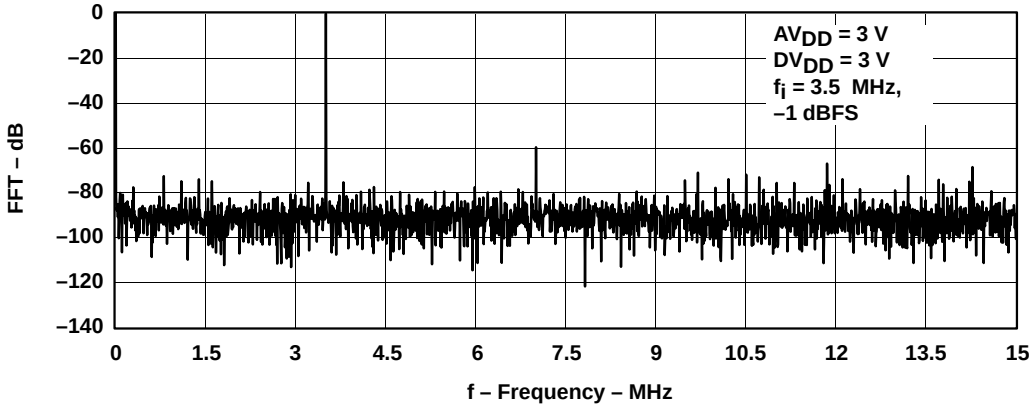


Figure 10

PRINCIPLES OF OPERATION

The analog input AIN is sampled in the sample-and-hold unit**,** the output of which goes to a programmable gain amplifier (PGA). The PGA feeds the ADC core, where the process of analog to digital conversion is performed against ADC reference voltages, REFTF and REFBF.

Connecting the MODE pin to one of three voltages, AGND, AV_{DD} or $AV_{DD}/2$ sets up operating configurations. The three settings open or close internal switches to select one of the three basic methods of ADC reference generation.

Depending on the user's choice of operating configuration, the ADC reference voltages may come from the internal reference buffer (IRB) or may be fed from completely external sources. Where the reference buffer is employed, the user can choose to drive it from the onboard reference generator (ORG), or may use an external voltage source. A specific configuration is selected by connections to the REFSENSE, VREF, REFTS and REFBS, and REFTF and REFBF pins, along with any external voltage sources selected by the user.

The THS1031 offers a clamp function for dc restoration of ac-coupled signals. The clamp voltage may be set digitally via the 10-bit clamp DAC or by the analog level applied to the CLAMPIN input.

The ADC core drives out through output buffers to the I/O pins I/O0 to I/O9. The output buffers can be disabled by the $\overline{OE}$ pin. Control input data on I/O0 to I/O9 can then be written, by pulses on WR, to the control registers. These registers control clamp operation, output format (unsigned binary or twos complement), the PGA gain setting and the device power down function.

A single-ended, sample-rate clock (30 MHz maximum) is required at pin CLK. The analog input signal is sampled on the rising edge of CLK, and corresponding data is output after the following third rising edge.

The user-chosen operating configuration and reference voltages determine what input signal voltage range the THS1031 can handle.

The following sections explain:

- The internal signal flow of the device, and how the input signal span is related to the ADC reference voltages;
- The ways in which the ADC reference voltages can be buffered internally, or externally applied;
- How to set the onboard reference generator output, if required, and several examples of complete configurations.
- Subsequent sections explain the clamp function and digital controls, followed by more detailed application information.

signal processing chain (sample and hold, PGA, ADC)

Figure 11 shows the signal flow through the sample and hold unit and the PGA to the ADC core.

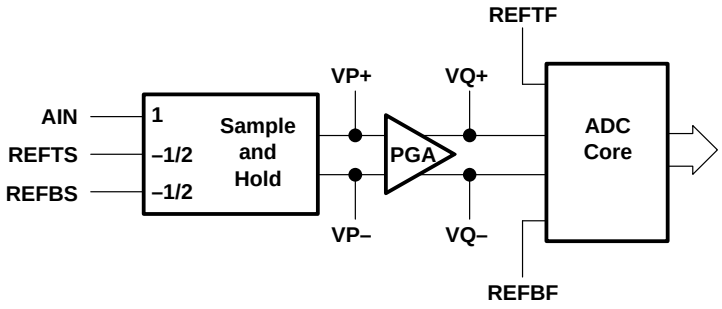


Figure 11. Analog Input Signal Flow

PRINCIPLES OF OPERATION

sample-and-hold

The analog input signal A_{IN} is applied to the AIN pin, either dc-coupled, ac-coupled, or ac-coupled with dc restoration using the THS1031 clamp circuit.

The differential sample and hold processes A_{IN} with respect to the voltages applied to the REFTS and REFBS pins, to give a differential output VP+ – VP– = VP given by:

$$VP = A_{IN} - VM \tag{1}$$

Where:

$$VM = \frac{(REFTS + REFBS)}{2} \tag{2}$$

For single-ended input signals, VM is a constant voltage; usually the AIN mid-scale input voltage. However if MODE = $AV_{DD}/2$ then REFTS and REFBS can be connected together to operate with AIN as a complementary pair of differential inputs (see Figures 15 and 16).

programmable gain amplifier

VP is amplified by the PGA and fed into the ADC as a differential voltage $VQ^+ - VQ^- = VQ$

$$VQ = Gain \times VP = Gain \times [A_{IN} - VM]$$

The default PGA gain at power up is 1, but can be programmed from 0.5 to 4.0 via the control register.

analog-to-digital converter

In all operating configurations, VQ is digitized against ADC reference voltages REFTF and REFBF, full-scale values of VQ being given by

$$VQFS + = \frac{+ (REFTF - REFBF)}{2} \tag{3}$$

$$VQFS - = \frac{- (REFTF - REFBF)}{2}$$

VQ voltages outside the range VQFS– to VQFS+ lie outside the conversion range of the ADC. Attempts to convert out-of-range inputs are signalled to the application by driving the OVR output pin high. VQ voltages less than VQFS– give ADC output code 0. VQ voltages greater than VQFS+ give output code 1023.

complete system

Combining equations 1 to 3, the analog full-scale input voltages at AIN which give VQFS+ and VQFS– at the PGA output are:

$$A_{IN} = FS + = VM + \frac{(REFTF - REFBF)}{(2 \times Gain)} \tag{4}$$

and

$$A_{IN} = FS - = VM - \frac{(REFTF - REFBF)}{(2 \times Gain)} \tag{5}$$

The analog input span (voltage range) that lies within the ADC conversion range is:

$$Input\ span = [(FS +) - (FS -)] = (REFTF - REFBF)/\ Gain \tag{6}$$

PRINCIPLES OF OPERATION

complete system (continued)

The REFTF and REFBF voltage difference and the gain sets the device input range. The next sections describe in detail the various methods available for setting voltages REFTF and REFBF to obtain the desired input span and device performance.

ADC reference generation

The THS1031 has three primary modes of ADC reference generation, selected by the voltage level applied to the MODE pin.

Connecting the MODE pin to AGND gives full external reference mode. In this mode, the user supplies the ADC reference voltages directly to pins REFTF and REFBF. This mode is used where there is need for minimum power drain or where there are very tight tolerances on the ADC reference voltages. This mode also offers the possibility of Kelvin connection of the reference inputs to the THS1031 to eliminate any voltage drops from remote references that may occur in the system. Only single-ended input is possible in this mode.

Connecting the MODE pin to $AV_{DD}/2$ gives differential mode. In this mode, the ADC reference voltages REFTF and REFBF are generated by the internal reference buffer from the voltage applied to the VREF pin. This mode is suitable for handling differentially presented inputs, which are applied to the AIN and REFTS/REFBS pins. A special case of differential mode is center span mode, in which user applies a single-ended signal to AIN and applies the mid-scale input voltage (VM) to the REFTS and REFBS pins.

Connecting the MODE pin to AV_{DD} gives top/bottom mode. In this mode, the ADC reference voltages REFTF and REFBF are generated by the internal reference buffer from the voltages applied to the REFTS and REFBS pins. Only single-ended input is possible in top/bottom mode.

Table 1. Typical Set of Reference Connections

REFERENCE MODE	MODE	REFSENSE	VREF VOLTAGE	REFTS, REFBS	ANALOG INPUT	FIGURES
External	AV_{SS}	AV_{DD}	Disabled	Reference buffer powered down, reference voltage provided directly by REFTS and REFBS	Single-ended	12, 13, 14
Internal	$AV_{DD}/2$	VREF	1 V	Externally connect REFTS to REFBS. This pair then forms AIN– to the ADC.	Differential or center span	15, 16, 17
		AGND	2 V			
		External divider	1 + Ra/Rb (see Figure 22)			
External (through internal reference buffer)	AV_{DD}	AV_{DD}	Disabled	$REFTS = V_{MID} + (V_{FS+} - V_{FS-}) \times Gain/2$ $REFBS = V_{MID} - (V_{FS+} - V_{FS-}) \times Gain/2$	Single-ended (top-bottom mode)	18, 19
Output of VREF can be externally tied to REFTS or REFBS to provide one of the reference voltages		VREF	1 V			
		AGND	2 V			
		External divider	1 + Ra/Rb (see Figure 22)			

PRINCIPLES OF OPERATION

full external reference mode (mode = AGND)

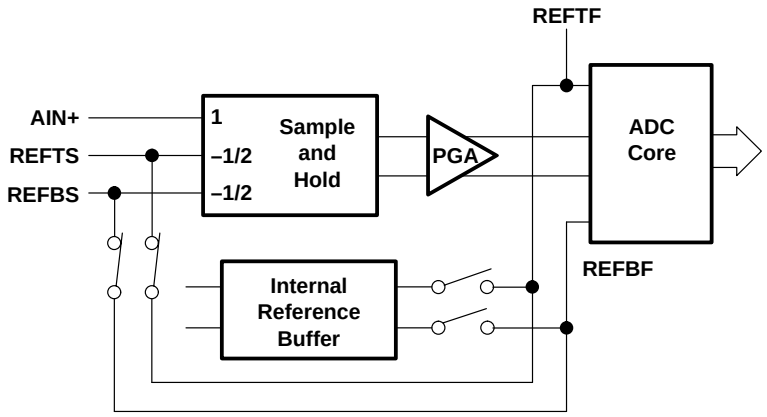


Figure 12. ADC Reference Generation, MODE = AGND

When MODE is connected to AGND, the internal reference buffer is powered down, its inputs and outputs disconnected, and REFTS and REFBS internally connected to REFTF and REFBF respectively. These nodes are connected by the user to external sources to provide the ADC reference voltages. The internal connections are designed for use in kelvin connection mode (Figure 14). When using external reference mode as shown in Figure 13, REFTS must be shorted to REFTF and REFBS must be shorted to REFBF externally. The mean of REFTF and REFBF must be equal to $AV_{DD}/2$ (see Figure 13).

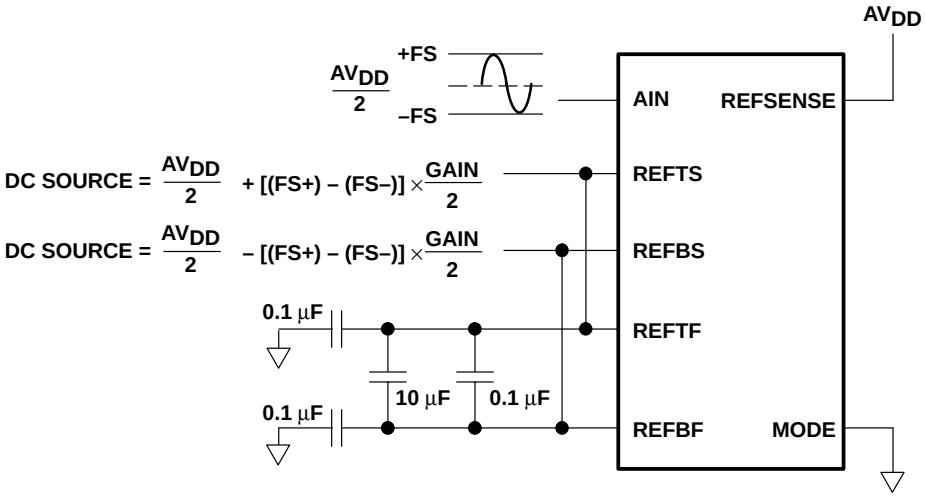


Figure 13. Full External Reference Mode

It is also possible to use REFTS and REFBS as sense lines to drive the REFTF and REFBF lines (Kelvin mode) to overcome any voltage drops within the system (see Figure 14).

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full external reference mode (mode = AGND) (continued)

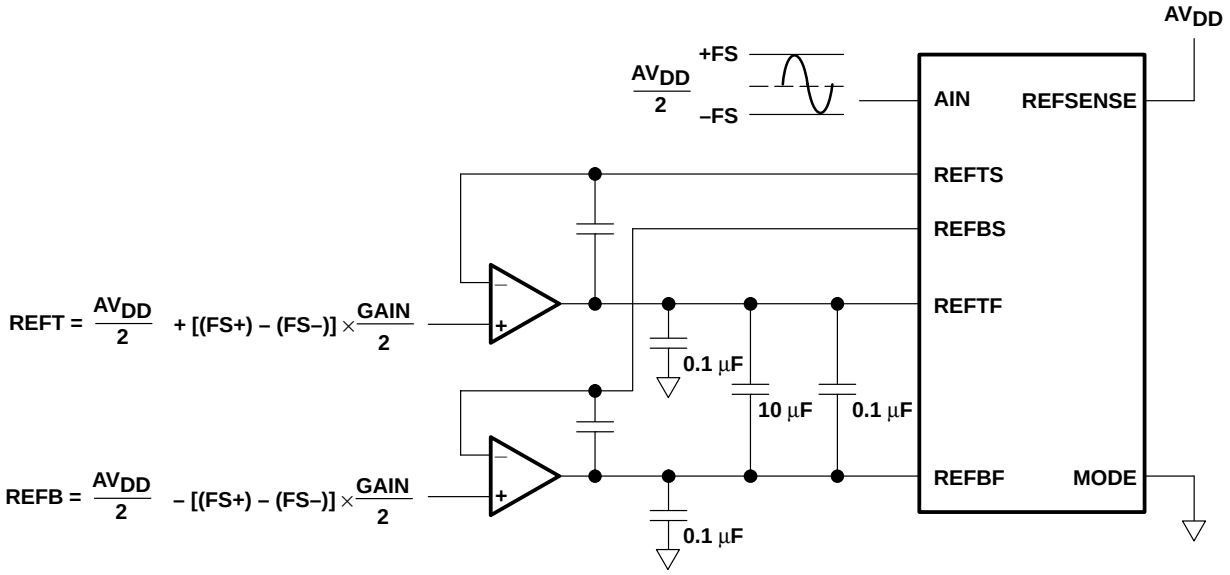

Figure 14. Full External Reference With Kelvin Connections

differential mode (mode = $AV_{DD}/2$)

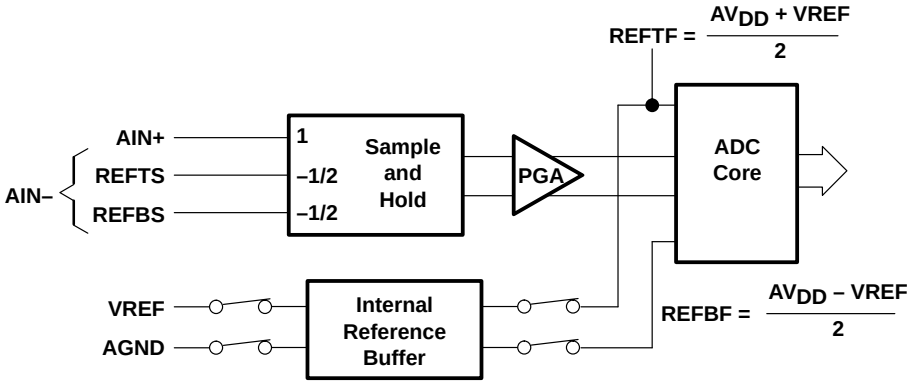

Figure 15. ADC Reference Generation, MODE = $AV_{DD}/2$

When MODE = $AV_{DD}/2$, the internal reference buffer is enabled, its outputs internally switched to REFTF and REFBF and inputs internally switched to VREF and AGND as shown in Figure 15. The REFTF and REFBF voltages are centered on $AV_{DD}/2$ by the internal reference buffer and the voltage difference between REFTF and REFBF equals the voltage at VREF. The internal REFTS to REFBS and REFTF to REFBF switches are open in this mode, allowing REFTS and REFBS to form the AIN– to the sample and hold.

Depending on the connection of the REFSENSE pin, the voltage on VREF may be externally driven, or set to an internally generated voltage of 1 V, 2 V, or an intermediate voltage (see the onboard reference generator configuration).

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differential mode (mode = $AV_{DD}/2$) (continued)

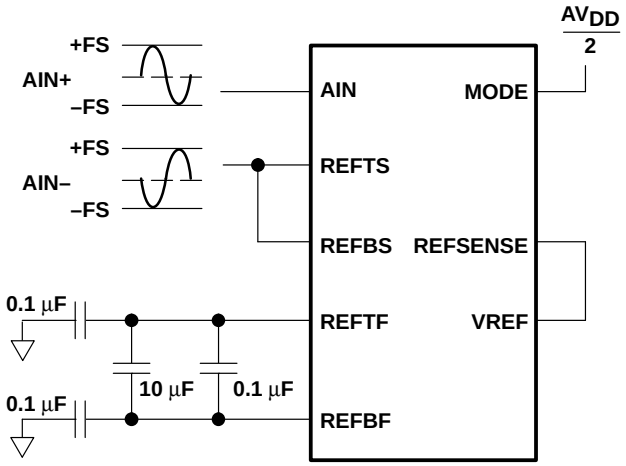

Figure 16. Differential Input Mode, 1-V Reference Span

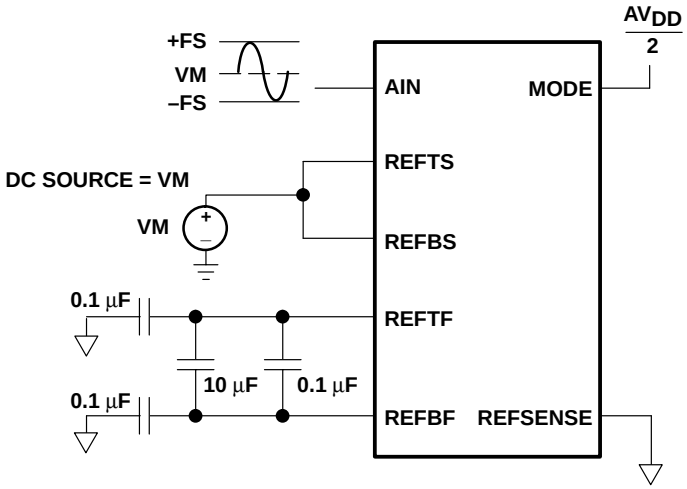

Figure 17. Center Span Mode, 2-V Reference Span

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top/bottom mode (MODE = AV_{DD})

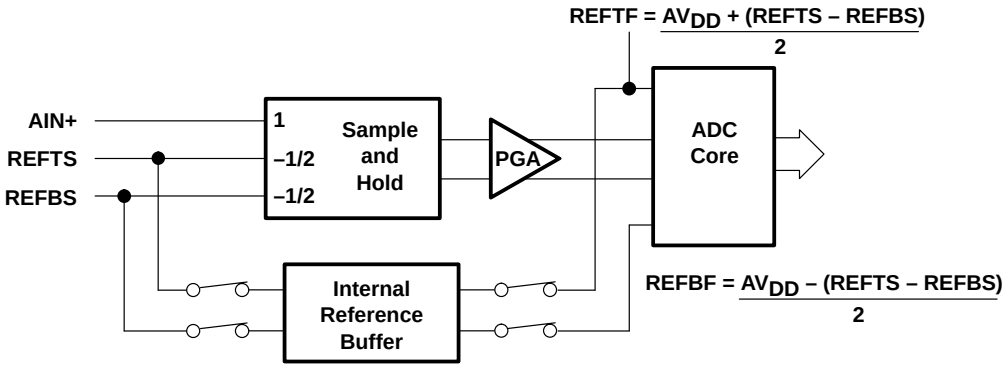

Figure 18. ADC Reference Generation Mode = AV_{DD}

Connecting MODE to AV_{DD} enables the internal reference buffer. Its inputs are internally switched to the REFTS and REFBS pins and its outputs internally switched to pins REFTF and REFBF. The internal connections (REFTS to REFTF) and (REFBS to REFBF) are broken.

To match the signal span to the full ADC input span, the voltage difference between REFTS and REFBS should be REFTS – REFBS = [(FS+) – (FS–)] × Gain, with the average of the REFTS and REFBS voltages being the AIN midscale voltage, VM.

Typically, REFSENSE is tied to AV_{DD} to disable the ORG output to VREF (as in Figure 19), but the user can choose to use the ORG output to VREF as either REFTS or REFBS.

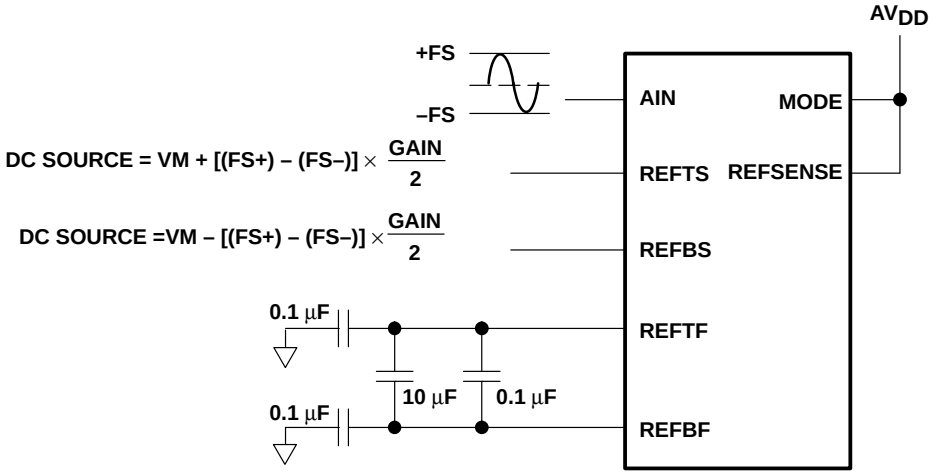

Figure 19. ADC Reference Generation Mode = AV_{DD}

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onboard reference generator configuration

The onboard reference generator (ORG) can supply a supply-voltage-independent and temperature-independent voltage on pin VREF.

External connections to REFSENSE control the ORG's output to the VREF pin as shown in Table 2.

Table 2. Effect of REFSENSE Connection on VREF Value

REFSENSE CONNECTION	ORG OUTPUT TO VREF	REFER TO:
VREF pin	1 V	Figure 20
AGND	2 V	Figure 21
External divider junction	$(1 + R_A/R_B)$	Figure 22
AV_{DD}	Open circuit	Figure 23

REFSENSE = AV_{DD} powers the ORG down, saving power when the ORG function is not required. If MODE = $AV_{DD}/2$, the voltage on VREF determines the ADC reference voltages:

$$\text{REFTF} = \frac{AV_{DD}}{2} + \frac{\text{VREF}}{2} \quad (7)$$

$$\text{REFBF} = \frac{AV_{DD}}{2} - \frac{\text{VREF}}{2}$$

$$\text{REFTF} - \text{REFBF} = \text{VREF}$$

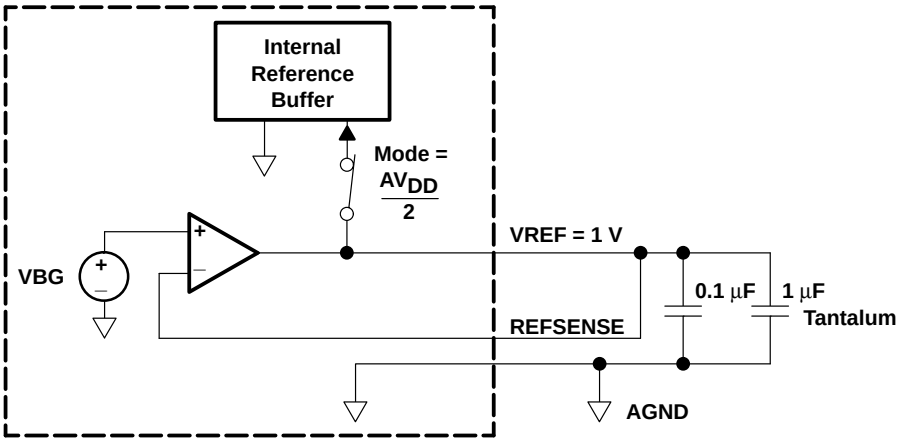

Figure 20. 1-V VREF Using ORG

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onboard reference generator configuration (continued)

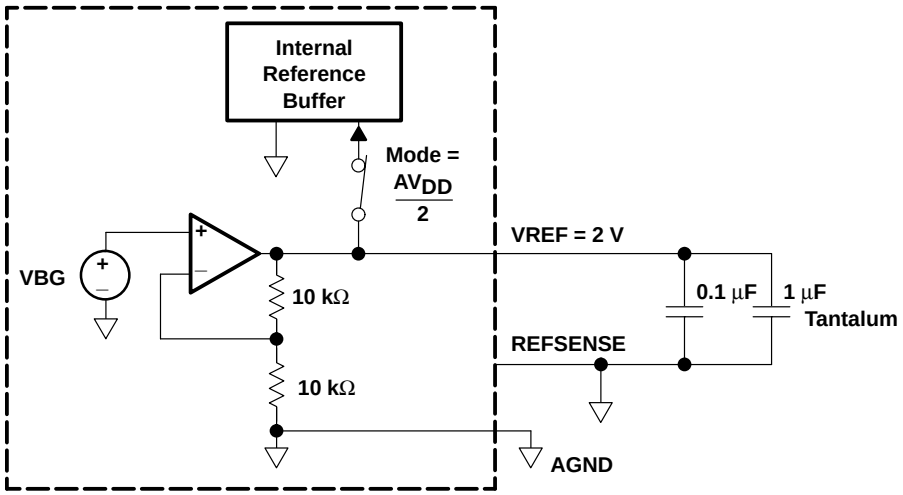

Figure 21. 2-V VREF Using ORG

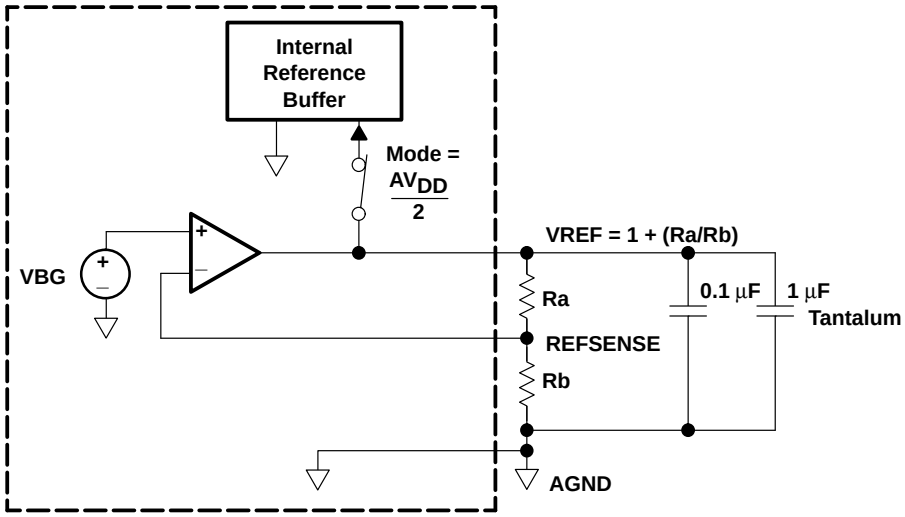

Figure 22. External Divider Mode

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onboard reference generator configuration (continued)

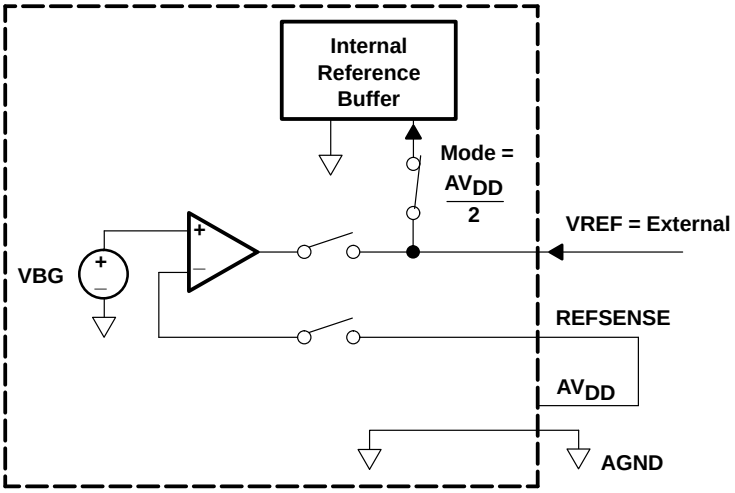

Figure 23. Drive VREF Mode

operating configuration examples

This section provides examples of operating configurations.

Figure 24 shows the operating configuration in top/bottom mode for a 2-V span single-ended input, using VREF to drive REFTS and with PGA gain = 1. Connecting the MODE pin to AV_{DD} puts the THS1031 in top/bottom mode. Connecting pin REFSENSE to AGND sets the output of the ORG to 2 V. REFTS and REFBS are user-connected to VREF and AGND respectively to match the AIN pin input range to the voltage range of the input signal.

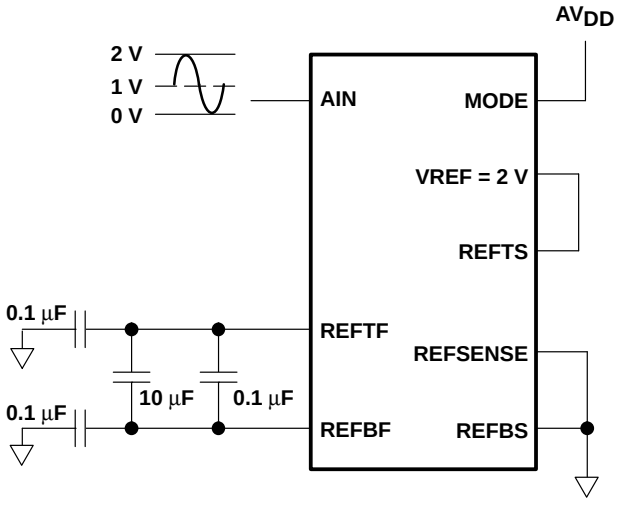

Figure 24. Operation Configuration in Top/Bottom Mode

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operating configuration examples (continued)

In Figure 25, the input signal is differential, so Mode = $AV_{DD}/2$ (differential mode) is set to allow the inverse signal to be applied to REFTS and REFBS. The differential input goes from –0.8 V to 0.8 V, giving a total input signal span of 1.6 V. Using a PGA gain of 1, REFTF–REFBF should therefore, equal 1.6 V. REFSENSE is connected to resistors RA and RB (external divider mode) to make VREF = 1.6 V, that is R_A/R_B = 0.6 (see Figure 22).

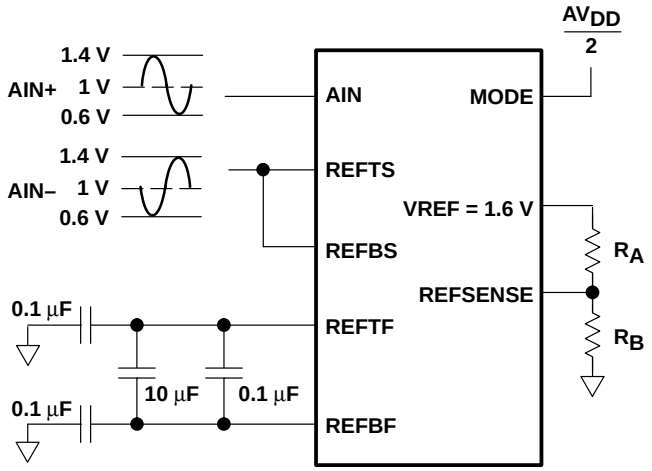

Figure 25. Differential Operation

Figure 26 shows a center span configuration for an input waveform swinging between 0.2 and 1.9 V. Pins REFTS and REFBS are connected to a voltage source of 1.05 V, equal to the mid-scale of the input waveform. With the PGA gain set to its default value of 1, REFTF–REFBF should be set equal to the span of the input waveform, 1.7 V, so VREF is connected to an external source of 1.7 V. REFSENSE must be connected to AV_{DD} to disable the ORG output to VREF (see Figure 23) to allow this external source to be applied.

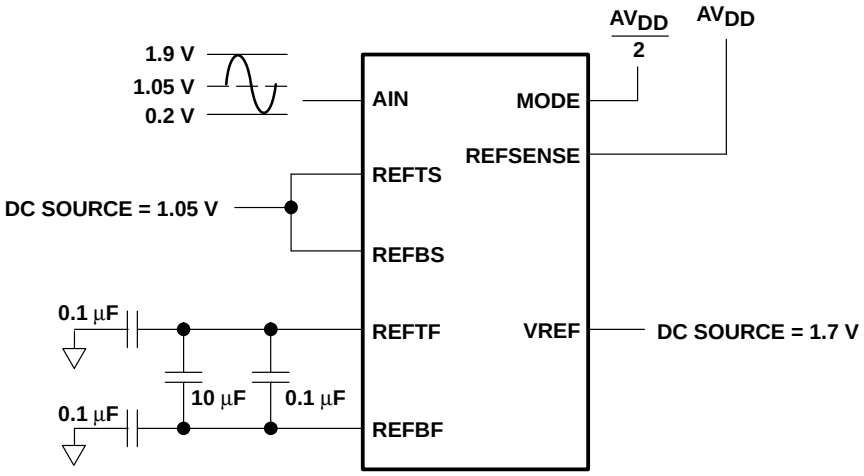

Figure 26. Center Span Operation

PRINCIPLES OF OPERATION

operating configuration examples (continued)

Figure 27 shows an example of top/bottom mode operation on an input span of 800 mV with mid-scale value 1.5 V. Pin REFTS is set to 2.5 V and pin REFBS to 0.5 V, making their average value equal to the mid-scale value of A_{IN} and giving the maximum specified difference of 2 V between REFTS and REFBS to maximize the full-scale range of the ADC core for best resolution. The PGA gain then has to be set to 2.5, to amplify the 800 mV_{PP} input signal to 2 V_{PP} at the ADC core input.

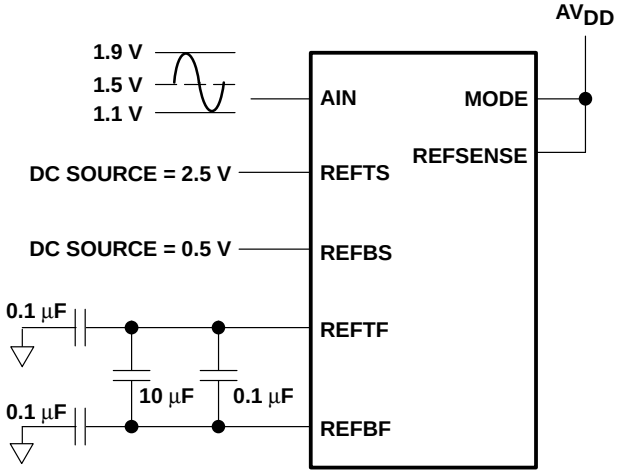

Figure 27. Top/Bottom Mode, PGA Gain 2.5

clamp operation

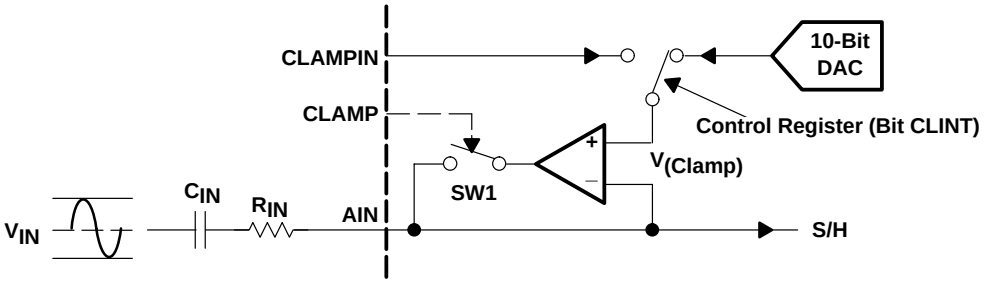

Figure 28. Schematic of Clamp Circuitry

The THS1031 provides a clamp function for restoring a dc reference level to the signal at AIN which has been lost through ac-coupling from the signal source to this pin.

Figure 29 shows an example of using the clamp to restore the black level of a composite video input ac coupled to AIN. While the clamp pin is held high, the clamp amplifier forces the voltage at AIN to equal the clamp reference voltage, setting the dc voltage at AIN for the video black level.

After power up, the clamp reference voltage is the voltage on the CLAMPIN pin. This reference can instead be taken from the internal CLAMP DAC by suitably programming the THS1031 clamp and control registers.

Clamp acquisition and clamp droop design calculations are discussed later.

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clamp operation (continued)

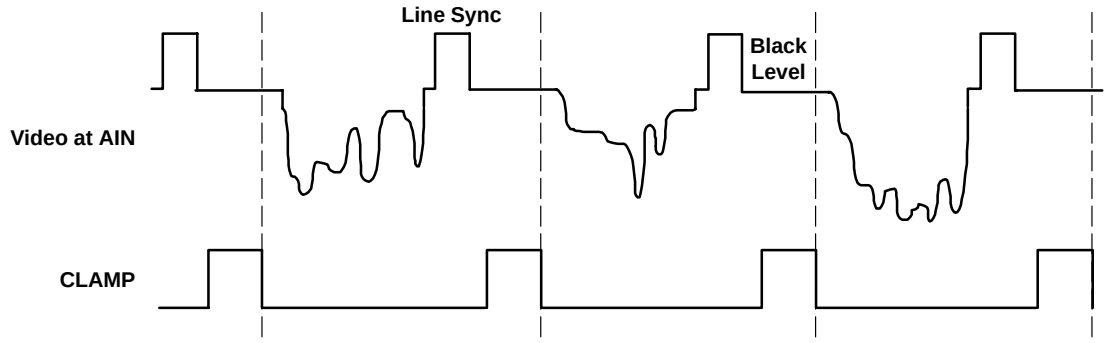

Figure 29. Example Waveforms for Line-Clamping to a Video Input Black Level

clamp DAC output voltage range and limits

When using the internal clamp DAC in top/bottom or center span mode, the user must ensure that the desired dc clamp level at AIN lies within the voltage range V_{REFBF} to V_{REFTF}. This is because the clamp DAC voltage is constrained to lie within this range V_{REFBF} to V_{REFTF}. Specifically:

$$VDAC = V_{REFBF} + (V_{REFTF} - V_{REFBF}) \times (0.006 + 0.988 \times (DAC\ code)/1024) \quad (8)$$

DAC codes can range from 0 to 1023. Figure 30 graphically shows the clamp DAC output voltage versus the DAC code.

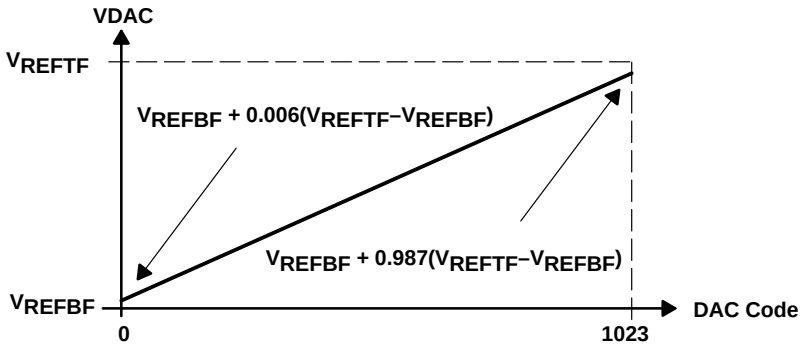

Figure 30. Clamp DAC Output Voltage Versus DAC Register Code Value

If the desired dc level at AIN does not lie within the voltage range V_{REFTF} to V_{REFBF}, then either the CLAMPIN pin can be used instead to provide a suitable reference voltage, or it may be possible to redesign the application to move the AIN input range into the CLAMP DAC voltage range. This is achieved in both top/bottom and center span modes by shifting both REFTS and REFBS up or down by the voltage through which the AIN input range is to be moved.

PRINCIPLES OF OPERATION

power management

In power-sensitive applications (such as battery-powered systems) where the THS1031 ADC is not required to convert continuously, power can be saved between conversion intervals by placing the THS1031 into power-down mode. This is achieved by setting bit 3 (PWDN) of the control register to 1. In power-down mode, the device typically consumes less than 1 mW of power in either top/bottom or center-span modes. Power-down mode is exited by resetting control register bit 3 to 0. On power up, the THS1031 typically requires 5 ms of wake-up time before valid conversion results are available.

In systems where the ADC must run continuously, but where the clamp is not required, setting control register bit 6 (CLDIS to 1), which disables only the clamp circuits, can save power.

Disabling the ORG in applications where the ORG output is not required can also reduce power dissipation by 1 mA analog I_{DD}. This is achieved by connecting the REFSENSE pin to AV_{DD}.

output format and digital I/O

While the $\overline{OE}$ pin is held low, ADC conversion results are output at pins I/O0 (LSB) to I/O9 (MSB). The ADC input over-range indicator is output at pin OVR. OVR is also disabled when $\overline{OE}$ is held high.

The default ADC output data format is unsigned binary (output codes 0 to 1023). The output format can be switched to 2s complement (output codes –512 to 511) by setting control register bit 5 (TWOC) to 1.

writing to the internal registers through the digital I/O bus

Pulling pin $\overline{OE}$ high disables the I/O and OVR pin output drivers, placing the driver outputs in a high impedance state. This allows control register data to be loaded into the THS1031 by presenting it on the I/O0 to I/O9 pins and pulsing the WR pin high to latch the data into the chosen control or DAC register.

Figure 31 shows an example register write cycle where the clamp DAC code is set to 10F (hex) by writing to clamp registers 1 and 2 (see the register map in Table 3). Pins I/O0 to I/O7 are driven to the clamp DAC code lower byte (0F hex) and pins I/08 and I/O9 are both driven to 0 to select clamp register 1 as the data destination. The clamp low-byte data is then loaded into this register by pulsing WR high. The top 2 bits of the DAC word are then loaded by driving 01(hex) on pins I/O0 to I/O7 and by driving pin I/O8 to 1 and pin I/O9 to 0 to select clamp register 2 as the data destination. WR is pulsed a second time to latch this second control word into clamp register 2. Interface timing parameters are given in Figures 1 and 2.

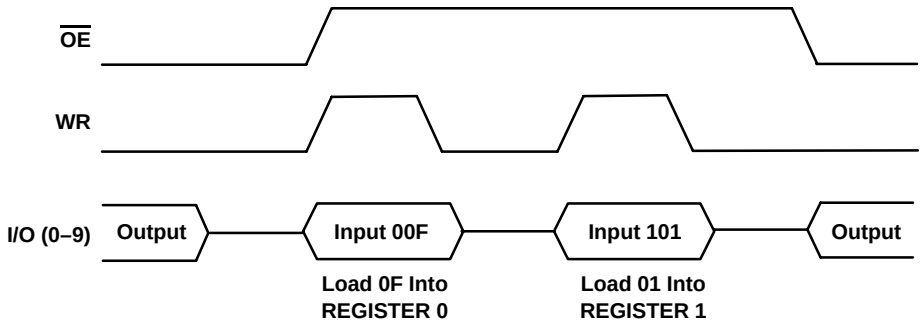

Figure 31. Example Register Write Cycle to Clamp DAC Register

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digital control registers

The THS1031 contains two clamp registers and a control register for user programming of THS1031 operation. Binary data can be written into these registers by using pins I/O0 to I/O9 and the WR and $\overline{OE}$ pins (see the previous section). In input mode, the two I/O bus MSBs are address bits, 00 addressing clamp register 1, 01 clamp register 2, and 10 the control register.

Table 3. Register Map

ADDRESS I/O[9:8]	DESCRIPTION	DEF (HEX)	BIT							
			B7	B6	B5	B4	B3	B2	B1	B0
00	Clamp Reg. 1	00	DAC[7]	DAC[6]	DAC[5]	DAC[4]	DAC[3]	DAC[2]	DAC[1]	DAC[0]
01	Clamp Reg. 2	00							DAC[9]	DAC[8]
10	Control Reg.	01		CLDIS	TWOC	CLINT	PDWN	PGA[2]	PGA[1]	PGA[0]
11	Reserved									

Table 4. Register Contents

REGISTER	BIT NO	BIT NAME(S)	DEFAULT	DESCRIPTION
Control Register I/O[9:8] = 10	2:0	PGA[2:0]	0	PGA gain: 000 = 0.5 001 = 1.0 (default value) 010 = 1.5 011 = 2.0 100 = 2.5 101 = 3.0 110 = 3.5 111 = 4.0
	3	PDWN	0	Power down 0 = THS1031 powered up 1 = THS1031 powered down
	4	CLINT	0	Clamp voltage internal/external 0 = external analog clamp voltage from CLAMPIN pin 1 = from onboard DAC (see clamp register)
	5	TWOC	0	Output format 0 = unsigned binary 1 = two's complement
	6	CLDIS	0	Clamp amplifier disable (for power saving) 0 = Enable 1 = Disable
	7			Unused
Clamp Register 1 I/O[9:8] = 00	7:0	DAC[7:0]	0	Clamp DAC voltage (DAC[0] = LSB.) DAC[9:0] = 00h: Clamp voltage = REFBF DAC[9:0] = 3Fh: Clamp voltage = REFTF
Clamp Register 2 I/O[9:8] = 01	7:2			Unused
	1:0	DAC[9:8]	0	Clamp DAC voltage (DAC[9] = MSB)

PRINCIPLES OF OPERATION

driving the THS1301 analog inputs

driving AIN

Figure 32 shows an equivalent circuit for the THS1031 AIN pin. The load presented to the system at the AIN pin comprises the switched input sampling capacitor, C_{SAMPLE}, and various stray capacitances, C_{P1} and C_{P2}.

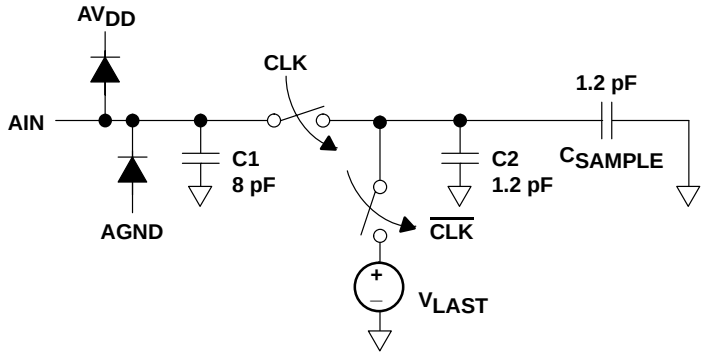

Figure 32. Equivalent Circuit of Analog Input AIN

In any single-ended input mode, V_{LAST} = the average of the previously sampled voltage at AIN and the average of the voltages on pins REFTS and REFBS. In any differential mode, V_{LAST} = the common mode input voltage.

The external source driving AIN must be able to charge and settle into C_{SAMPLE} and the C_{P1} and C_{P2} strays to within 0.5 LSB error while sampling (CLK pin low) to achieve full ADC resolution.

AIN input current and input load modeling

When CLK goes low, the source driving AIN must charge the total switched capacitance $C_S = C_{SAMPLE} + C_{P2}$. The total charge transferred depends on the voltage at AIN and is given by

$$Q_{CHARGING} = (AIN - V_{LAST}) \times C_S. \quad (9)$$

For a fixed voltage at AIN, so that AIN and V_{LAST} do not change between samples, the maximum amount of charge transfer occurs at AIN = FS– (charging current flows out of THS1030) and AIN = FS+ (current flows into THS1030). If AIN is held at the voltage FS+, VLAST = [(FS+) + VM]/2, giving a maximum transferred charge:

$$Q(FS) = \frac{(FS+) - [(FS+) + VM]}{2} \times C_S = \frac{[(FS+) - VM] \times C_S}{2} \quad (10)$$

$$= (1/4 \text{ of the input voltage span}) \times C_S$$

If the input voltage changes between samples, then the maximum possible charge transfer is

$$Q(max) = 3 \times Q(FS) \quad (11)$$

which occurs for a full-scale input change (FS+ to FS– or FS– to FS+) between samples.

The charging current pulses can make the AIN source jump or ring, especially if the source is slightly inductive at high frequencies. Inserting a small series resistor of 20 Ω or less in the input path can damp source ringing. See Figure 33. This resistor can be made larger than 20 Ω if reduced input bandwidth or distortion performance is acceptable.

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AIN input current and input load modeling (continued)

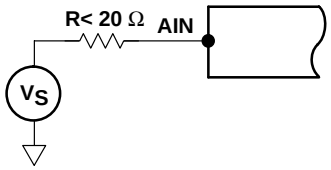

Figure 33. Damping Source Ringing Using a Small Resistor

equivalent input resistance at AIN and ac-coupling to AIN

Some applications may require ac-coupling of the input signal to the AIN pin. Such applications can use an ac-coupling network such as shown in Figure 34.

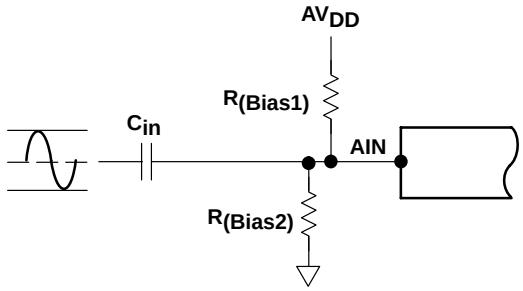

Figure 34. AC-Coupling the Input Signal to the AIN Pin

Note that if the bias voltage is derived from the supplies, as shown in Figure 34, then additional filtering should be used to ensure that noise from the supplies does not reach AIN.

Working with the input current pulse equations given in the previous section is awkward when designing ac-coupling input networks. For such design, it is much simpler to model the AIN input as an equivalent resistance, R_{AIN}, from the AIN pin to a voltage source VM where

VM = (REFTS + REFBS)/2 and $R_{AIN} = 1 / (C_S \times f_{clk})$

where f_{clk} is the CLK frequency.

The high-pass –3 dB cutoff frequency for the circuit shown in Figure 34 is:

$$f_{(-3\ dB)} = \frac{1}{\left(2 \times \pi \times R_{IN}tot\right)} \quad (12)$$

where R_{IN}tot is the parallel combination of Rbias1, Rbias2, and R_{AIN}. This approximation is good provided that the clock frequency, f_{clk}, is much higher than f(–3 dB).

Note also that the effect of the equivalent R_{AIN} and VM at the AIN pin must be allowed for when designing the bias network dc level.

PRINCIPLES OF OPERATION

details

The above value for R_{AIN} is derived by noting that the average AIN voltage must equal the bias voltage supplied by the ac coupling network. The average value of V_{LAST} in equation 13 is thus a constant voltage

$$V_{LAST} = V(\text{AIN bias}) - VM \tag{13}$$

For an input voltage V_{in} at the AIN pin,

$$Qin = (V_{IN} - V_{LAST}) \times C_S \tag{14}$$

Provided that f (–3 dB) is much lower than f_{clk}, a constant current flowing over the clock period can approximate the input charging pulse

$$\begin{aligned} I_{IN} &= Qin/t_{clk} \\ &= Qin \times f_{clk} \\ &= (Vin - V_{LAST}) \times C_S \times f_{clk} \end{aligned} \tag{15}$$

The ac input resistance R_{AIN} is then

$$\begin{aligned} R_{AIN} &= dIin/dVin \\ &= 1 / (dVin / dIin) \\ &= 1 / (C_S \times f_{clk}) \end{aligned} \tag{16}$$

driving the VREF pin (differential mode)

Figure 35 shows the equivalent load on the VREF pin when driving the internal reference buffer via this pin (MODE = $AV_{DD}/2$ and REFSENSE = AV_{DD}).

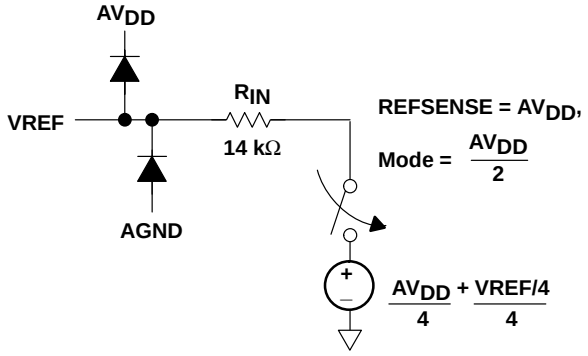

Figure 35. Equivalent Circuit of VREF

The current flowing into I_{IN} is given by

$$I_{IN} = \frac{(3 \times VREF - AV_{DD})}{(4 \times R_{IN})} \tag{17}$$

Note that the actual IIN may differ from this value by up to 50% due to device-to-device processing variations and allowing for operating temperature variations.

The user should ensure that VREF is driven from a low noise, low drift source, well-decoupled to analog ground and capable of driving I_{IN}.

PRINCIPLES OF OPERATION

driving the internal reference buffer (top/bottom mode)

Figure 36 shows the load present on the REFTS and REFBS pins in top/bottom mode due to the internal reference buffer only. The sample and hold must also be driven via these pins, which adds additional load.

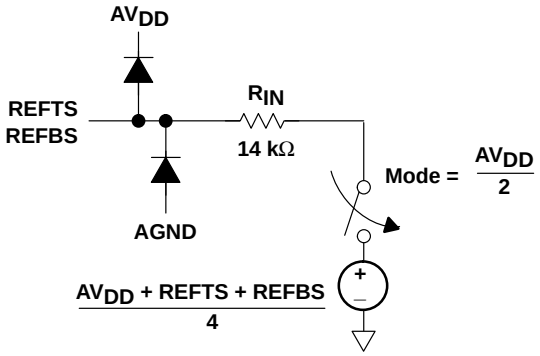

Figure 36. Equivalent Circuit of Inputs to Internal Reference Buffer

Equations for the currents flowing into REFTS and REFBS are:

$$I_{IN}TS = \frac{(3 \times REFTS - AV_{DD} - REFBS)}{(4 \times R_{IN})}$$

$$I_{IN}BS = \frac{(3 \times REFBS - AV_{DD} - REFTS)}{(4 \times R_{IN})} \quad (18)$$

These currents must be provided by the sources on REFTS and REFBS in addition to the requirements of driving the sample and hold. Tolerance on these currents are ±50%.

driving REFTS and REFBS

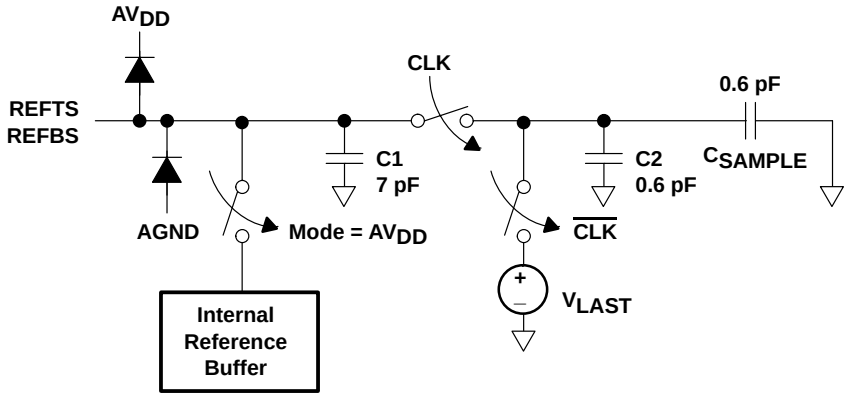

Figure 37. Equivalent Circuit of REFTS and REFBS Inputs

This is essentially a combination of driving the ADC internal reference buffer (if in top/bottom mode) and also driving a switched capacitor load like AIN, but with the sampling capacitor and C_{P2} on each pin now being 0.6 pF and about 0.6 pF respectively.

driving REFTF and REFBF (full external reference mode)

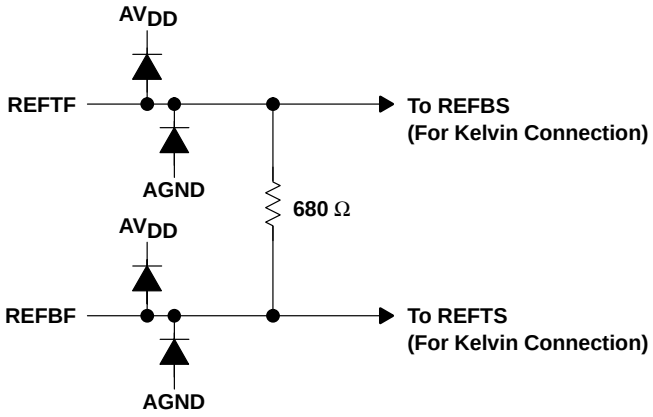

Figure 38. Equivalent Circuit of REFTF and REFBF Inputs

Note the need for off-chip decoupling.

clamp operation

The clamp voltage output level may be established by an analog voltage on the CLAMPIN pin or by programming the on-chip clamp DAC.

clamp acquisition time

Figure 39 shows the basic operation of the clamp circuit with the analog input AIN coupled via an RC circuit.

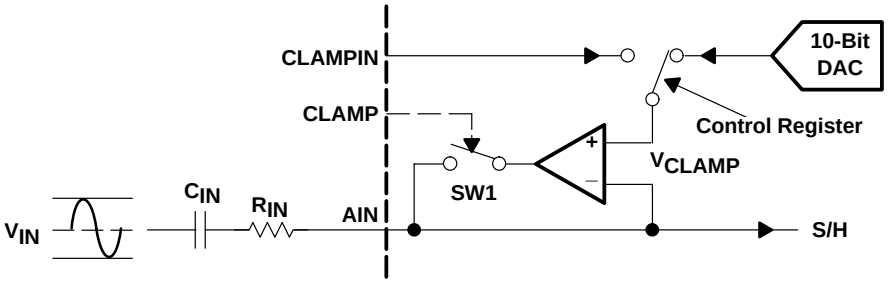

Figure 39. Schematic of Clamp Circuitry

After powerup, the clamp circuit requires SW1 to be closed to charge the coupling capacitor, C_{IN}, to the voltage required to set the dc clamp level at AIN. The charging time required to set the correct clamp voltage is called the clamp acquisition time, t_{ACQ}:

$$t_{ACQ} = C_{IN} \times R_{IN} \times \ln\left(\frac{Vc}{Ve}\right) \quad (19)$$

Vc is the difference between the dc bias voltage level of the input signal, V_{IN}, and the target clamp output voltage, $V_{(clamp)}$. Ve is the difference between the ideal Vc and the actual Vc obtained during the acquisition time. The maximum tolerable error depends on the application requirements.

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clamp acquisition time (continued)

For example, consider clamping an incoming video signal that has a black level near 0.3 V to a black level of 1.3 V at the THS1031 input. The voltage Vc required across the input coupling capacitor is thus 1.3 – 0.3 = 1 V. If a 10 mV or less clamp voltage error Ve will give acceptable system operation, if the source resistance Rin is 20 Ω and the coupling capacitor C_{IN} is 1 µF, then the total clamp pulse duration required to reach this error is:

$$t_{ACQ} = C_{IN} \times R_{IN} \times \ln\left(\frac{Vc}{Ve}\right) = 1\ \mu F \times 20\ \Omega \times \ln\left(\frac{1}{0.01}\right) = 92\ \mu s \text{ (approximately)} \quad (20)$$

Note that SW1 does not have to be closed continuously until the desired clamp voltage is achieved. The clamp level can be acquired over a longer interval by using a series of shorter clamp pulses with total pulse duration at least equal to the acquisition time calculated using equation 19.

droop

The charge pulses entering or leaving AIN caused by the sample and hold switched capacitor input can charge or discharge C_{IN}, causing the voltage at AIN to drift toward VM (the average of REFTS and REFBS) during the time between clamp pulses. This effect is called clamp droop and can be seen as a slow change in the ADC output code when the input signal is a constant dc level. Through careful clamp circuit design, this droop can be kept below 1 LSB, giving no change in the ADC output between clamp pulses.

The clamp voltage droop is a function of the input current to the THS1031 and the time between clamp pulses, td

$$V_{DROOP} = \frac{I_{IN}}{C_{IN}} \times td \text{ (approximately)} \quad (21)$$

Where:

$$I_{IN} = (V_{AIN} - VM) \ / \ \left(2 \times R_{AIN}\right)$$
$$= (V_{AIN} - VM) \times CS \times fclk \ / \ 2$$

R_{AIN} is the input resistance given by equation 20. Cs is approximately 2.5 pF. Substituting I_{IN} into the droop voltage equation gives

$$V_{DROOP} = (V_{AIN} - VM) \times CS \times td \ / \ (2 \times C_{IN}) \quad (22)$$

Note that I_{IN} has maximum value when V_{AIN} is either +FS or –FS, and so the droop rate is worst then the clamp level is near either full-scale input voltage. There is no droop when the clamp level equals VM because I_{IN} is zero. Note that the actual voltage droop may be up to 50% more than given by equation 22 when allowing for temperature variations and device to device processing variations.

For example, with C_{IN} = 1 µF at f_{clk} = 30 MSPS conversion rate in top/bottom mode with REFTS = 2.5 V and REFBS = 0.5 V, the clamp droop over td = 63.5 ms when V_{AIN} = +FS is

$$V_{DROOP} = (V_{AIN} - VM) \times CS \times fclk \times td \ / \ (2 \times C_{IN})$$
$$= (2.5\ V - 1.5\ V) \times 2.5\ pF \times 30\ MMz \ /2$$
$$= 0.0024\ mV$$
$$= 1.25\ LSB \text{ (assuming PGA gain } = 1) \quad (23)$$

PRINCIPLES OF OPERATION

clamp operation (continued)

Thus if a constant voltage is applied to the clamp input that drives the ADC output to code 1023 (with no over-range), then the ADC output code will slowly drop to code 1022, or possibly code 1021, over the period t_d.

If the calculated droop is greater than can be tolerated in the application then increase C_{IN} to slow the droop and hence reduce the voltage change between clamp pulses.

If a high leakage capacitor is used for coupling the input source to the AIN pin then the droop may be significantly larger than calculated above due to the capacitor's rapid rate of self-discharge. Avoid using electrolytic and tantalum coupling capacitors as these usually exhibit much higher leakage then nonpolarized capacitor types. Electrolytic and tantalum capacitors also tend to have higher parasitics inductance, which can cause further problems at high input frequencies.

steady-state clamp voltage error

Under steady-state conditions, the change in the clamp voltage caused during clamping must equal the change caused by clamp droop, otherwise the effect causing the largest voltage change would pull the clamp voltage away until these charging and droop effects equalize.

Figure 40 shows the approximate voltage waveform at AIN resulting from clamp droop during t_d and clamp voltage reacquisition during the clamp pulse time, t_c.

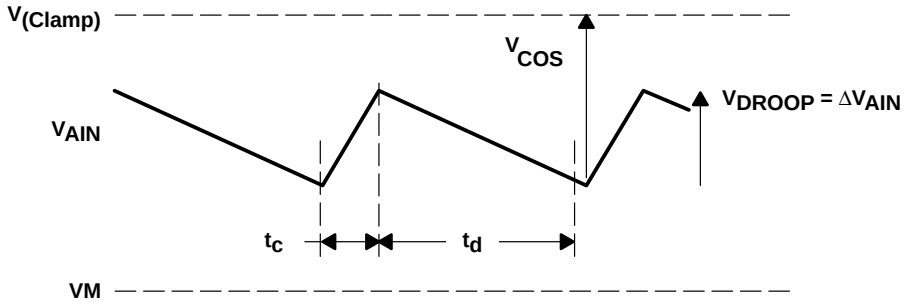


Figure 40. Approximate Waveforms at AIN During Droop and Clamping

The voltage change at AIN during acquisition has been approximated as a linear charging ramp by assuming that almost all of V_{COS} appears across R_{IN}, giving a charging current V_{COS}/Rin (this is a reasonable approximation when V_{COS} is large enough to be a problem). The voltage change at AIN during clamp acquisition is then

$$\Delta V_{AIN} = \frac{V_{COS}}{R_{IN}} \times tc \tag{24}$$

The peak-to-peak voltage variation at AIN must equal the clamp droop voltage at steady state. Equating the droop voltage to the clamp acquisition voltage change gives

$$V_{COS} = \frac{R_{IN} \times I_{IN} \times td}{tc} \tag{25}$$

Where I_{IN} is the input current given by equation, thus for low offset voltage, keep R_{IN} low and ensure that the ratio t_d/t_c is not unreasonably large.

PRINCIPLES OF OPERATION

driving the clock input

Obtaining good performance from the THS1031 requires care when driving the clock input.

Different sections of the sample-and-hold and ADC operate while the clock is low or high. The user should ensure that the clock duty cycle remains near 50% to ensure that all internal circuits have as much time as possible in which to operate.

The CLK pin should be driven from a low jitter source for best dynamic performance. To maintain low jitter at the CLK input, any clock buffers external to the THS1031 should have fast rising edges. Use a fast logic family such as AC or ACT to drive the CLK pin, and consider powering any clock buffers separately from any other logic on the PCB to prevent digital supply noise appearing on the buffered clock edges as jitter.

The CLK input threshold is nominally around $AV_{DD}/2$—ensure that any clock buffers have an appropriate supply voltage to drive above and below this level.

digital output loading and circuit board layout

The THS1031 outputs are capable of driving rail-to-rail with up to 20 pF of load per pin at 30 MHz clock and 3 V digital supply. Minimizing the load on the outputs will improve THS1031 signal-to-noise performance by reducing the switching noise coupling from the THS1031 output buffers to the internal analog circuits. The output load capacitance can be minimized by buffering the THS1031 digital outputs with a low input capacitance buffer placed as close to the output pins as physically possible, and by using the shortest possible tracks between the THS1031 and this buffer.

Noise levels at the output buffers, and hence coupling to the analog circuits within THS1031, becomes worse as the THS1031 digital supply voltage is increased. Where possible, consider using the lowest DV_{DD} that the application can tolerate.

Use good layout practices when designing the application PCB to ensure that any off-chip return currents from the THS1031 digital outputs (and any other digital circuits on the PCB) do not return via the supplies to any sensitive analog circuits. The THS1031 should be soldered directly to the PCB for best performance. Socketing the device will degrade performance by adding parasitic socket inductance and capacitance to all pins.

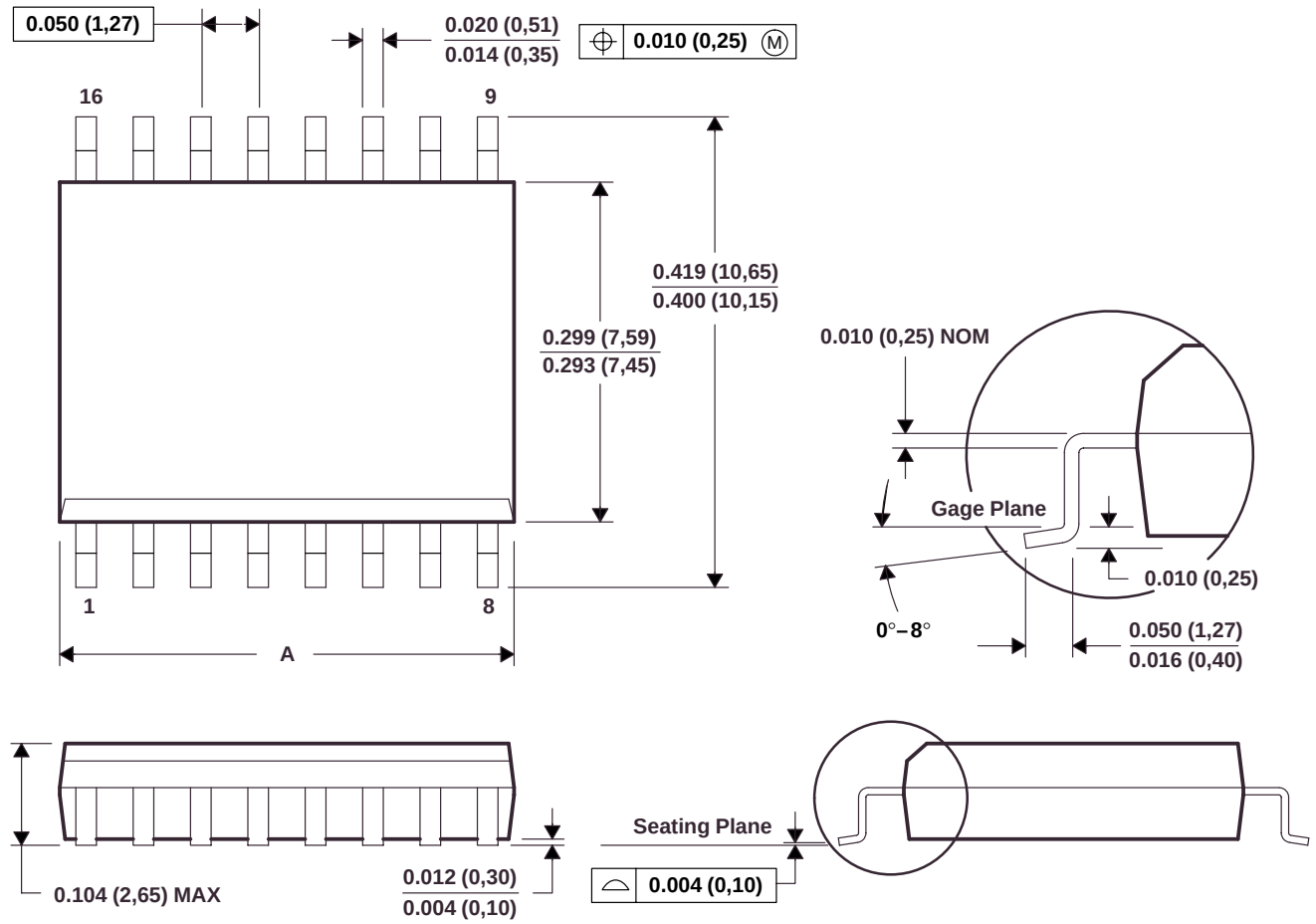
user tips for obtaining best performance from the THS1031

- Voltages on AIN, REFTF and REFBF and REFTS and REFBS must all be inside the supply rails.
- ORG modes offer the simplest configurations for ADC reference generation.
- Choose differential input mode for best distortion performance.
- Choose a 2-V ADC input span for best noise performance.
- Choose a 1-V ADC input span for best distortion performance.
- If the ORG is not used to provide ADC reference voltages, its output may be used for other purposes in the system. Care should be taken to ensure noise is not injected into the THS1031.
- Use external voltage sources for ADC reference generation where there are stringent requirements on accuracy and drift.
- Drive clock input CLK from a low-jitter, fast logic stage, with a well-decoupled power supply and short PCB traces.

MECHANICAL DATA

DW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

16 PINS SHOWN



DIM \ PINS **	16	20	24	28
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

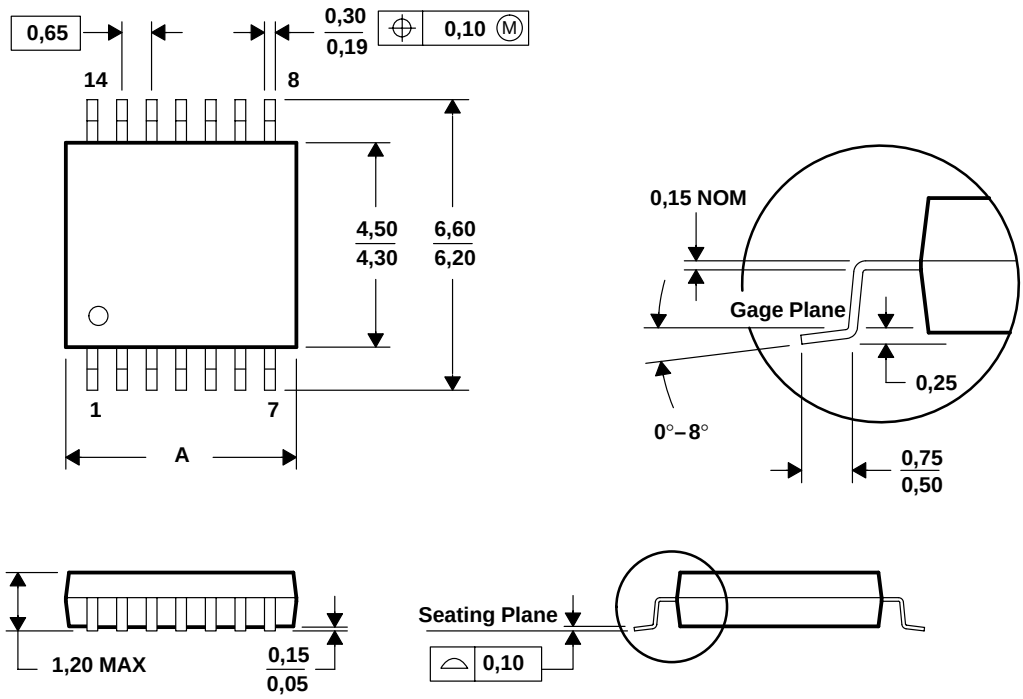
4040000/C 07/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

MECHANICAL DATA

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
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