

### Features

- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage – dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for both channels
- 3.3 V input logic compatible
- Separate logic supply range from 3.3 V to 20 V
- Logic and power ground  $\pm 5$  V offset
- CMOS Schmitt-triggered inputs with pull-down
- Cycle by cycle edge-triggered shutdown logic
- Matched propagation delay for both channels
- Output in phase with inputs
- Leadfree, RoHS Compliant

### Description

The IRS2113MPBF is a high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 V.

### Product Summary

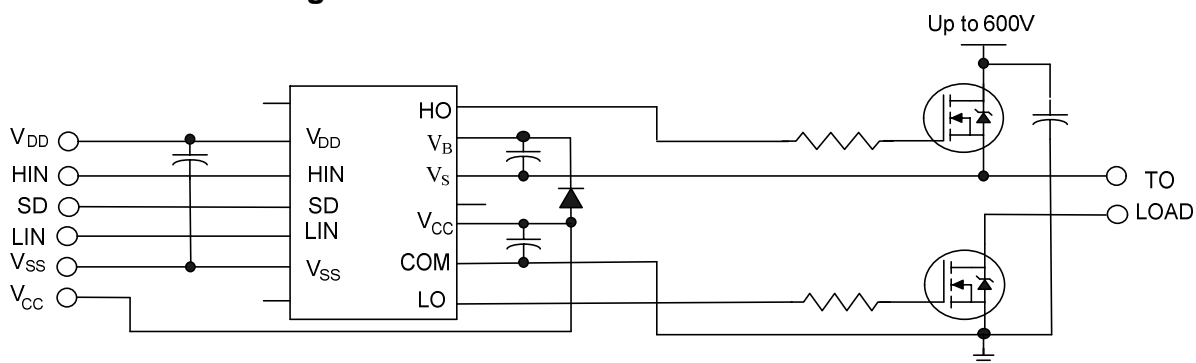
Topology	2 channels
$V_{\text{OFFSET}}$	600 V max
$V_{\text{OUT}}$	10 V – 20 V
$I_{\text{o+}}$ & $I_{\text{o-}}$ (typical)	2.5 A / 2.5 A
$t_{\text{ON}}$ & $t_{\text{OFF}}$ (typical)	130 ns & 120 ns
Delay Matching	20 ns max

### Package Option



MLPQ4x4-16-Lead  
(without 2 leads)

### Typical Connection Diagram



(Refer to Leads Assignment for correct pin configurations) This diagram shows electrical connections only. Please refer to our Application Notes and Design Tips for proper circuit board layout.

**Qualification Information<sup>†</sup>**

<b>Qualification Level</b>		Industrial <sup>††</sup> (per JEDEC JESD 47)	
		Comments: This IC has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.	
<b>Moisture Sensitivity Level</b>		MLPQ4x4 14L	MSL2 <sup>†††</sup> (per IPC/JEDEC J-STD-020)
<b>ESD</b>	Machine Model	Class A (+/-200V) (per JEDEC standard JESD22-A115)	
	Human Body Model	Class 1B (+/-1000V) (per EIA/JEDEC standard EIA/JESD22-A114)	
	Charged Device Model	Class III (+/-1000V) (per JEDEC standard JESD22-C101)	
<b>IC Latch-Up Test</b>		Class II, Level A (per JESD78A)	
<b>RoHS Compliant</b>		Yes	

† Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

### Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V <sub>B</sub>	High-side floating supply voltage	-0.3	625	V
V <sub>S</sub>	High-side floating supply offset voltage	V <sub>B</sub> - 20	V <sub>B</sub> + 0.3	
V <sub>HO</sub>	High-side floating output voltage	V <sub>S</sub> - 0.3	V <sub>B</sub> + 0.3	
V <sub>CC</sub>	Low-side fixed supply voltage	-0.3	25	
V <sub>LO</sub>	Low-side output voltage	-0.3	V <sub>CC</sub> + 0.3	
V <sub>DD</sub>	Logic supply voltage	-0.3	V <sub>SS</sub> + 20 (†)	
V <sub>SS</sub>	Logic supply offset voltage	V <sub>CC</sub> - 20	V <sub>CC</sub> + 0.3	
V <sub>IN</sub>	Logic input voltage (HIN, LIN & SD)	V <sub>SS</sub> - 0.3	V <sub>DD</sub> + 0.3	
dV <sub>S</sub> /dt	Allowable offset supply voltage transient (Fig. 2)	—	50	V/ns
P <sub>D</sub>	Package power dissipation @ TA ≤ 25°C	—	2.08	W
R <sub>thJA</sub>	Thermal resistance, junction to ambient	—	36	°C/W
T <sub>J</sub>	Junction temperature	—	150	°C
T <sub>S</sub>	Storage temperature	-55	150	
T <sub>L</sub>	Lead temperature (soldering, 10 seconds)	—	300	

† All supplies are fully tested at 25 V, and an internal 20 V clamp exists for each supply.

### Recommended Operating Conditions

The input/output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V<sub>S</sub> and V<sub>SS</sub> offset rating are tested with all supplies biased at 15 V differential.

Symbol	Definition	Min.	Max.	Units
V <sub>B</sub>	High-side floating supply absolute voltage	V <sub>S</sub> + 10	V <sub>S</sub> + 20	V
V <sub>S</sub>	High-side floating supply offset voltage	†	600	
V <sub>HO</sub>	High-side floating output voltage	V <sub>S</sub>	V <sub>B</sub>	
V <sub>CC</sub>	Low-side fixed supply voltage	10	20	
V <sub>LO</sub>	Low-side output voltage	0	V <sub>CC</sub>	
V <sub>DD</sub>	Logic supply voltage	V <sub>SS</sub> + 3	V <sub>SS</sub> + 20	
V <sub>SS</sub>	Logic ground offset voltage	-5 (††)	5	
V <sub>IN</sub>	Logic input voltage (HIN, LIN & SD)	V <sub>SS</sub>	V <sub>DD</sub>	
T <sub>A</sub>	Ambient temperature	-40	125	°C

† Logic operational for V<sub>S</sub> of -4 V to +500 V. Logic state held for V<sub>S</sub> of -4 V to -V<sub>BS</sub>.  
(Please refer to the Design Tip DT97 -3 for more details).

†† When V<sub>DD</sub> < 5 V, the minimum V<sub>SS</sub> offset is limited to -V<sub>DD</sub>.

### Static Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ,  $V_{DD}$ ) = 15 V,  $T_A$  = 25°C and  $V_{SS}$  = COM unless otherwise specified. The  $V_{IL}$ ,  $V_{TH}$  and  $I_{IN}$  parameters are referenced to  $V_{SS}$  and are applicable to all three logic input leads: HIN, LIN and SD. The  $V_O$  and  $I_O$  parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

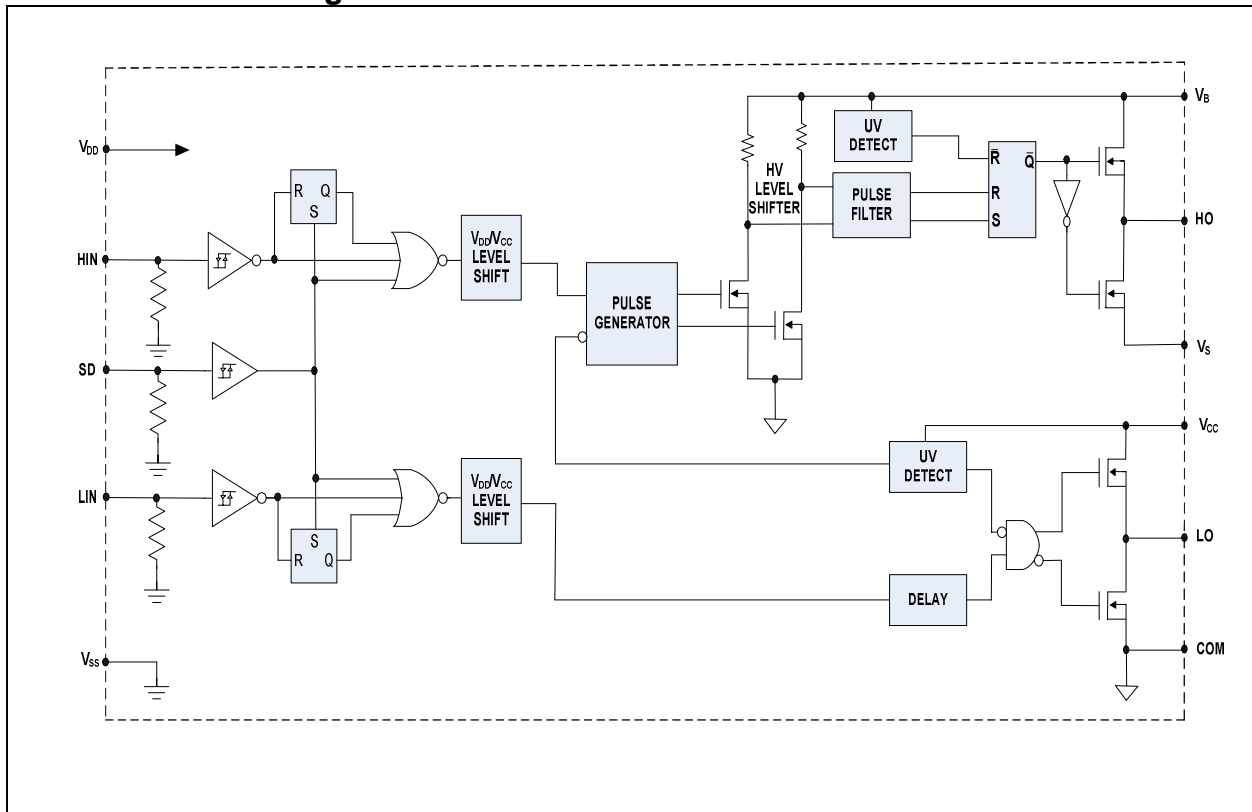
Symbol	Definition	Min	Typ	Max	Units	Test Conditions	
$V_{IH}$	Logic "1" input voltage	9.5	—	—	V		
$V_{IL}$	Logic "0" input voltage	—	—	6.0			
$V_{OH}$	High level output voltage, $V_{BIAS} - V_O$	—	—	1.4			$I_O = 0$ A
$V_{OL}$	Low level output voltage, $V_O$	—	—	0.15			$I_O = 20$ mA
$I_{LK}$	Offset supply leakage current	—	—	50	$\mu$ A	$V_B = V_S = 600$ V	
$I_{QBS}$	Quiescent $V_{BS}$ supply current	—	125	230		$V_{IN} = 0$ V or $V_{DD}$	
$I_{QCC}$	Quiescent $V_{CC}$ supply current	—	180	340			
$I_{QDD}$	Quiescent $V_{DD}$ supply current	—	15	30			
$I_{IN+}$	Logic "1" input bias current	—	20	40		$V_{IN} = V_{DD}$	
$I_{IN-}$	Logic "0" input bias current	—	—	5.0		$V_{IN} = 0$ V	
$V_{BSUV+}$	$V_{BS}$ supply undervoltage positive going threshold	7.5	8.6	9.7	V		
$V_{BSUV-}$	$V_{BS}$ supply undervoltage negative going threshold	7.0	8.2	9.4			
$V_{CCUV+}$	$V_{CC}$ supply undervoltage positive going threshold	7.4	8.5	9.6			
$V_{CCUV-}$	$V_{CC}$ supply undervoltage negative going threshold	7.0	8.2	9.4			
$I_{O+}$	Output high short circuit pulsed current	2.0	2.5	—	A	$V_O = 0$ V, $V_{IN} = V_{DD}$ $PW \leq 10$ $\mu$ s	
$I_{O-}$	Output low short circuit pulsed current	2.0	2.5	—		$V_O = 15$ V, $V_{IN} = 0$ V $PW \leq 10$ $\mu$ s	

### Dynamic Electrical Characteristics

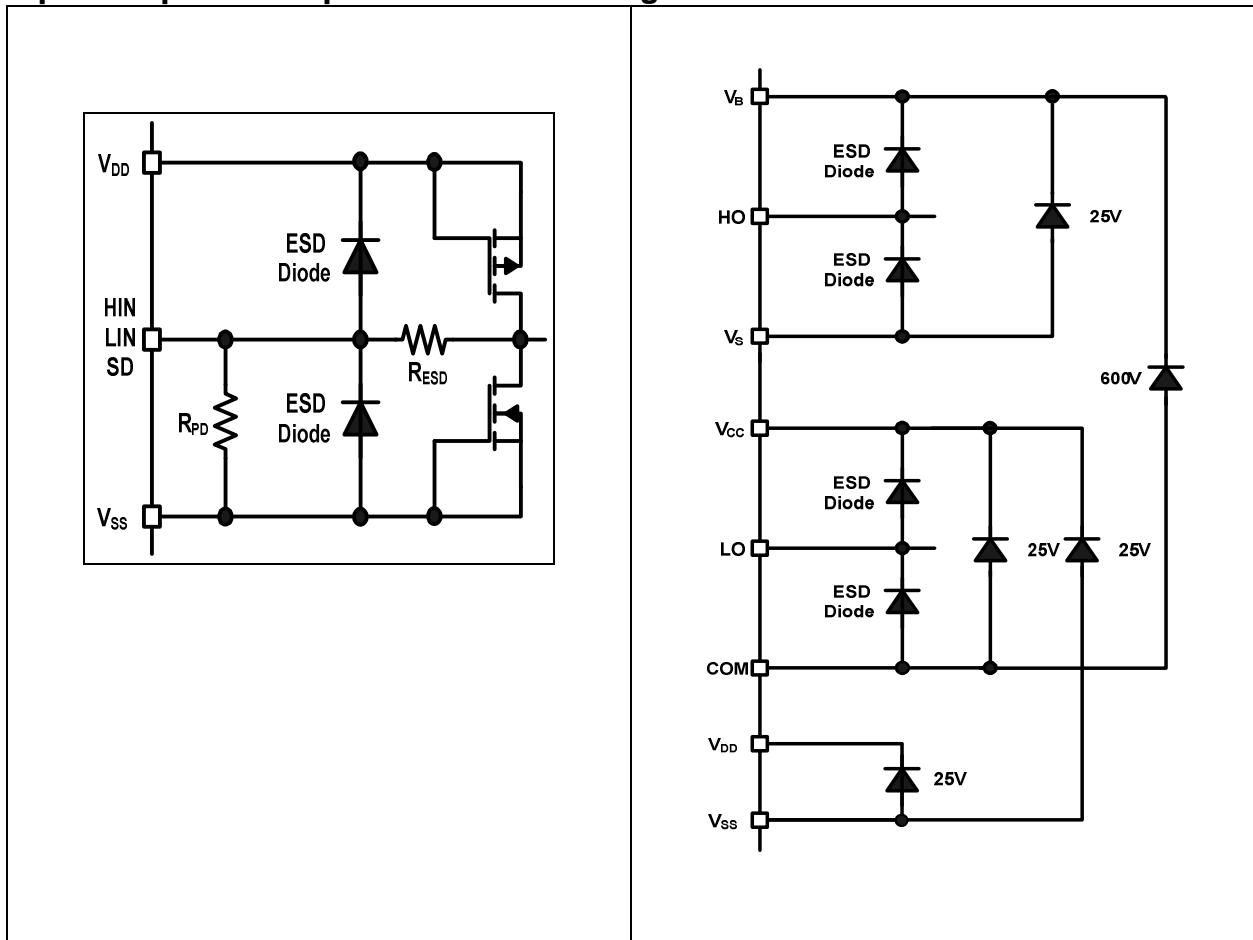
$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ,  $V_{DD}$ ) = 15 V,  $C_L$  = 1000 pF,  $T_A$  = 25°C and  $V_{SS}$  = COM unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Fig. 3.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
$t_{on}$	Turn-on propagation delay	—	130	200	ns	$V_S = 0$ V
$t_{off}$	Turn-off propagation delay	—	120	190		$V_S = 600$ V
$t_{sd}$	Shutdown propagation delay	—	130	160		
$t_r$	Turn-on rise time	—	25	35		
$t_f$	Turn-off fall time	—	17	25		
MT	Delay matching, HS & LS turn on/off	—	—	20		

**Functional Block Diagram**



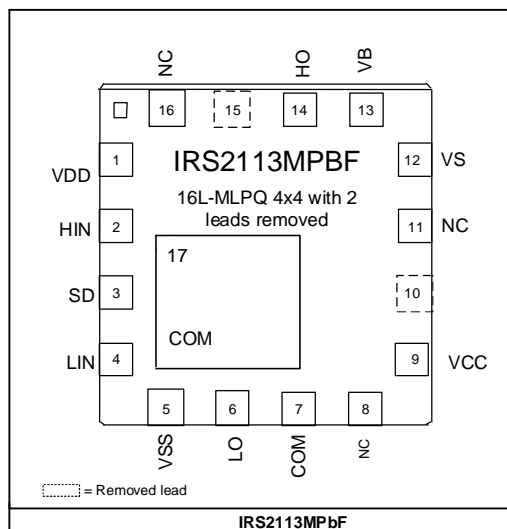
**Input/Output Pin Equivalent Circuit Diagrams**



### Lead Definitions

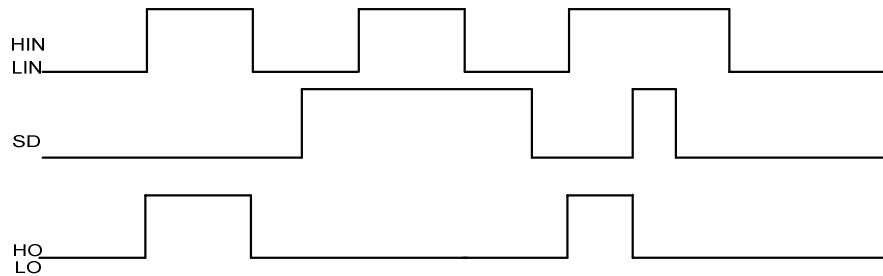
PIN	Symbol	Description
1	V <sub>DD</sub>	Logic supply
2	HIN	Logic input for high-side gate driver output (HO), in phase
3	SD	Logic input for shutdown
4	LIN	Logic input for low-side gate driver output (LO), in phase
5	V <sub>SS</sub>	Logic ground
6	LO	Low-side gate drive output
7	COM	Low-side return
8	NC	No Connection
9	V <sub>CC</sub>	Low-side supply
10	NC	No Connection (pin removed)
11	NC	No Connection
12	V <sub>S</sub>	High-side floating supply return
13	V <sub>B</sub>	High-side floating supply
14	HO	High-side gate drive output
15	NC	No Connection (pin removed)
16	NC	No Connection

### Lead Assignments

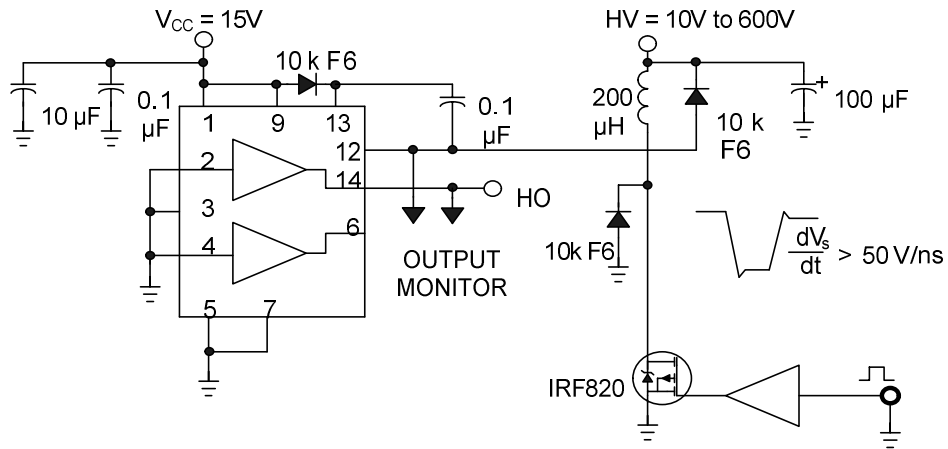


Central exposed pad (17) is internally connected to ground. It is recommended to connect the central exposed pad to COM externally for better electrical performance.

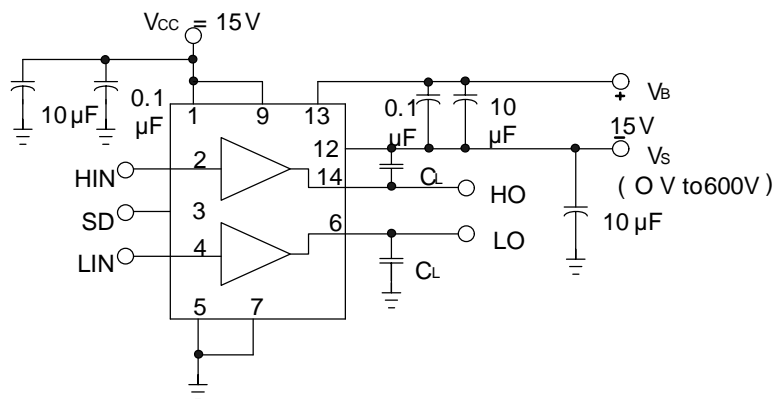
**Application Information and Additional Details**



**Figure 1: Input/Output Timing Diagram**

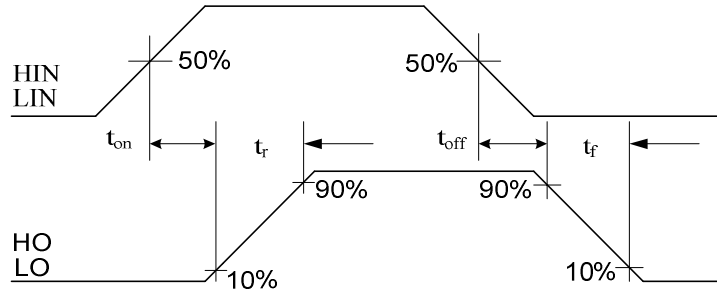


**Figure 2: Floating Supply Voltage Transient Test Circuit**

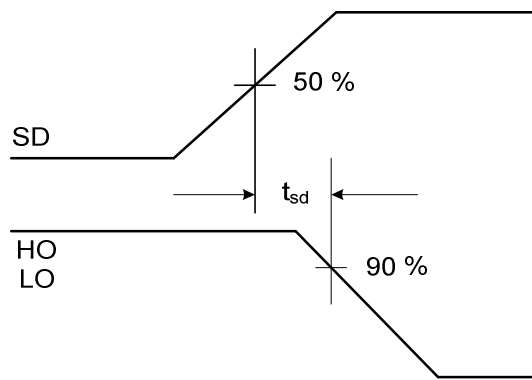


**Figure 3: Switching Time Test Circuit**

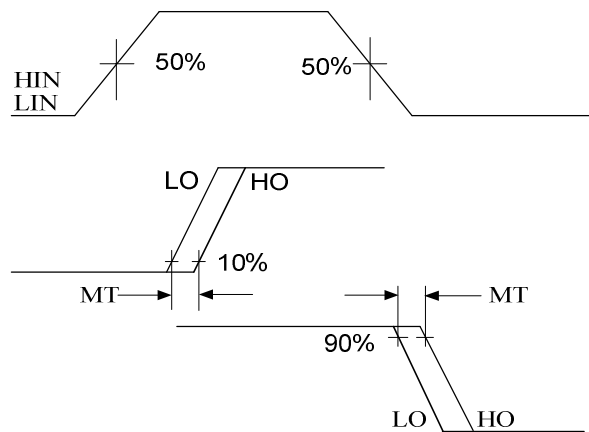




**Figure 4: Switching Time Waveform Definitions**



**Figure 5: Shutdown Waveform Definitions**



**Figure 6: Delay Matching Waveform Definitions**

**Parameter Temperature Trends**

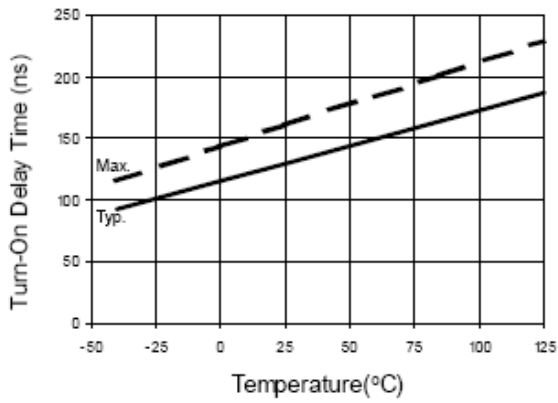


Figure 7A. Turn-On Time vs. Temperature

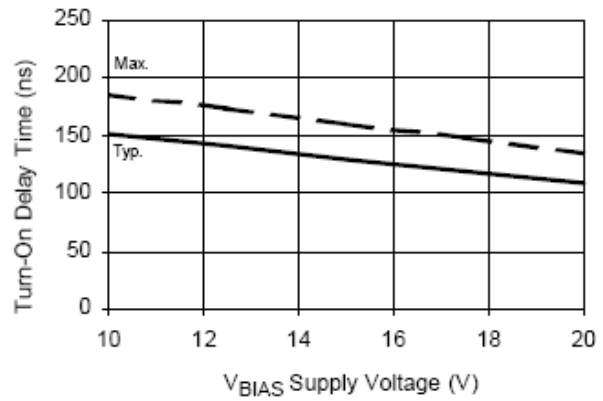


Figure 7B. Turn-On Time vs. Supply Voltage

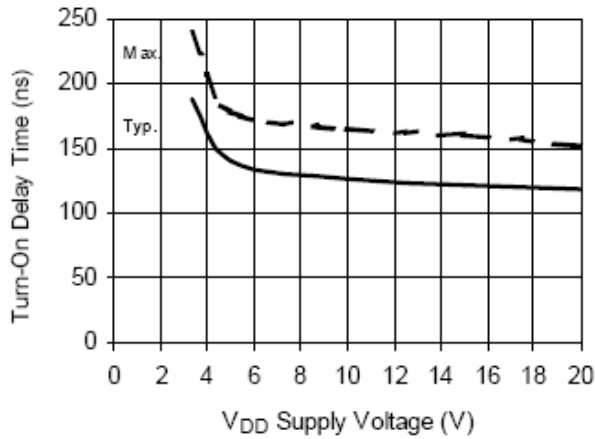


Figure 7C. Turn-On Time vs. V<sub>DD</sub> Supply Voltage

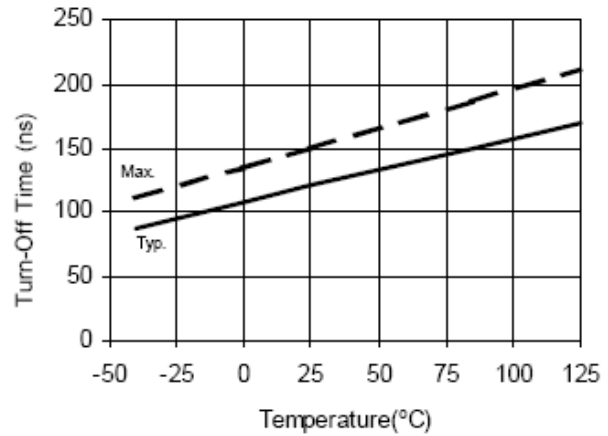


Figure 8A. Turn-Off Time vs. Temperature

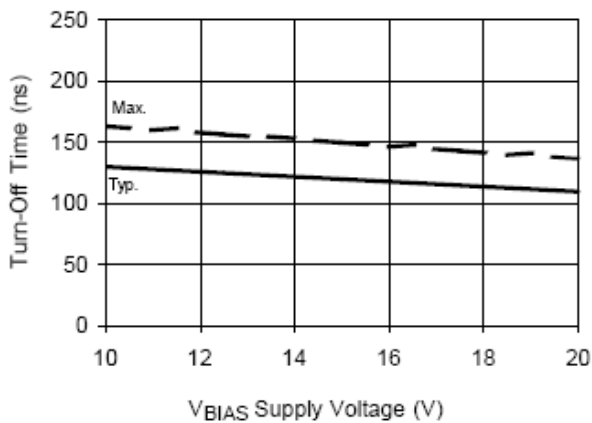


Figure 8B. Turn-Off Time vs. Supply Voltage

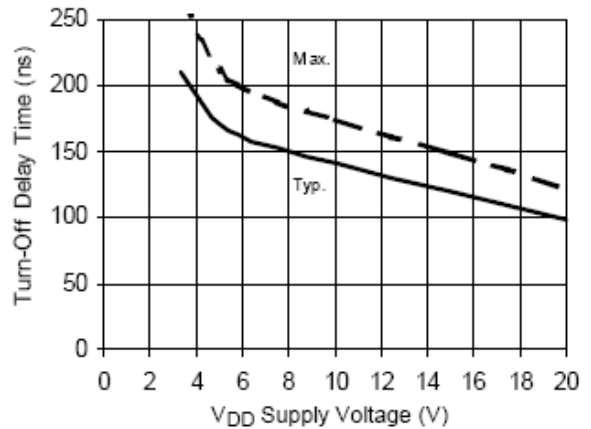


Figure 8C. Turn-Off Time vs. V<sub>DD</sub> Supply Voltage

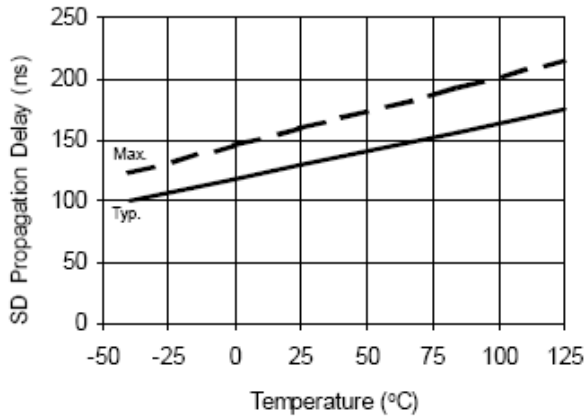


Figure 9A. Shutdown Time vs. Temperature

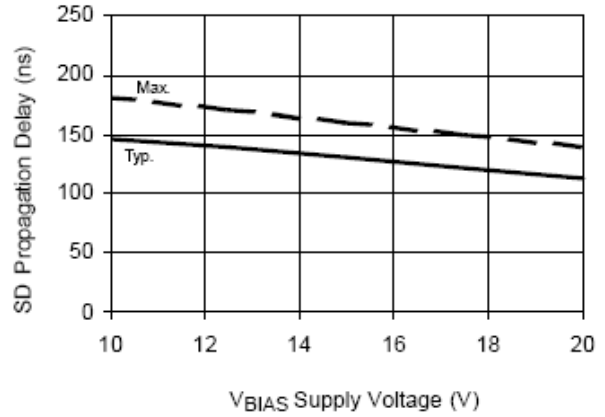


Figure 9B. Shutdown Time vs. Supply Voltage

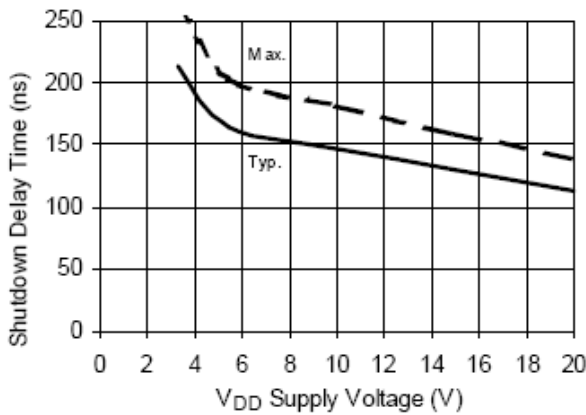


Figure 9C. Shutdown Time vs. VDD Supply Voltage

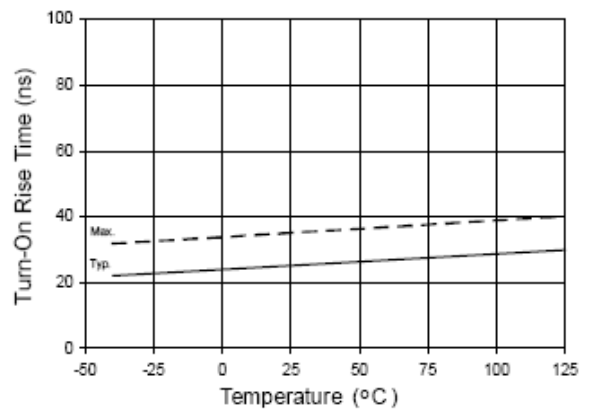


Figure 10A. Turn-On Rise Time vs. Temperature

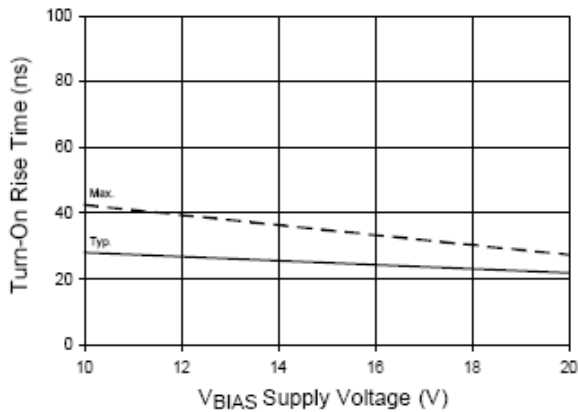


Figure 10B. Turn-On Rise Time vs. Voltage

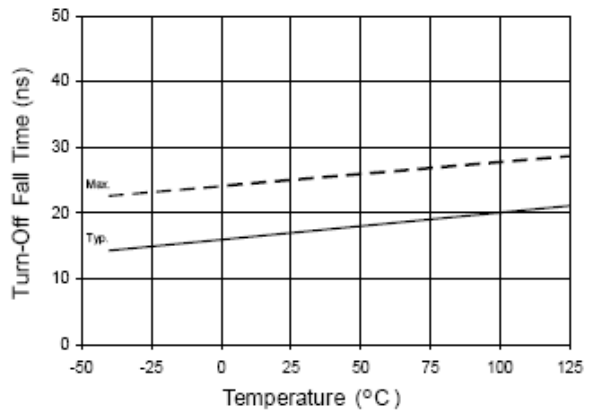


Figure 11A. Turn-Off Fall Time vs. Temperature

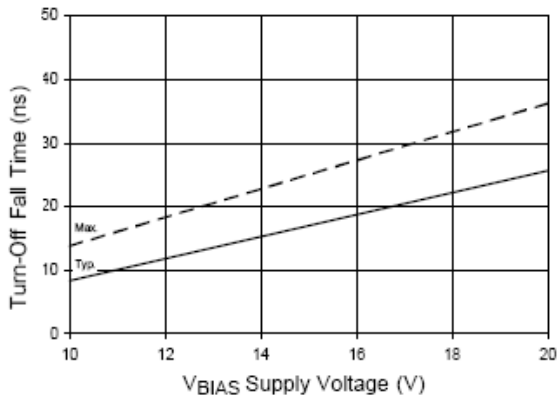


Figure 11B. Turn-Off Fall Time vs. Voltage

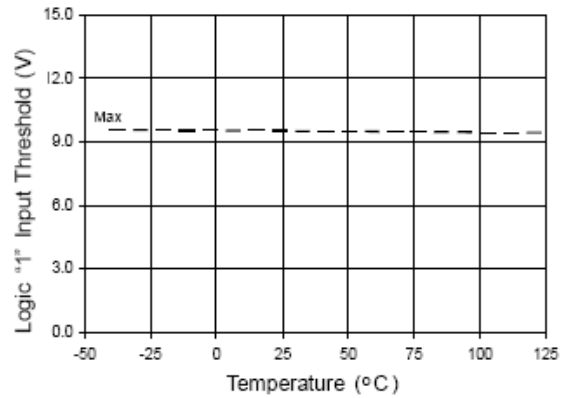


Figure 12A. Logic "1" Input Threshold vs. Temperature

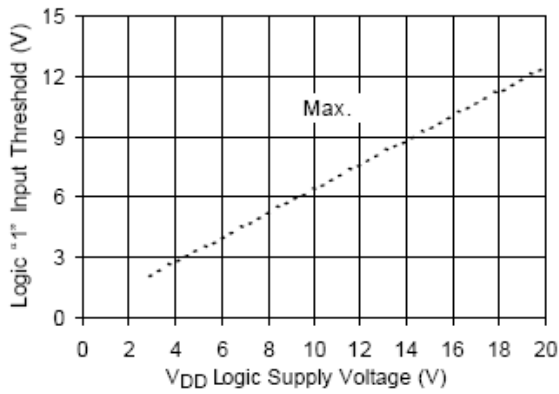


Figure 12B. Logic "1" Input Threshold vs. Voltage

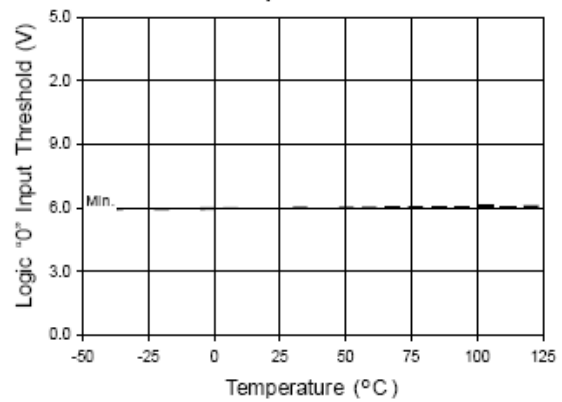


Figure 13A. Logic "0" Input Threshold vs. Temperature

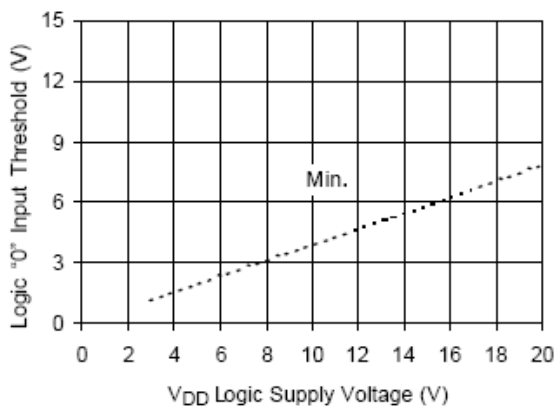


Figure 13B. Logic "0" Input Threshold vs. Voltage

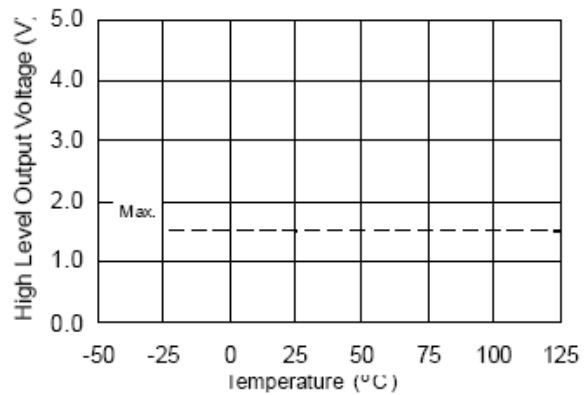


Figure 14A. High Level Output Voltage vs. Temperature ( $I_O = 0$  mA)

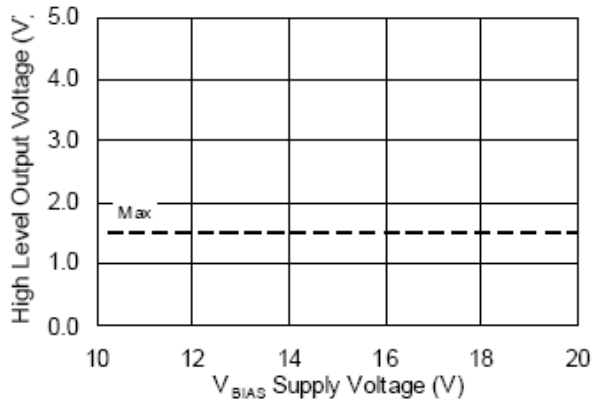


Figure 14B. High Level Output Voltage vs. Supply Voltage ( $I_O = 0$  mA)

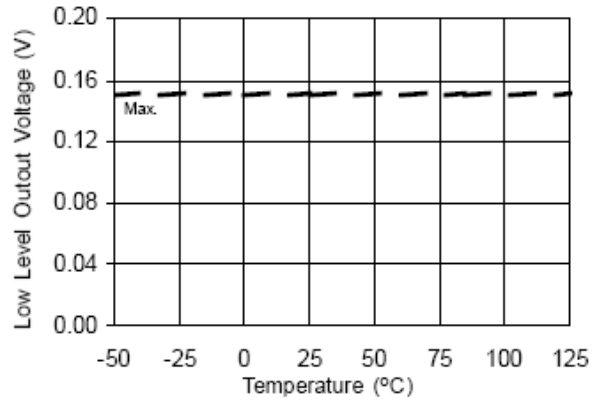


Figure 15A. Low Level Output vs. Temperature

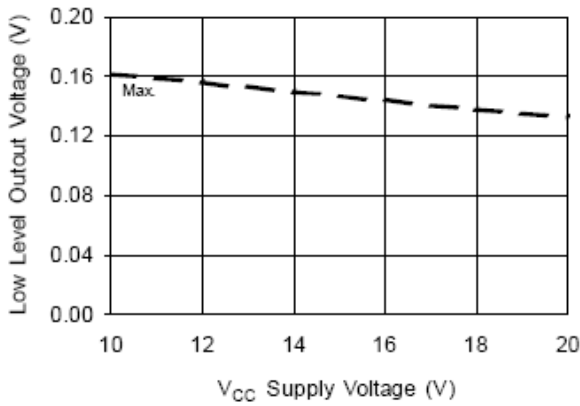


Figure 15B. Low Level Output vs. Supply Voltage

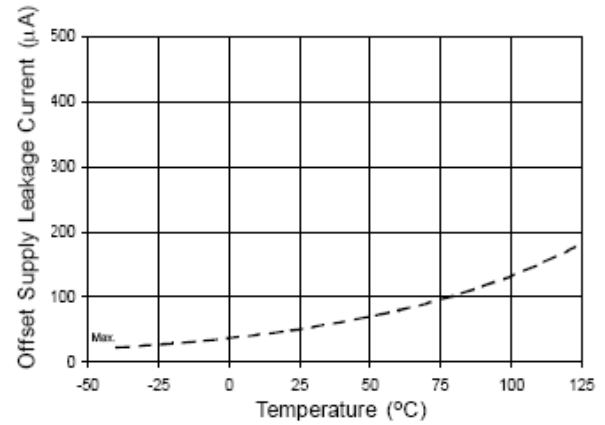


Figure 16A. Offset Supply Current vs. Temperature

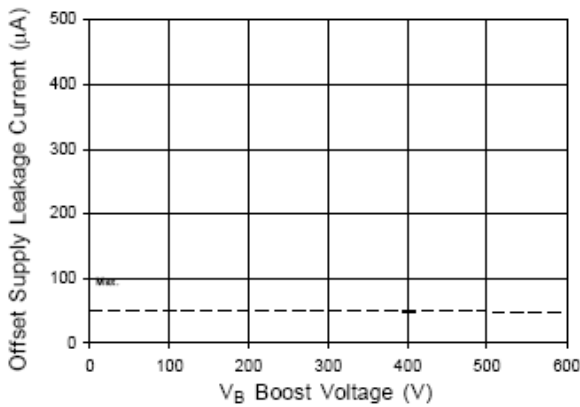


Figure 16B. Offset Supply Current vs. Voltage

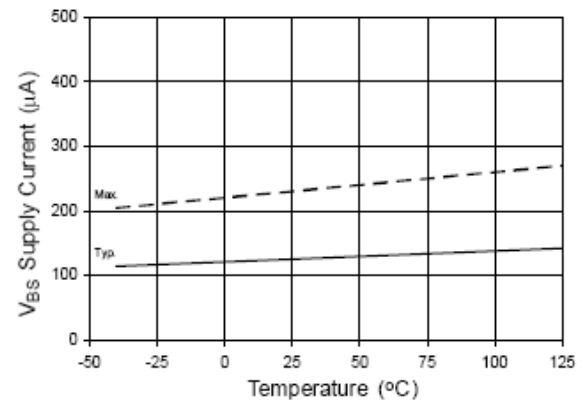


Figure 17A. VBS Supply Current vs. Temperature

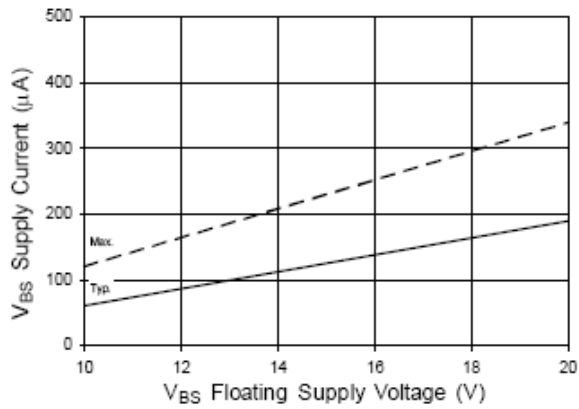


Figure 17B. V<sub>BS</sub> Supply Current vs. Voltage

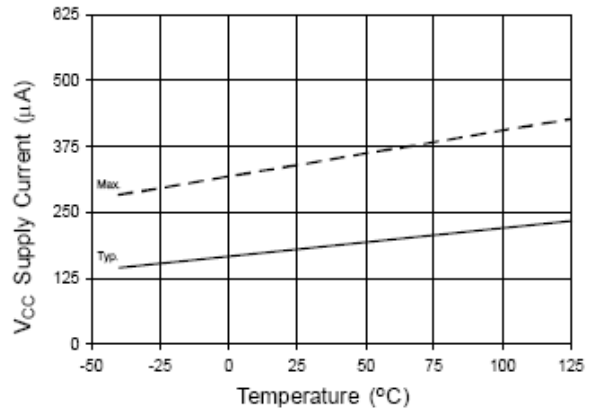


Figure 18A. V<sub>CC</sub> Supply Current vs. Temperature

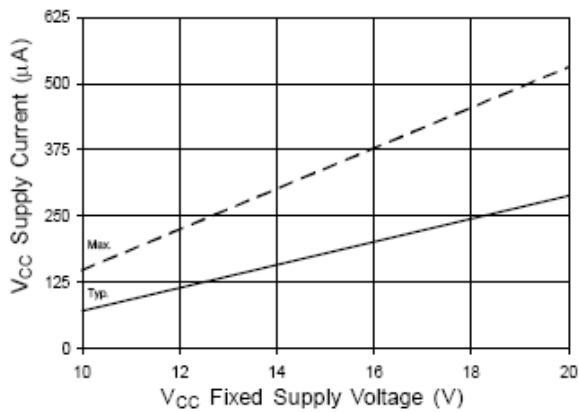


Figure 18B. V<sub>CC</sub> Supply Current vs. Voltage

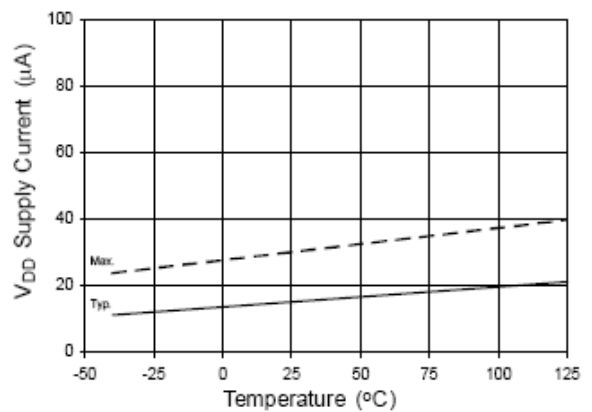


Figure 19A. V<sub>DD</sub> Supply Current vs. Temperature

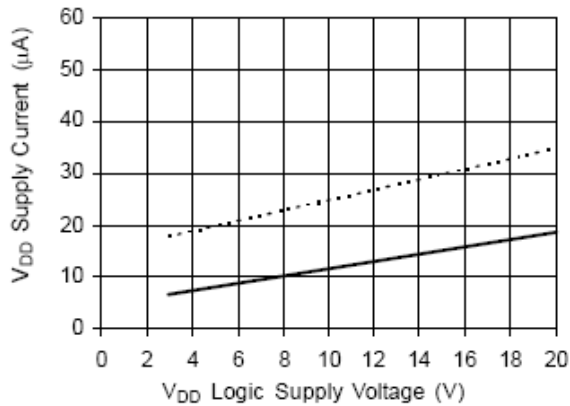


Figure 19B. V<sub>DD</sub> Supply Current vs. V<sub>DD</sub> Voltage

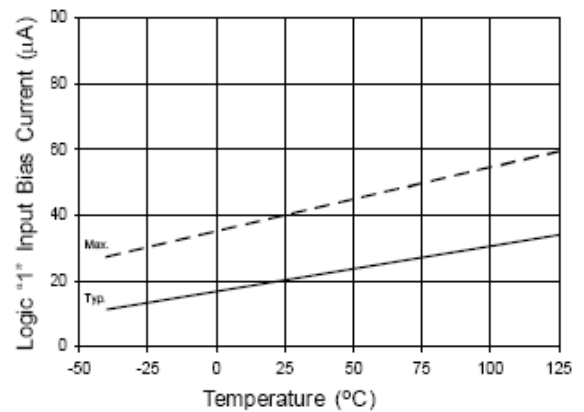


Figure 20A. Logic "1" Input Current vs. Temperature

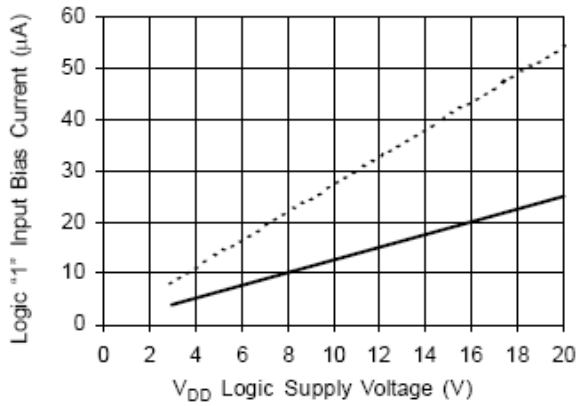


Figure 20B. Logic "1" Input Current vs.  $V_{DD}$  Voltage

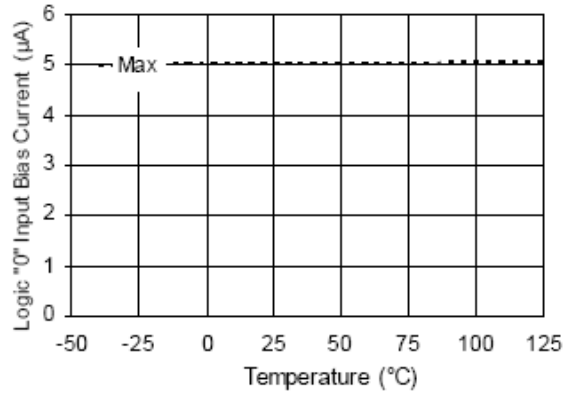


Figure 21A. Logic "0" Input Bias Current vs. Temperature

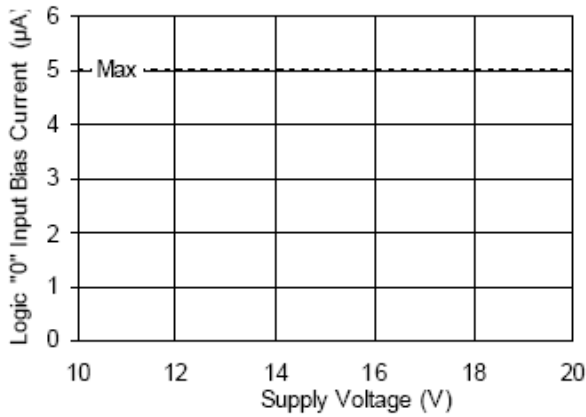


Figure 21B. Logic "0" Input Bias Current vs. Voltage

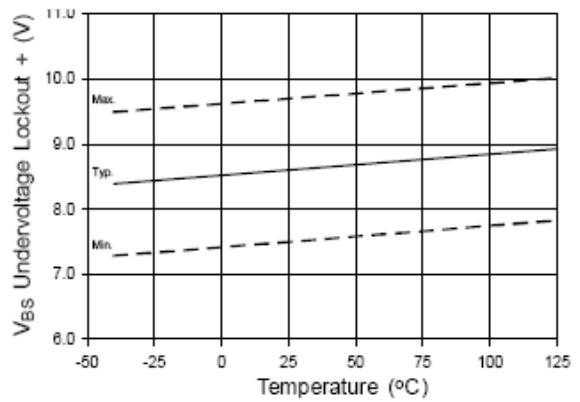


Figure 22.  $V_{BS}$  Undervoltage (+) vs. Temperature

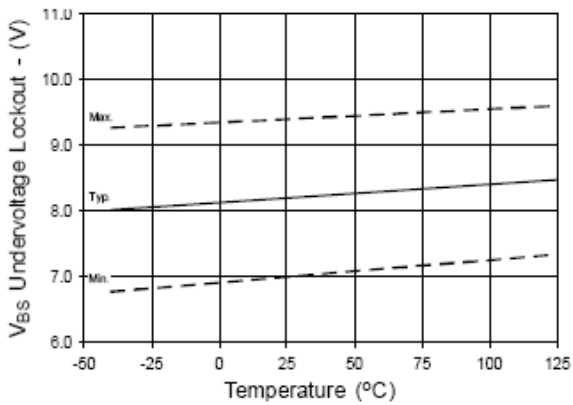


Figure 23.  $V_{BS}$  Undervoltage (-) vs. Temperature

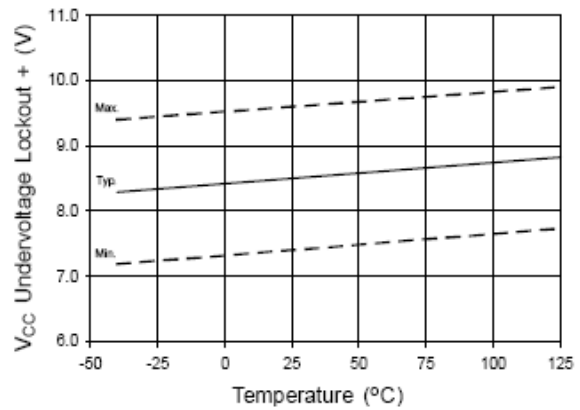
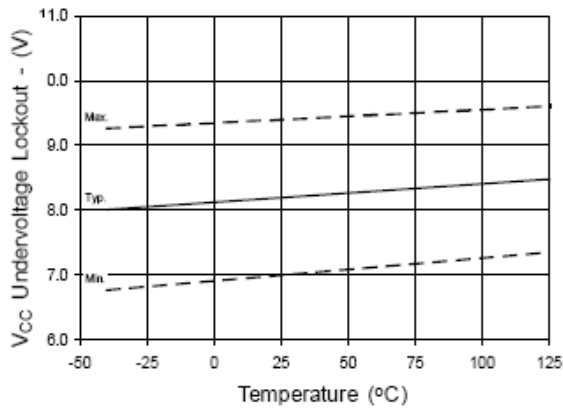
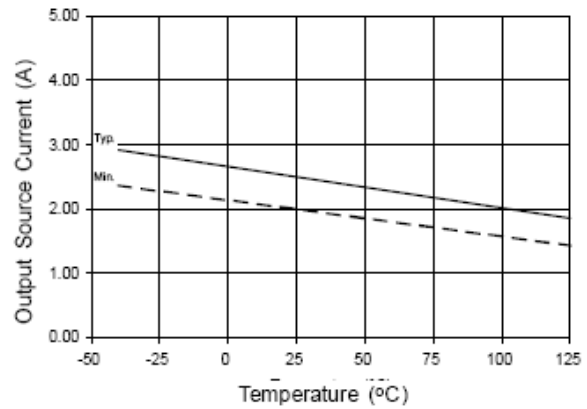


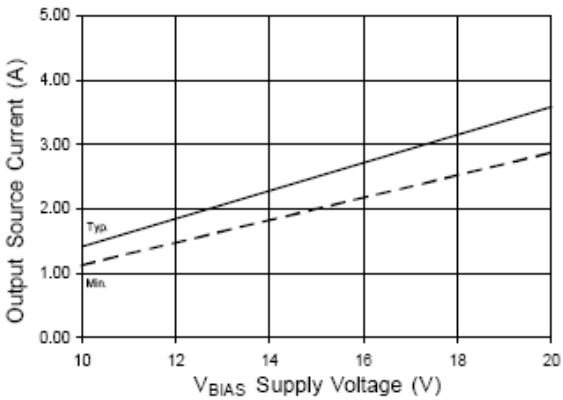
Figure 24.  $V_{CC}$  Undervoltage (+) vs. Temperature



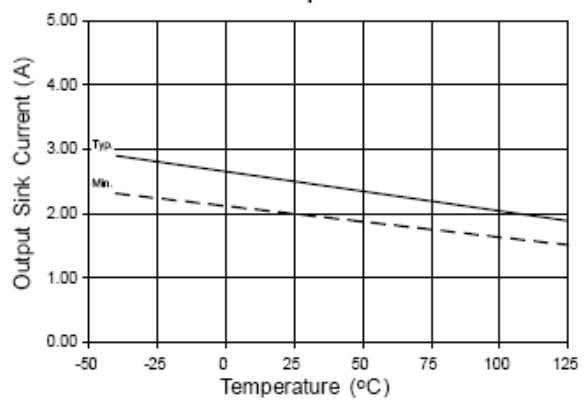
**Figure 25. V<sub>CC</sub> Undervoltage (-) vs. Temperature**



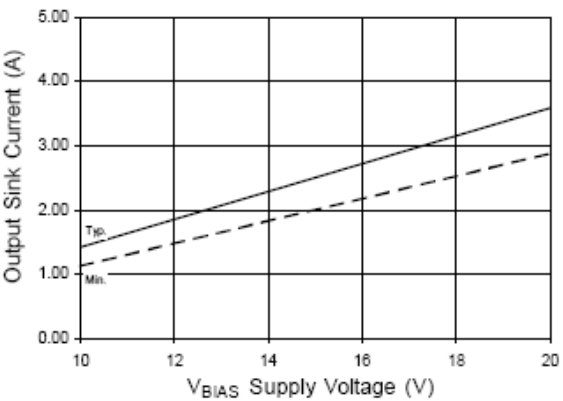
**Figure 26A. Output Source Current vs. Temperature**



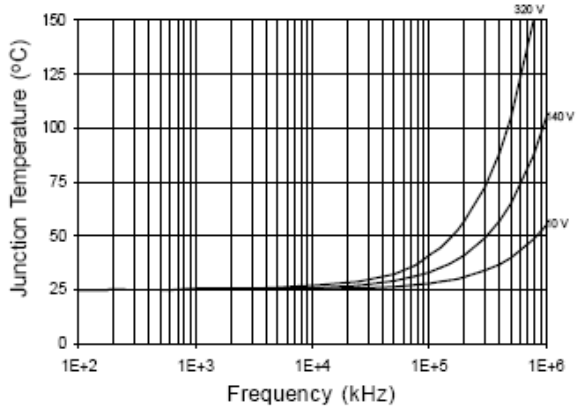
**Figure 26B. Output Source Current vs. Voltage**



**Figure 27A. Output Sink Current vs. Temperature**

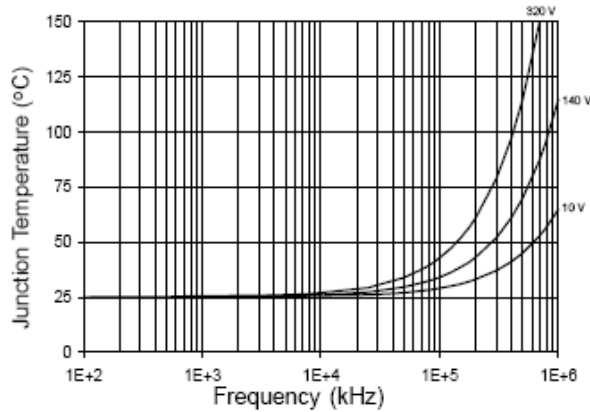


**Figure 27B. Output Sink Current vs. Voltage**

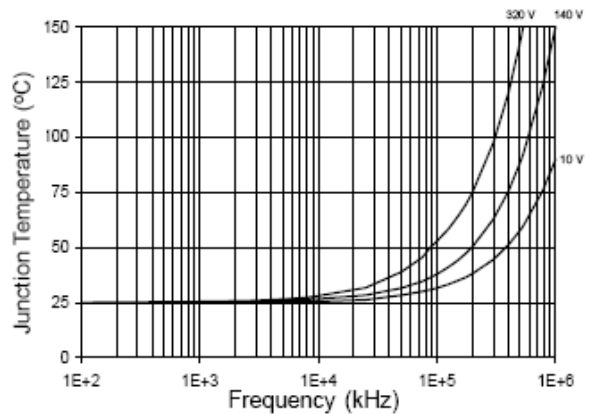


**Figure 28. IRS2110/IRS2113 T<sub>J</sub> vs. Frequency (IRFBC20) R<sub>GATE</sub> = 33 Ω, V<sub>CC</sub> = 15 V**

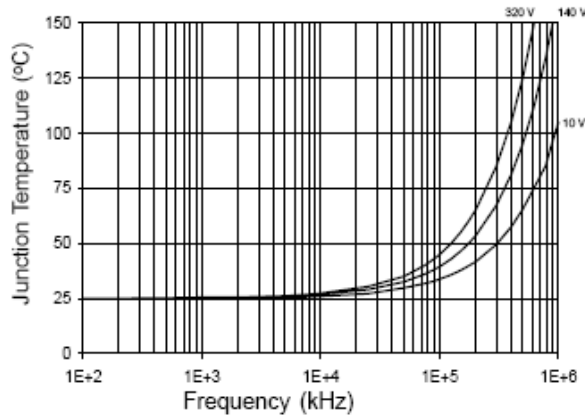




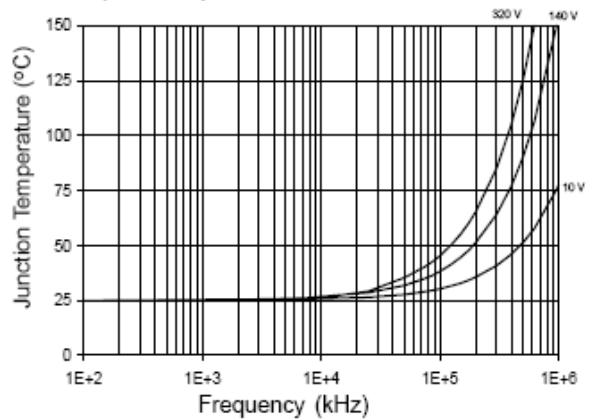
**Figure 29. IRS2110/IRS2113  $T_J$  vs. Frequency (IRFBC30)  $R_{GATE} = 22 \Omega$ ,  $V_{CC} = 15 V$**



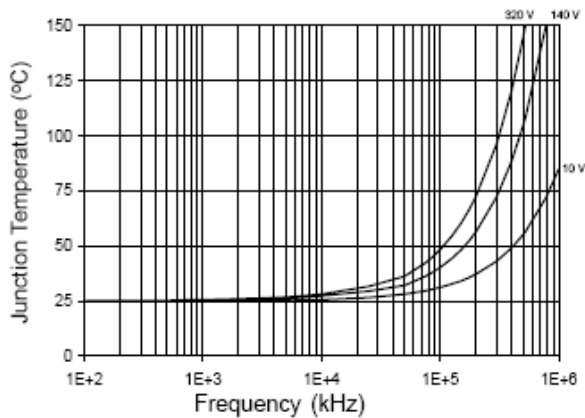
**Figure 30. IRS2110/IRS2113  $T_J$  vs. Frequency (IRFBC40)  $R_{GATE} = 15 \Omega$ ,  $V_{CC} = 15 V$**



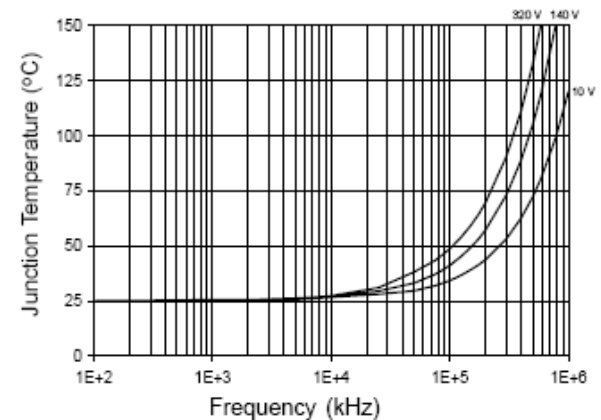
**Figure 31. IRS2110/IRS2113  $T_J$  vs. Frequency (IRFPE50)  $R_{GATE} = 10 \Omega$ ,  $V_{CC} = 15 V$**



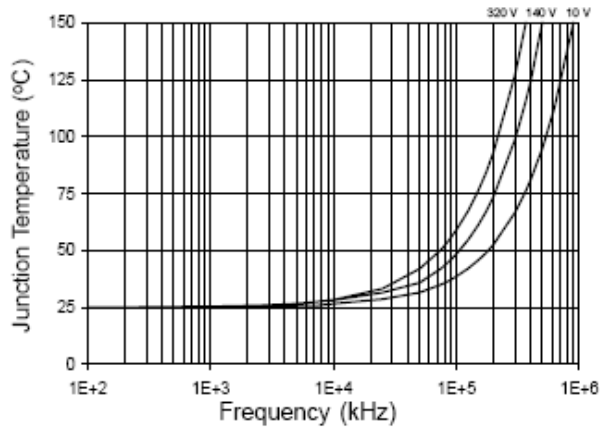
**Figure 32. IRS2110S/IRS2113S  $T_J$  vs. Frequency (IRFBC20)  $R_{GATE} = 33 \Omega$ ,  $V_{CC} = 15 V$**



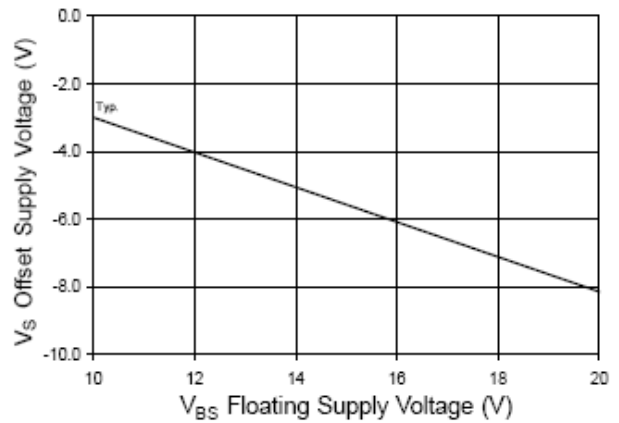
**Figure 33. IRS2110S/IRS2113S  $T_J$  vs. Frequency (IRFBC30)  $R_{GATE} = 22 \Omega$ ,  $V_{CC} = 15 V$**



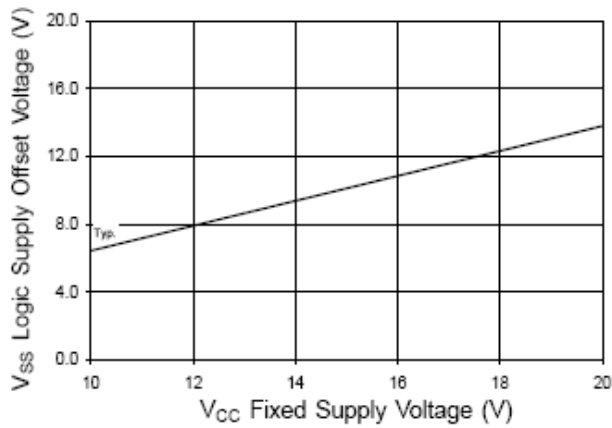
**Figure 34. IRS2110S/IRS2113S  $T_J$  vs. Frequency (IRFBC40)  $R_{GATE} = 15 \Omega$ ,  $V_{CC} = 15 V$**



**Figure 35. IRS2110S/IRS2113S  $T_J$  vs. Frequency (IRFPE50)  $R_{GATE} = 10 \Omega$ ,  $V_{CC} = 15 V$**

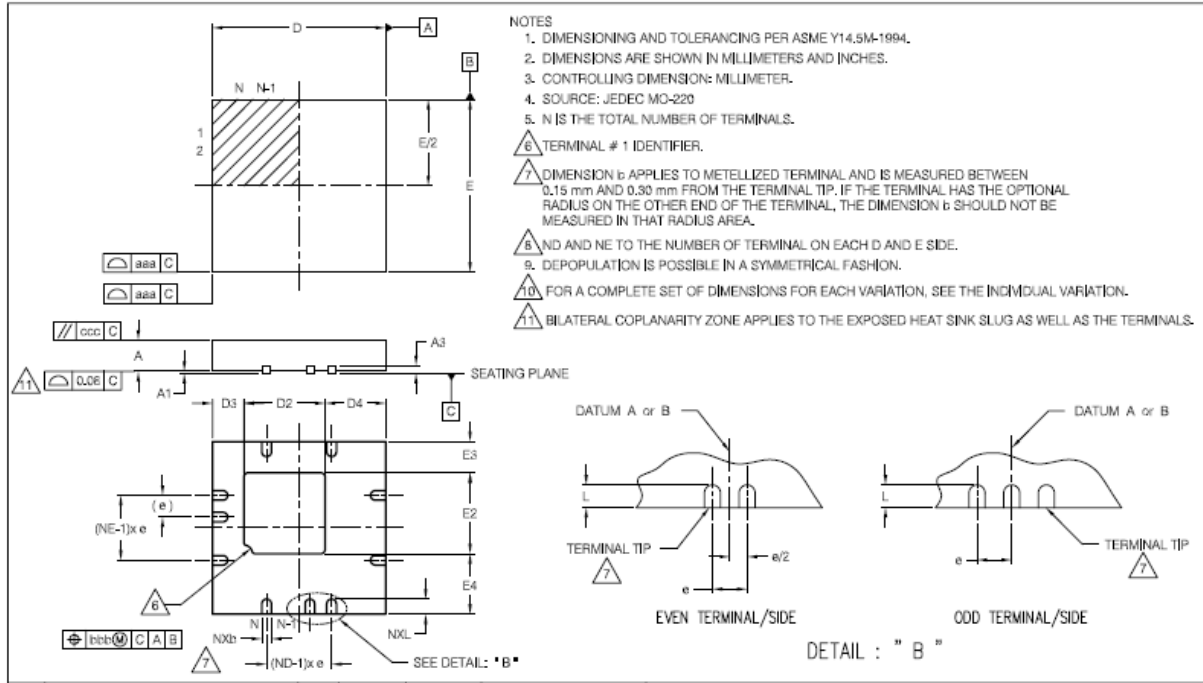


**Figure 36. Maximum  $V_S$  Negative Offset vs.  $V_{BS}$  Supply Voltage**



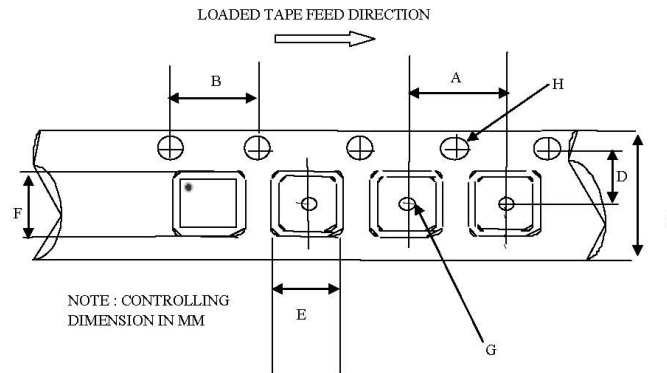
**Figure 37. Maximum  $V_{SS}$  Positive Offset vs.  $V_{CC}$  Supply Voltage**

Package Details: MLPQ 4x4 -16L



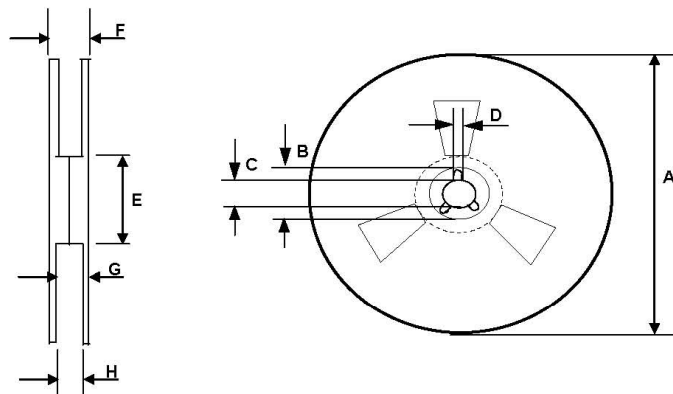
SYMBOL	VGGD-10					
	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	0.90	1.00	.032	.035	.039
A1	0.00	0.02	0.05	.000	.0008	.0019
A3	0.20 REF			.008 REF		
b	0.18	0.25	0.30	.007	.010	.012
D2	1.78	1.88	1.98	.070	.074	.078
D3	0.73 REF			.029 REF		
D4	1.40 REF			.055 REF		
D	4.00 BSC			.157 BSC		
E	4.00 BSC			.157 BSC		
E4	1.40 REF			.055 REF		
E3	0.73 REF			.029 REF		
E2	1.78	1.88	1.98	.070	.074	.078
L	0.30	0.40	0.50	.012	.016	.020
e	0.50 PITCH			.020 PITCH		
N	16			16		
ND	4			4		
NE	4			4		
aaa	0.15			.0059		
bbb	0.10			.0039		
ccc	0.10			.0039		
ddd	0.05			.0019		

**Tape and Reel Details: MLPQ 4x4**



CARRIER TAPE DIMENSION FOR MLPQ4X4V

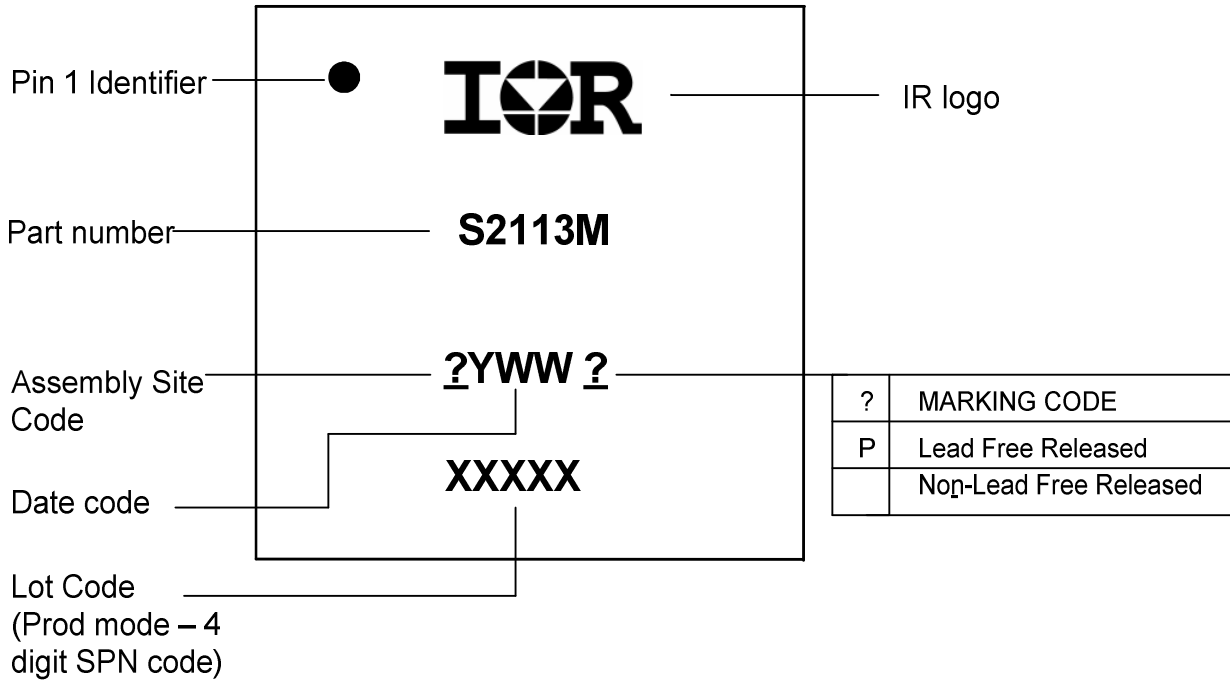
Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.358
B	3.90	4.10	0.154	0.161
C	11.70	12.30	0.461	0.484
D	5.45	5.55	0.215	0.219
E	4.25	4.45	0.168	0.176
F	4.25	4.45	0.168	0.176
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.063



REEL DIMENSIONS FOR MLPQ4X4V

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

**Part Marking Information:**



**Ordering Information**

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
IRS2113	MLPQ 4x4-16L	Tube/Bulk	92	IRS2113MPBF
		<i>Tape and Reel</i>	3,000	IRS2113MTRPBF

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**Revision History**

<b>Date</b>	<b>Comment</b>
09/24/09	Initial conversion from SO package style data sheet
03/24/2010	Included qual info page
08/08/2011	Update the package details
02/08/2012	Update pin assignment drawing
02/08/2023	Add note regarding the exposed pad