NXP Semiconductors
Application Note

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Schematic guidelines for the MMPF0100

1 Introduction

This application note provides guidelines for schematic entry using the MMPF0100. For an example Bill of Materials, refer to the MMPF0100 datasheet.

NXP analog ICs are manufactured using the SMARTMOS process, a combinational BiCMOS manufacturing flow that integrates precision analog, power functions and dense CMOS logic together on a single cost-effective die.

Contents

2 Pin connection guidelines

This section provides recommended pin connections in Table 1. These guidelines help ensure that the MMPF0100 functions properly.

Table 1. MMPF0100 pin connection guidelines

Pin	Pin name	Pin function	Recommended connection	Recommended connection when not used
1	INTB	Open drain interrupt signal to processor	Pull-up via 68 kΩ - 100 kΩ to VSNVS or other rail at voltage less than or equal to V_{IN}	Leave floating
2	SDWNB	Open drain signal to indicate an imminent system shutdown	Pull-up via 68 kΩ - 100 kΩ to VSNVS or other rail at voltage less than or equal to V_{IN}	Leave floating
3	RESETBMCU	Open drain reset output to processor	Pull-up via 68 kΩ - 100 kΩ to VSNVS or other rail at voltage less than or equal to V_{IN}	Leave floating
4	STANDBY	Standby input signal from processor	Connect to PMIC_STBY_REQ signal from processor	Connect to ground
5	ICTEST	Reserved Pin	Connect to ground	Connect to ground

Table 1. MMPF0100 pin connection guidelines (continued)

Pin	Pin name	Pin function	Recommended connection	Recommended connection when not used
6	SW1FB	Output voltage feedback for SW1AB regulator	Connect to SW1AB output voltage rail near load. Leave floating if SW1 is used in SW1ABC Single Phase mode	Leave floating
7	SW1AIN	Input to SW1A MOSFETs for SW1AB regulator	Connect to VIN and bypass with 0.1 µF + 4.7 µF to ground	Connect to VIN
8	SW1ALX	SW1A switching node	Connect to SW1AB inductor when used in SW1AB Single Phase mode. Connect to SW1ABC inductor when used in SW1ABC Single Phase mode. Connect to SW1A inductor when used in SW1AB Dual Phase mode	Leave floating
9	SW1BLX	SW1B switching node	Connect to SW1AB inductor when used in SW1AB Single Phase mode. Connect to SW1ABC inductor when used in SW1ABC Single Phase mode. Connect to SW1B inductor when used in SW1AB Dual Phase mode	Leave floating
10	SW1BIN	Input to SW1B MOSFETs for SW1AB regulator	Connect to VIN and bypass with 0.1 µF + 4.7 µF to ground	Connect to VIN
11	SW1CLX	Regulator SW1C switching node	Connect to SW1C Inductor when SW1C is used as an independent regulator. Connect SW1ALX, SW1BLX, and SW1CLX together when SW1 is used in SW1ABC Single Phase mode	Leave floating
12	SW1CIN	Input to SW1C regulator	Connect to VIN and bypass with 0.1 µF + 4.7 µF to ground	Connect to VIN
13	SW1CFB	Output voltage feedback for SW1C Independent and SW1ABC Single Phase configurations	Connect to SW1C output voltage rail near load. Connect to SW1ABC output voltage rail if SW1ABC Single Phase configuration is used	Leave floating
14	SW1VSSSNS	Ground reference for SW1 regulator(s)	Connect to ground. Keep away from high current ground return paths.	N/A
15	GNDREF1	Ground reference for regulators SW2 and SW4	Connect to ground. Keep away from high current ground return paths.	N/A
16	VGEN1	VGEN1 regulator output	Bypass with 2.2 µF to ground	Leave floating
17	VIN1	VGEN1 and VGEN2 LDO regulators' input supply	Bypass with 1.0 µF capacitor to ground	Connect to output of a regulator with voltage <3.4 V
18	VGEN2	VGEN2 regulator output	Bypass with 4.7 µF to ground	Leave floating
19	SW4FB	Output voltage feedback for SW4	Connect to SW4 output voltage rail near load	Leave floating
20	SW4IN	Input to SW4 regulator	Connect to VIN and bypass with 0.1 µF + 4.7 µF to ground	Connect to VIN
21	SW4LX	SW4 switching node	Connect to SW4 inductor	Leave floating
22	SW2LX	SW2 switching node	Connect to SW2 inductor	Leave floating
23	SW2IN	Input to SW2 regulator	Connect to VIN and bypass with 0.1 µF + 4.7 µF to ground. Connect pins 23 and 24 together.	Connect to VIN
24	SW2IN	Input to SW2 regulator		Connect to pin 23
25	SW2FB	Output voltage feedback for SW2	Connect to SW2 output voltage rail near load	Leave floating
26	VGEN3	VGEN3 regulator output	Bypass with 2.2 µF to ground	Leave floating

Table 1. MMPF0100 pin connection guidelines (continued)

Pin	Pin name	Pin function	Recommended connection	Recommended connection when not used
27	VIN2	VGEN3 and VGEN4 LDO regulators' input	Bypass with 1.0 µF capacitor to ground	Connect to regulator with output voltage <3.6 V
28	VGEN4	VGEN4 regulator output	Bypass with 4.7 µF to ground	Leave floating
29	VHALF	Half supply reference for VREFDDR	Bypass with 0.1 µF to ground	Leave floating
30	VINREFDDR	VREFDDR regulator input	Connect 0.1.0 µF to VHALF pin. Ensure there is at least 1.0 µF net capacitance from VINREFDDR to ground	Leave floating
31	VREFDDR	VREFDDR regulator output	Bypass with 1.0 µF to ground	Leave floating
32	SW3VSSSNS	Ground reference for SW3 regulator(s)	Connect to ground. Keep away from high current ground return paths.	N/A
33	SW3BFB	Output voltage feedback for SW3B regulator	Leave floating when SW3 is used in SW3AB Single Phase mode. Connect to SW3B output voltage rail near load if SW3 is used in independent mode	Leave floating
34	SW3BIN	Input to SW3B regulator	Connect to VIN and bypass with 0.1 µF + 4.7 µF to ground	Connect to VIN
35	SW3BLX	SW3B switching node	Connect to SW3AB inductor if SW3 is used in Single Phase mode. Connect to SW3B inductor if SW3 is used in independent mode.	Leave floating
36	SW3ALX	SW3A switching node	Connect to SW3AB inductor if SW3 is used in Single Phase mode. Connect to SW3A inductor if SW3 is used in independent mode.	Leave floating
37	SW3AIN	Input to SW3A regulator	Connect to VIN and bypass with 0.1 µF + 4.7 µF to ground	Connect to VIN
38	SW3AFB	Output voltage feedback for SW3A or SW3AB regulators	Connect to SW3A(B) output voltage rail near load	Leave floating
39	VGEN5	VGEN5 regulator output	Bypass with 2.2 µF to ground	Leave floating
40	VIN3	VGEN5 and VGEN6 LDO regulators' input	Bypass with 1.0 µF capacitor to ground	Connect to VIN
41	VGEN6	VGEN6 regulator output	Bypass with 2.2 µF to ground	Leave floating
42	LICELL	Coin cell supply input/output	Bypass with 0.1 µF capacitor. Connect to optional coin cell.	Bypass with 0.1 µF
43	VSNVS	VSNVS regulator/switch output	Bypass with 0.47 µF to ground	Bypass with 0.47 µF to ground
44	SWBSTFB	SWBST regulator output voltage feedback	Connect to SWBST output voltage rail near load	Leave floating
45	SWBSTIN	Input to SWBST regulator	Connect to VIN and bypass with 0.1 µF + 10 µF to ground	Connect to VIN
46	SWBSTLX	SWBST switch node connection	Connect to SWBST inductor and Schottky diode	Leave floating
47	VDDOTP	Supply to program OTP fuses	Connect to VCOREDIG through a 100 kΩ resistor if PF0100 is used in the default mode. Connect to ground if PF0100 is used in the fuse mode. If on-board programming is desired, give provision to apply 8.0 V programming voltage to the pin with bypass of 2x10 µF capacitors	N/A

Table 1. MMPF0100 pin connection guidelines (continued)

Pin	Pin name	Pin function	Recommended connection	Recommended connection when not used
48	GNDREF1	Ground reference for the main band gap regulator.	Connect to ground. Keep away from high current ground return paths.	N/A
49	VCORE	Analog Core supply	Bypass with 1.0 µF to ground	N/A
50	VIN	Main chip supply	Bypass with 1.0 µF to ground	N/A
51	VCOREDIG	Digital Core supply	Bypass with 1.0 µF to ground	N/A
52	VCOREREF	Main band gap reference	Bypass with 0.22 µF to ground	N/A
53	SDA	I^2C data line	Pull-up to VDDIO	Leave floating
54	SCL	I^2C clock line	Pull-up to VDDIO	Leave floating
55	VDDIO	Supply for I^2C bus	Connect to 1.7 to 3.6 V supply. Bypass with 0.1 µF to ground. Ensure that VDDIO is always lesser than or equal to VIN.	Leave floating
56	PWRON	Power On/off from processor	Connect to PMIC_ON_REQ from processor. Pull up via 8 kΩ - 100 kΩ to VSNVS if required	N/A
-	EP	Expose pad. Functions as ground return for buck and boost regulators	Ground. Connect this pad to the inner and external ground planes through multiple vias to allow effective thermal dissipation.	N/A

3 References

Document number and description		URL
MMPF0100	Data Sheet	http://www.nxp.com/files/analog/doc/data_sheet/MMPF0100.pdf
AN1902	QFN (Quad Flat Pack No-Lead) Application Note	http://www.nxp.com/files/analog/doc/app_note/AN1902.pdf
AN4622	MMPF0100 Layout Guidelines	http://www.nxp.com/files/analog/doc/app_note/AN4622.pdf
Support Pages		**URL**
MMPF0100 Product Summary Page		http://www.nxp.com/webapp/sps/site/prod_summary.jsp?code=MMPF0100
Power Management Home Page		http://www.nxp.com/webapp/sps/site/homepage.jsp?code=POWERMGTHOME
Analog Home Page		http://www.nxp.com/analog

4 Revision history

Revision	Date	Description of changes
2.0	5/2013	• Initial release
3.0	6/2015	• Replaced AN4530 by AN1902
	7/2016	• Updated to NXP document form and style

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