PCN Number:	20170801000	PCN Date:	August 08, 2017
Title:	Datasheet for DAC38RF86, DAC38RF96, DAC38RF87, and DAC38RF97		
Customer Contact:	PCN Manager	Dept:	Quality Services

Change Type:

☐	Assembly Site	☐	Design	☐	Wafer Bump Site
☐	Assembly Process	☒	Data Sheet	☐	Wafer Bump Material
☐	Assembly Materials	☐	Part number change	☐	Wafer Bump Process
☐	Mechanical Specification	☐	Test Site	☐	Wafer Fab Site
☐	Packing/Shipping/Labeling	☐	Test Process	☐	Wafer Fab Materials
				☐	Wafer Fab Process

Notification Details

Description of Change:

Texas Instruments Incorporated is announcing an information only notification.
The product datasheet(s) is being updated as summarized below.
The following change history provides further details.

TEXAS INSTRUMENTS

DAC38RF86, DAC38RF96
DAC38RF87, DAC38RF97

SLASEF4B – FEBRUARY 2017 – REVISED JULY 2017

Changes from Revision A (April 2017) to Revision B **Page**

- Changed the *Description* ... 1
- Changed the *Device Information* table ... 1
- Changed From: alarm_out_pol To: alm_out_pol in ALARM pin description in the *Pin Functions* table ... 7
- Changed the Description of pins A3, A4, A7, A6, A9, A10, A12, F11, F7, G6, G12, H5, H7, J6, J11 in the *Pin Functions* table ... 7
- Added description to TXENABLE pin in the *Pin Functions* table ... 8
- Changed the MAX value of VEE18N rail in the *Absolute Maximum Ratings* From: 0.5 V To: 0.3 V ... 9
- Added "Supply Voltage Range" to the *Recommended Operating Conditions* table ... 9
- Added "Reference voltage drift" to the *Electrical Characteristics - DC Specifications* table ... 10
- Added Isolation vs Output Frequency plot in Figure 14 ... 22
- Added Isolation vs output frequency plot for DAC38RF87/97 in Figure 30 ... 26
- Changed the MPY values in Table 4 ... 31
- Added MPY value for 16.5x to Table 4 ... 31
- Changed x To: √ in the *JESD204B Formats for DAC38RFxx* table ... 34
- Changed JESD204B frame format for LMFSHd=84111 in Table 12 ... 35
- Changed JESD204B frame format for LMFSHd=44210 in Table 14 ... 36
- Changed JESD204B frame format for LMFSHd=24410 in Table 16 ... 36
- Changed JESD204B frame format for LMFSHd=44210 in Table 17 ... 36
- Changed JESD204B frame format for LMFSHd=88210 in Table 18 ... 37
- Changed JESD204B frame format for LMFSHd=24410 in Table 19 ... 37
- Changed JESD204B frame format for LMFSHd=48410 in Table 20 ... 37
- Changed JESD204B frame format for LMFSHd=24310 in Table 21 ... 37
- Changed JESD204B frame format for LMFSHd=48310 in Table 22 ... 37
- Changed Table 33 ... 50
- Changed register field programming values for LMFSHd=24410 and 24310 in Table 36 ... 55
- Changed the bit positions of N_M1 register field in Table 37 ... 55
- Changed the bit positions of N_M1' N_M1' (NPRIME_M1) register field in Table 37 ... 55
- Deleted ISFIRCD_ENA and ISFIR_AB regsiter fields. Added ISFIR_ENA register field in *Inverse Sinc Filter* ... 57
- Changed the description of DAC PLL alarm in *Alarm Monitoring* ... 60
- Changed from BIST_ENA to Reserved in Table 56 ... 80
- Changed from BIST_ZERO to Reserved in Table 56 ... 80
- Changed the description of OUTSUM_SEL field in Table 64 ... 86
- Changed the junction temp and loop filter voltage range for PLL tuning in Figure 150 ... 130

Changes from Original (February 2017) to Revision A **Page**

- Changed the Title From: "Dual- or Single-Channel, Single-Ended, 14-bit, 9-GSPS,.." To: Dual-Channel, Single-Ended, 14-bit, 6 & 9-GSPS,..." 1
- Changed the Description of SYSREF+ From: "LVPECL SYSREF positive input." To: "LVPECL SYSREF positive input, self biased." in the *Pin Functions* table 8
- Deleted Latency and PLL/VCO parameters from the end of the *Electrical Characteristics - DC Specifications* table 15
- Changed the *Electrical Characteristics - AC Specifications* table, and added "0 dBFS" amplitude of input digital data in test conditions 16
- Added the *PLL/VCO Electrical Characteristics* table 19
- Added JESD204B clock phase register setting to Table 36 55
- Removed descriptions for CLKJESD_DIV register from Table 36 55
- Added JESD204B clock phase register setting to Table 37 55
- Added information about the DAC output total current for various full scale current settings in *DAC Fullscale Output Current* 62
- Changed Table 125 125
- Changed description of SERDES_REFCLK_DIV register field in Table 126 126
- Changed Bit 12:11, 6:5 and 4:2 of Table 129 128

The datasheet number will be changing.

Device Family	Change From:	Change To:
DAC38RF86, DAC38RF96, DAC38RF87, and DAC38RF97	SLASEF4	SLASEF4B

These changes may be reviewed at the datasheet links provided.

http://www.ti.com/product/DAC38RF86

Reason for Change:

To accurately reflect device characteristics.

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

No anticipated impact. This is a specification change announcement only. There are no changes to the actual device.

Changes to product identification resulting from this PCN:

None.

Product Affected:

DAC38RF86IAAV	DAC38RF86IAAVR	DAC38RF87IAAV	DAC38RF87IAAVR
DAC38RF96IAAV	DAC38RF96IAAVR	DAC38RF97IAAV	DAC38RF97IAAVR

For questions regarding this notice, e-mails can be sent to the regional contacts shown below or your local Field Sales Representative.

Location	E-Mail
USA	PCNAmericasContact@list.ti.com
Europe	PCNEuropeContact@list.ti.com
Asia Pacific	PCNAsiaContact@list.ti.com
Japan	PCNJapanContact@list.ti.com