



## Customer Information Notification

2021040511 : i.MX 8M Dual/8M QuadLite/8M Quad Consumer and Industrial Datasheet Update to Rev.3 and Reference Manual Update to Rev.3.1

**Note:** This notice is NXP Company Proprietary.

**Issue Date:** Jul 08, 2021 **Effective date:** Jul 09, 2021

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## PCN Overview

### Description

NXP Semiconductors announces Industrial and Consumer Datasheet (DS) update for i.MX 8M Dual/8M QuadLite/8M Quad to revision 3 and Reference Manual (RM) update for i.MX 8M Dual/8M QuadLite/8M Quad to revision 3.1. The revision history included in the updated document provides a detailed description of the changes.

Industrial and Consumer Datasheet Changes Summary:

Highlighted Changes:

- Updated the descriptions of PCIE\_VPH in the Table 8, "Operating ranges"

Please refer the change summary for other changes.

The i.MX 8M Dual/8M QuadLite/8M Quad Industrial and Consumer Datasheet Rev.3 are attached to this notice, and can be found at:

<https://www.nxp.com/docs/en/data-sheet/IMX8MDQLQIEC.pdf>

<https://www.nxp.com/docs/en/data-sheet/IMX8MDQLQCEC.pdf>

Reference Manual Changes Summary:

- Updated the description of field 12 "PCIE1\_VREG\_BYPASS" in 8.2.4.15 GPR14 General Purpose Register (IOMUXC\_GPR\_GPR14)
- Updated the description of field 12 "PCIE2\_VREG\_BYPASS" in 8.2.4.17 GPR16 General Purpose Register (IOMUXC\_GPR\_GPR16)

- Chapter 11.4 PCIe Express PHY (PCIe\_PHY) previously was an incorrect version of the spec and now has been updated with the correct version.

The i.MX 8M Dual/8M QuadLite/8M Quad Reference Manual Rev.3.1 is attached to this notice, and can be found at:

<https://www.nxp.com/docs/en/reference-manual/IMX8MDQLQRM.pdf>

Software patches are provided along with this DS and RM change, which can be found at:  
<https://community.nxp.com/t5/i-MX-Processors-Knowledge-Base/i-MX-8M-Dual-8M-QuadLite-8M-Quad-Incorrect-PCIE-Supply/ta-p/1299599>

#### **Reason**

Datasheet and Reference Manual have been updated to correct errors and provide additional technical clarification on some device features. Below are the details:

The PCIe\_VPH power supply is selectable in software between 1.8V and 3.3V. When the PCIe\_VPH supply is configured to operate at 3.3V, the 1.8V internal regulator (disabled by default) must be enabled to prevent overstress conditions on the PCIe PHY. If the 1.8V internal regulator is left disabled when the PCIe\_VPH supply is configured to operate at 3.3V, it could potentially affect reliability or cause permanent damage to the device. This impacts i.MX 8M NXP reference designs and/or customer design if PCIe\_VPH is supplied with 3.3V and the internal 1.8V regulator is disabled.

3 software patches for each release are provided as per this DS and RM change to enable the 1.8V regulator by default, and they have already been included in L5.4.70\_2.3.2 and later releases. NXP recommends to check the HW design for PCIe\_VPH supply and configuration.

#### **Identification of Affected Products**

Product identification does not change

#### **Anticipated Impact on Form, Fit, Function, Reliability or Quality**

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When PCIe\_VPH is supplied with 3.3V, the internal 1.8V regulator must be enabled through software configuration otherwise it will lead to overstress and could potentially affect reliability or cause permanent damage to the device.

#### **Data Sheet Revision**

A new datasheet will be issued

#### **Contact and Support**

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<b>Affected OPN</b>	<b>12NC</b>
MIMX8MQ5CVAHZAA	935358612557
MIMX8MQ5DVAJZAA	935358613557
MIMX8MQ5DVAJZAB	93537777557
MIMX8MQ6CVAHZAA	935358614557
MIMX8MQ6CVAHZAB	935377778557
MIMX8MQ6DVAJZAA	935358615557
MIMX8MQ6DVAJZAB	935377779557
MIMX8MQ6DVAJZIB	935395873557
MIMX8MQ6DVAJZJB	935395827557
MIMX8MQ7CVAHZAA	935358616557
MIMX8MQ7CVAHZAB	935377784557
MIMX8MQ7DVAJZAA	935358617557
MIMX8MQ7DVAJZAB	935377785557
MIMX8MD6CVAHZAA	935358607557
MIMX8MD6CVAHZAB	935377781557
MIMX8MD6DVAJZAA	935358608557
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MIMX8MD7DVAJZAB	935377783557
MIMX8MQ5CVAHZAB	93537776557