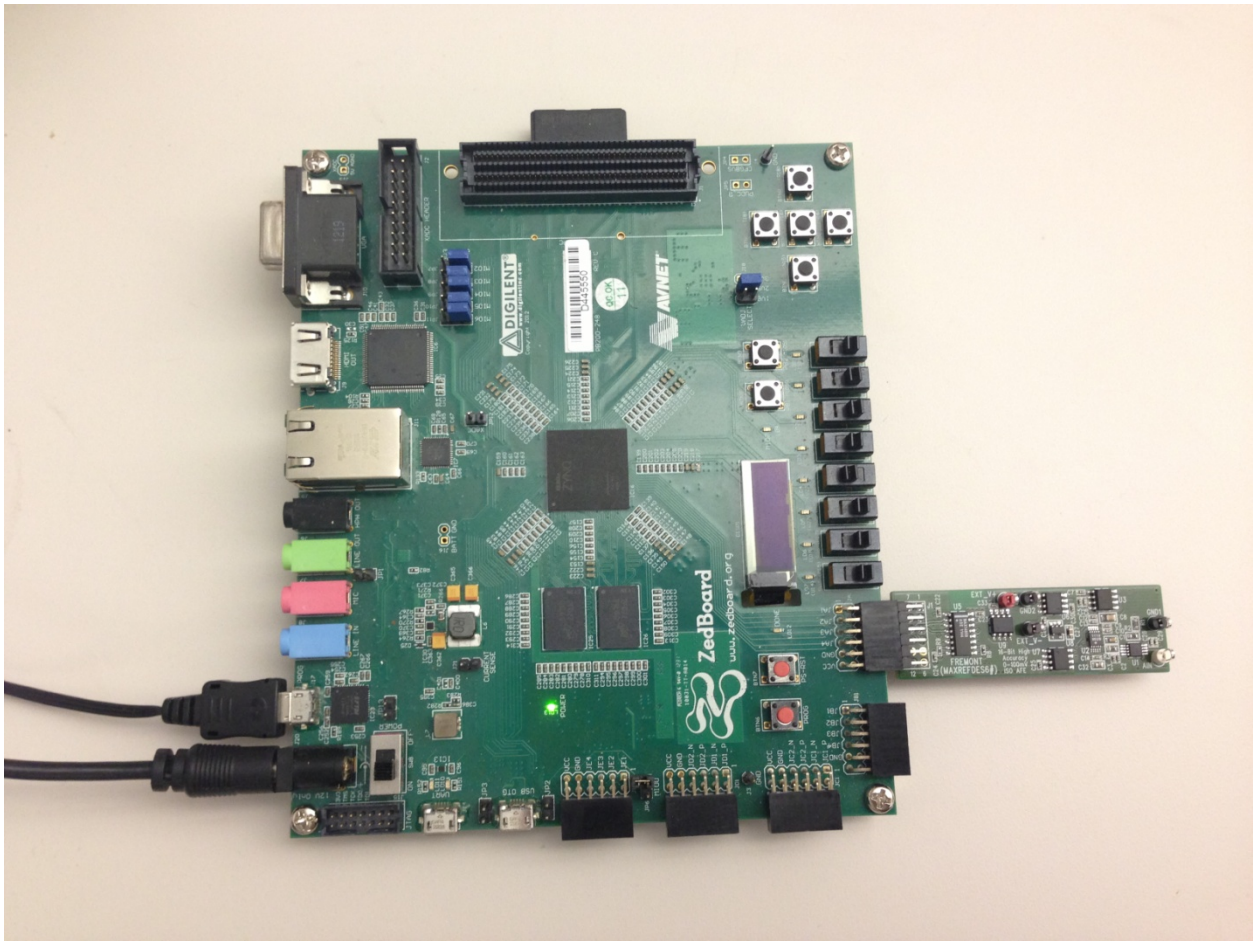
# Fremont (MAXREFDES6#) ZedBoard Quick Start Guide

***Rev 0; 9/13***



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## 1. Required Equipment

- PC with Windows® OS with Xilinx® ISE®/SDK version 14.2 or later and two USB ports (Refer to Xilinx AR# 51895 if you installed ISE WebPack™ design software on your PC.)
- One +7V power supply
- One -6V power supply
- License for Xilinx EDK/SDK version 14.2 or later (free WebPack license is OK)
- Fremont (MAXREFDES6#) board
- ZedBoard™ development kit
- Industrial sensor or signal source

## 2. Overview

Below is a high-level overview of the steps required to quickly get the Fremont design running by downloading and running the FPGA project. Detailed instructions for each step are provided in the following pages. **The Fremont (MAXREFDES6#) subsystem reference design will be referred to as Fremont throughout this document.**

1) Connect the Fremont board to the JA1 port of a ZedBoard as shown in Figure 1. Ensure the connector is aligned as shown in Figure 2.
2) Download the latest **RD6V01_00.ZIP** file located at the Fremont page.
3) Extract the **RD6V01_00.ZIP** file to a directory on your PC.
4) Open the Xilinx SDK.
5) Download the bitstream (.BIT) file to the board. This bitstream contains the FPGA hardware design and software bootloader.
6) Use Xilinx SDK to download and run the executable file (.ELF) on one of the two ARM® Cortex™-A9 processors.

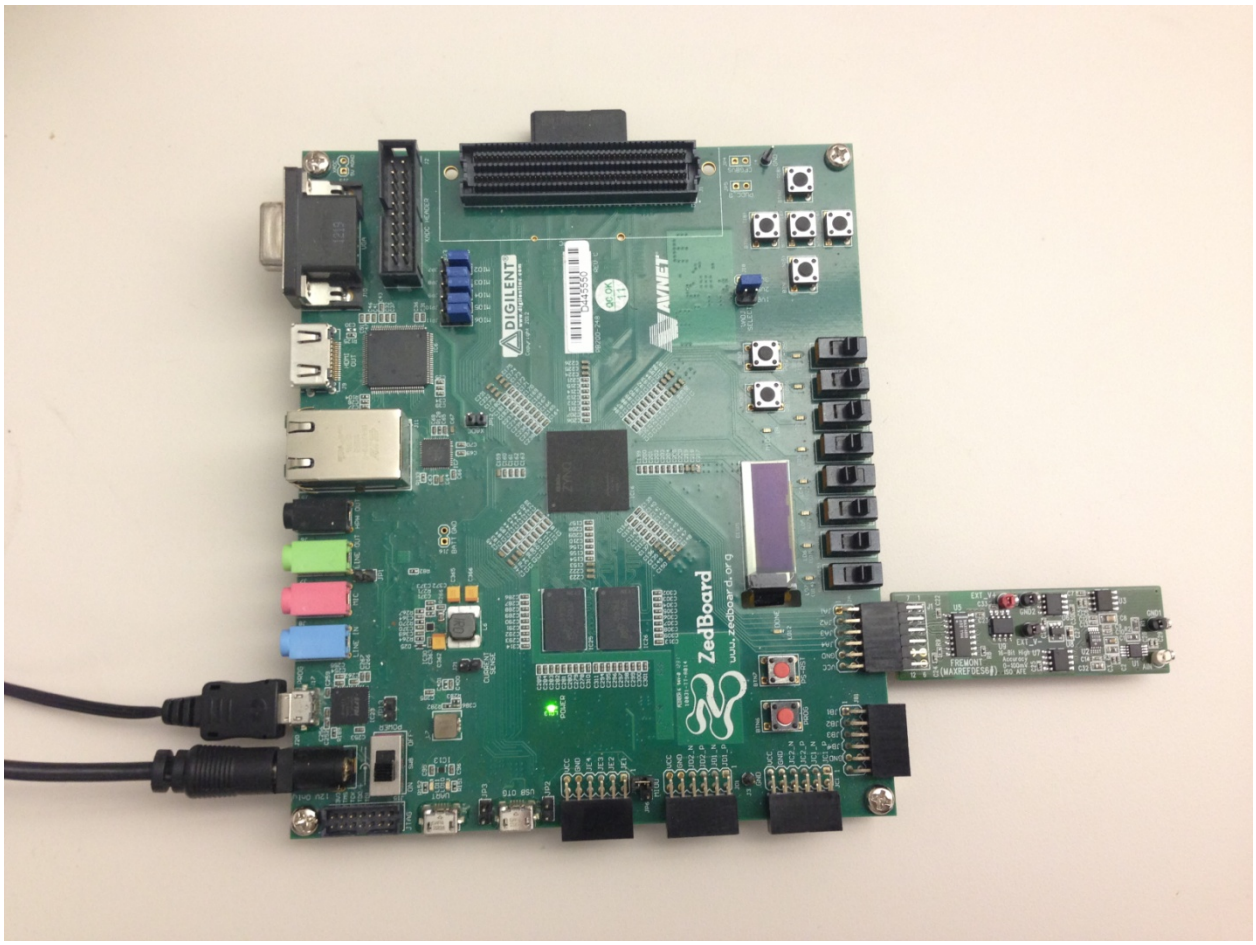



**Figure 1. Fremont Board Connected to ZedBoard Kit**

**Figure 2. Pmod™ Connector Alignment**

## 3. Included Files

The top level of the hardware design is a Xilinx PlanAhead Project (.PRR) for Xilinx PlanAhead version 14.2. The Verilog-based arm_system_stub.v module provides FPGA/board net connectivity, and instantiates the wrapper that carries both the Zynq® Processing System and AXI_MAX11100 custom IP core that interface to the Pmod port. This is supplied as a Xilinx software development kit (SDK) project that includes a demonstration software application to evaluate the Fremont subsystem reference design. The lower level c-code driver routines are portable to the user's own software project.

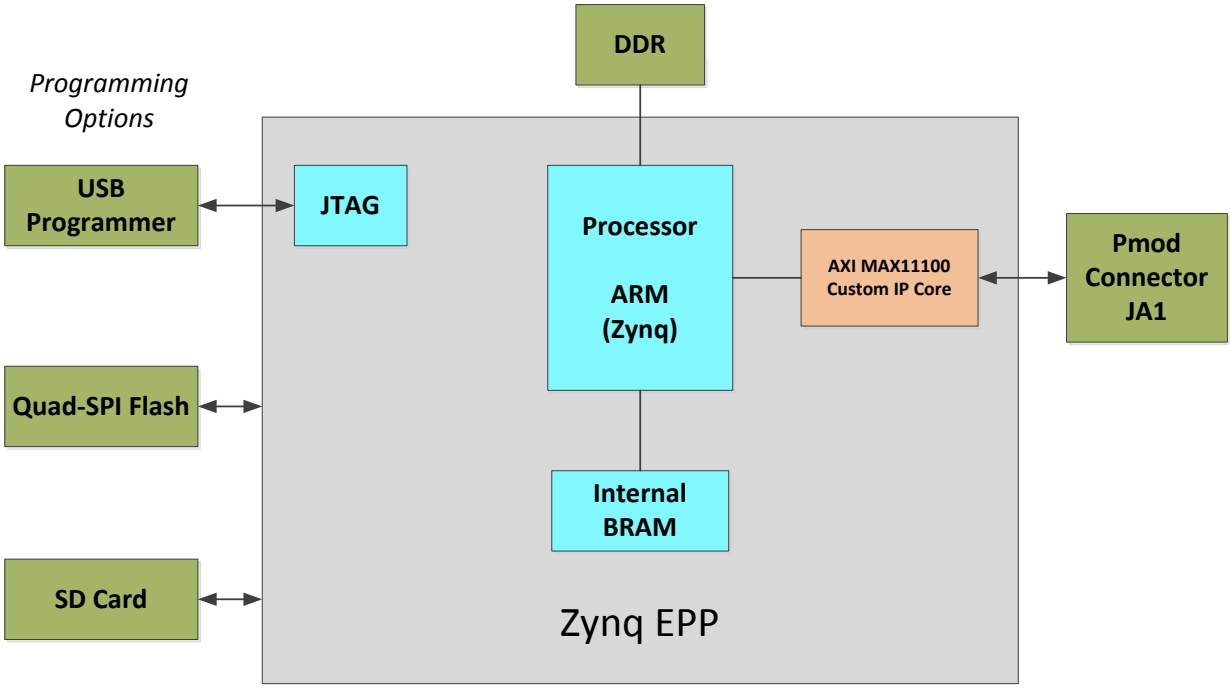



**Figure 3. Block Diagram of FPGA Hardware Design**

# 4. Procedure

1. Connect the Fremont board to the JA1 port of a ZedBoard as shown in Figure 1.

2. Power up the ZedBoard by sliding the SW8 switch on the ZedBoard to the ON position.

3. Download the latest **RD6V01_00.ZIP** file at **www.maximintegrated.com/fremont**. All files available for download are available at the bottom of the page.

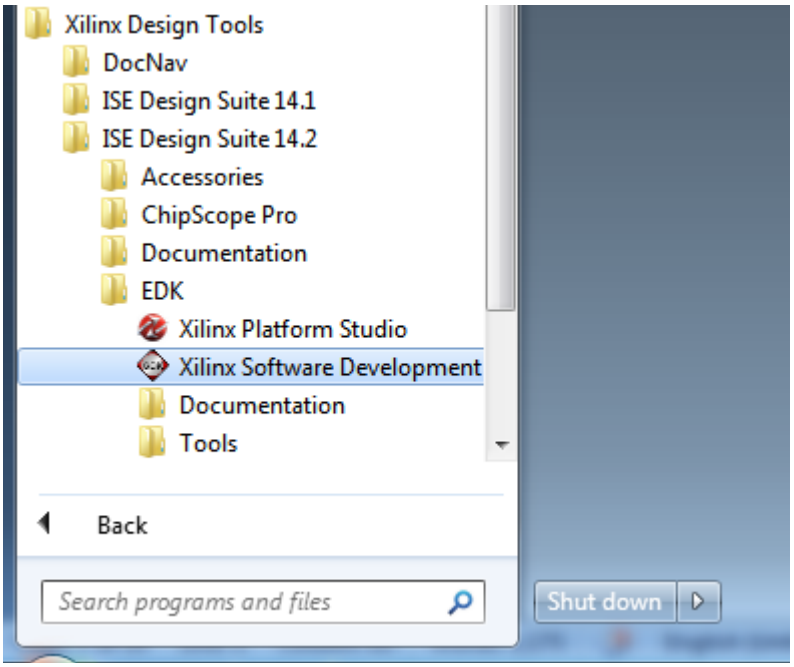
4. Extract the **RD6V01_00.ZIP** file to a directory on your PC. The location is arbitrary but the maximum path length limitation in Windows (260 characters) should not be exceeded.

   In addition, the Xilinx tools require the path to not contain any spaces.

   **C:\Do Not Use Spaces In The Path\RD6V01_00.ZIP**
   **(This path has spaces.)**

   For the purposes of this document, it will be **C:\designs\maxim\RD6V01_00**. See **Appendix A: Project Structure and Key Filenames** in this document for the project structure and key filenames.

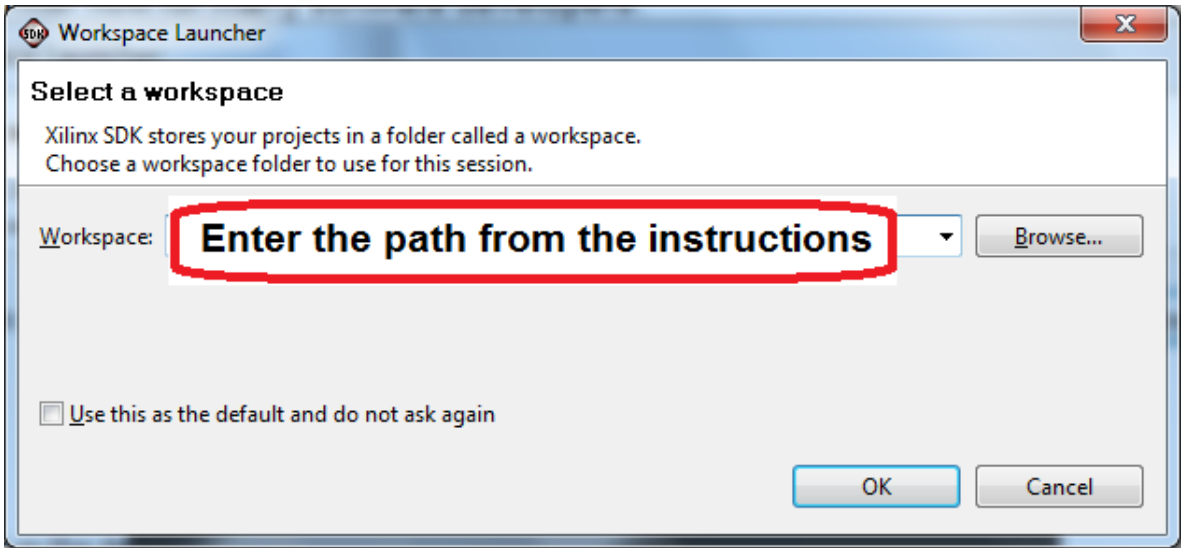
5. Open the **Xilinx Software Development Kit (SDK)** from the Windows **Start** menu.



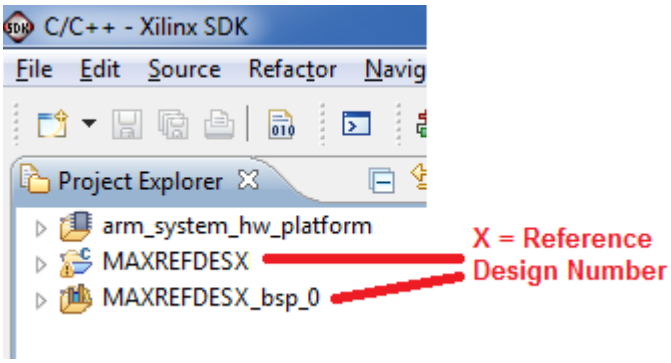

6. SDK will prompt for a workspace directory, which is the location where the software project is located. For this example, it is:

**C:\designs\maxim\RD6V01_00\RD6_ZED_V01_00\Design_Files\top.sdk\SDK\SDK_Export**

Click **OK** and SDK will open. The Xilinx SDK is based on an Eclipse™-based IDE, so it will be a familiar flow for many software developers.



7. Review the SDK IDE. The **Project Explorer** in the upper left tab should have three components as shown in the image below. If all three subfolders are present, you can skip the next step.

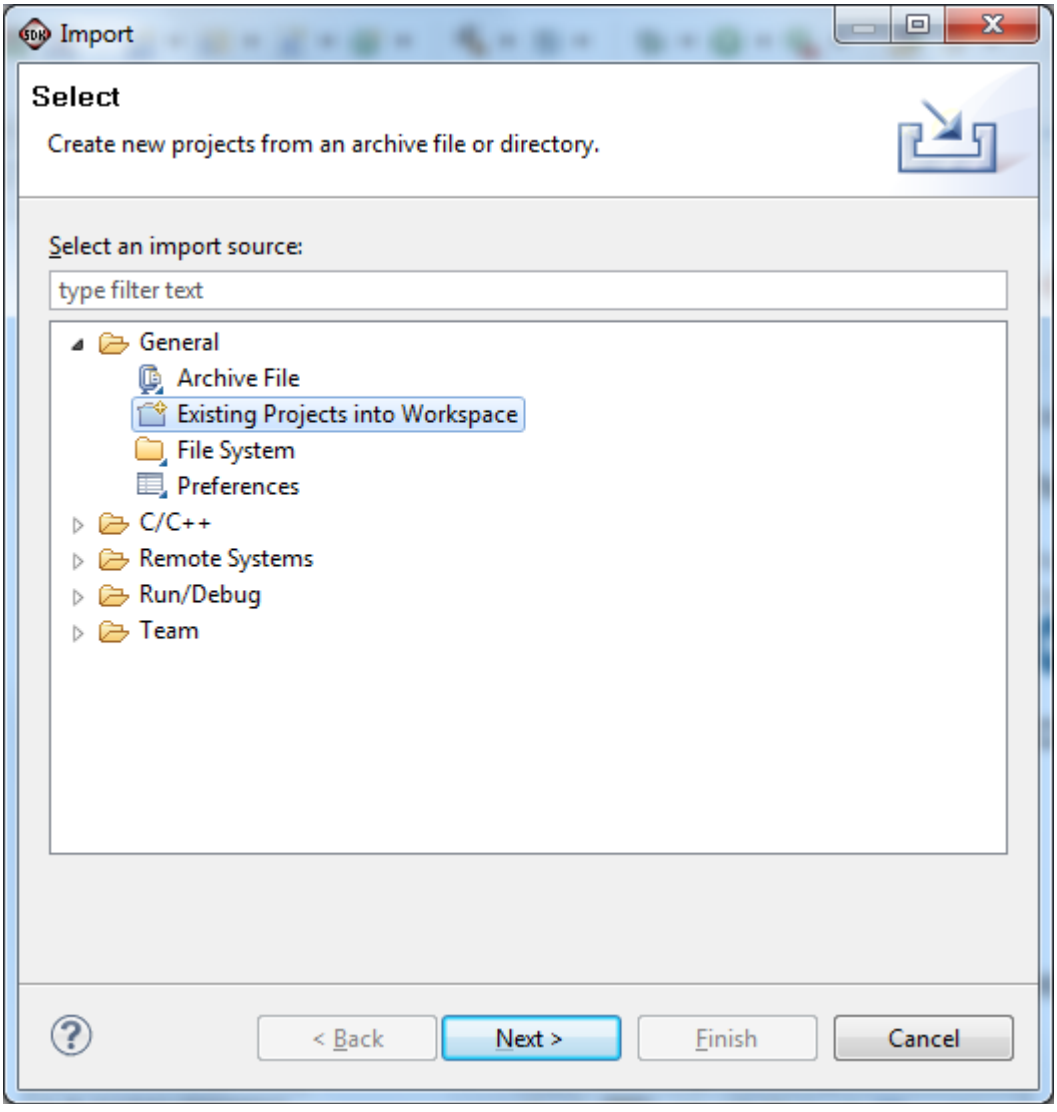


8. If the **Project Explorer** does not contain these three subfolders, launch the **File | Import** menu, expand the **General** folder, and select **Existing Projects into Workspace**. Click **Next**. Set the root directory to:

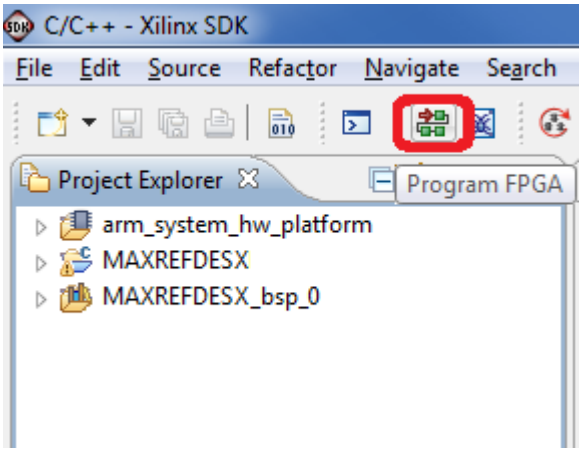
   **C:\designs\maxim\RD6V01_00\RD6_ZED_V01_00\Design_Files\top.sdk\SDK\SDK_Export**

   and the missing projects should appear in SDK **Project Explorer** with their checkboxes checked.

   Click **Finish** to import the projects.



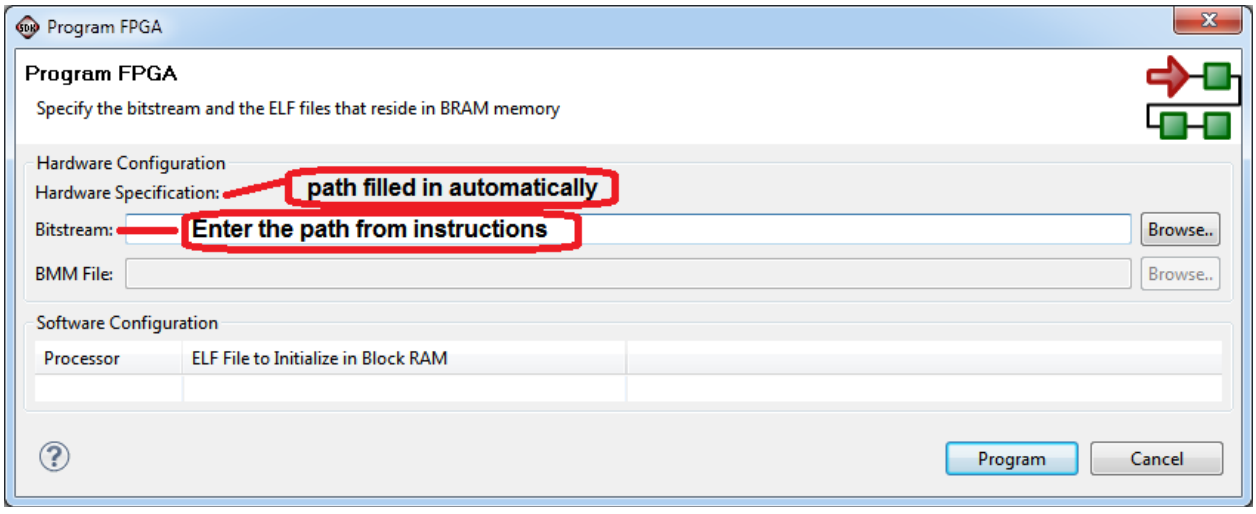
9. To download the bitstream (.BIT) file to the board, click on the **Program FPGA** icon (which looks like a green chain of devices).




The **Program FPGA** dialog box appears. From here, an FPGA bitstream (.BIT) file is selected. Be sure to select the .BIT file by using the paths below.

Bitstream:
**C:\designs\maxim\RD6V01_00\RD6_ZED_V01_00\Design_Files\top.sdk\SDK\SDK_Export\arm_system_hw_platform**

Press **Program**.




It takes approximately 10 seconds to download the FPGA, then a message box indicating **FPGA configuration complete** appears.

10. Setup of the terminal program to run on the PC using the following steps. Before loading the executable firmware file on the FPGA, the terminal program on the PC should be running. The example firmware running on the FPGA communicates with the PC via a USB port set up to emulate a serial port (UART). To establish this communication link, the PC must be configured with the appropriate Windows drivers. A suitable terminal program such as Tera Term or HyperTerminal should be invoked.

    The ZedBoard utilizes the Cypress USB-UART bridge IC. If the Windows cannot automatically install the driver for the Cypress USB-UART bridge IC, the driver is available for download from (http://www.cypress.com/?rID=63794). The driver is WHQL certified for the default Cypress VID / PID of 0x04B4 / 0x0008.

    Once installed, Windows will assign a previously unused COM port. Use the Windows **Control Panel | System | Device Manager** to determine the COM port number. (It will be named Cypress Serial.) Make a note of which COM port this is. That information is needed in the next step.

    Next, a terminal emulation program needs to be installed and launched. For Windows XP® and earlier systems, the HyperTerminal program is the usual choice. However, since HyperTerminal was eliminated from Windows 7, it may be necessary to locate an alternative. Several are available; one good choice is called Tera Term (http://ttssh2.sourceforge.jp/). Whatever terminal program you choose, the communication should be set up by opening the COM port number previously described above and the port configured as:

    bits per second: **460,800**;

    data bits: **8**;

    parity: **none**;

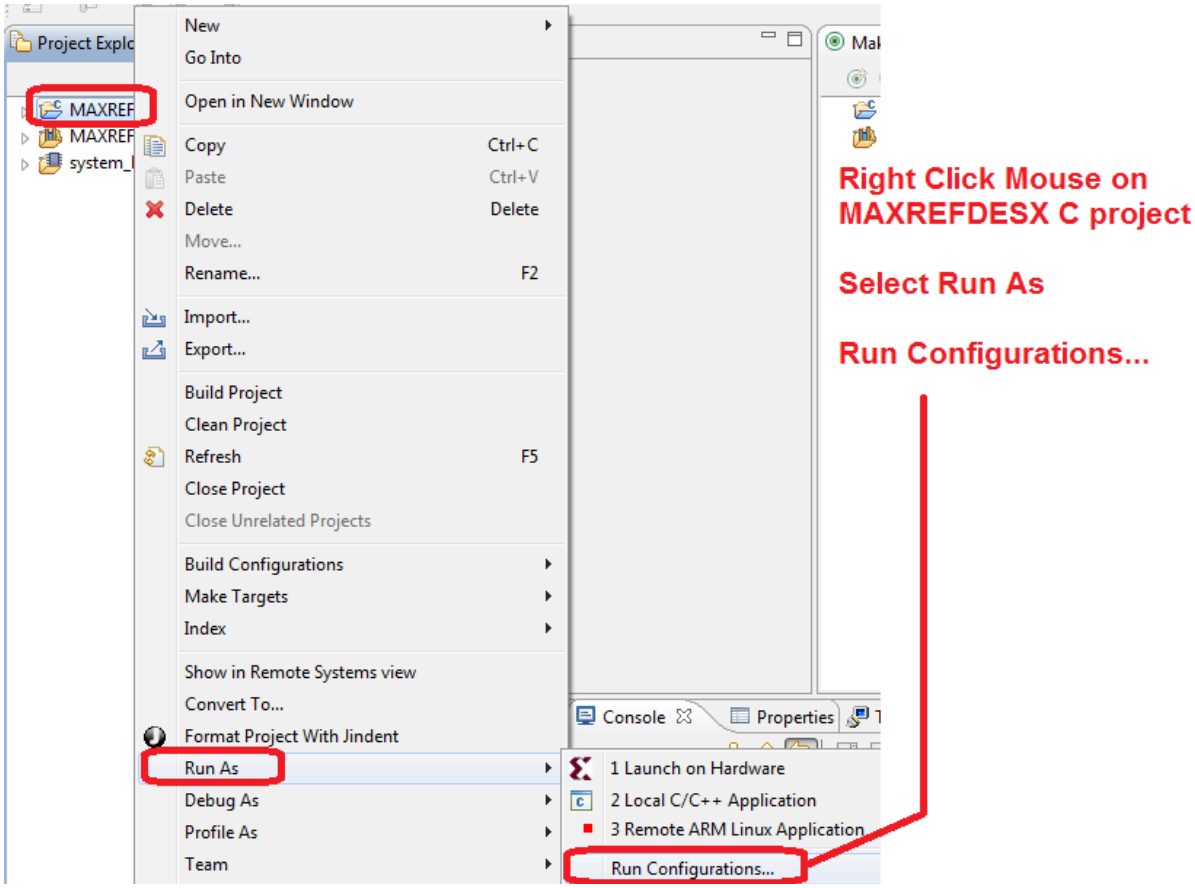
    stop bits: **1**;

    flow control: **none**.

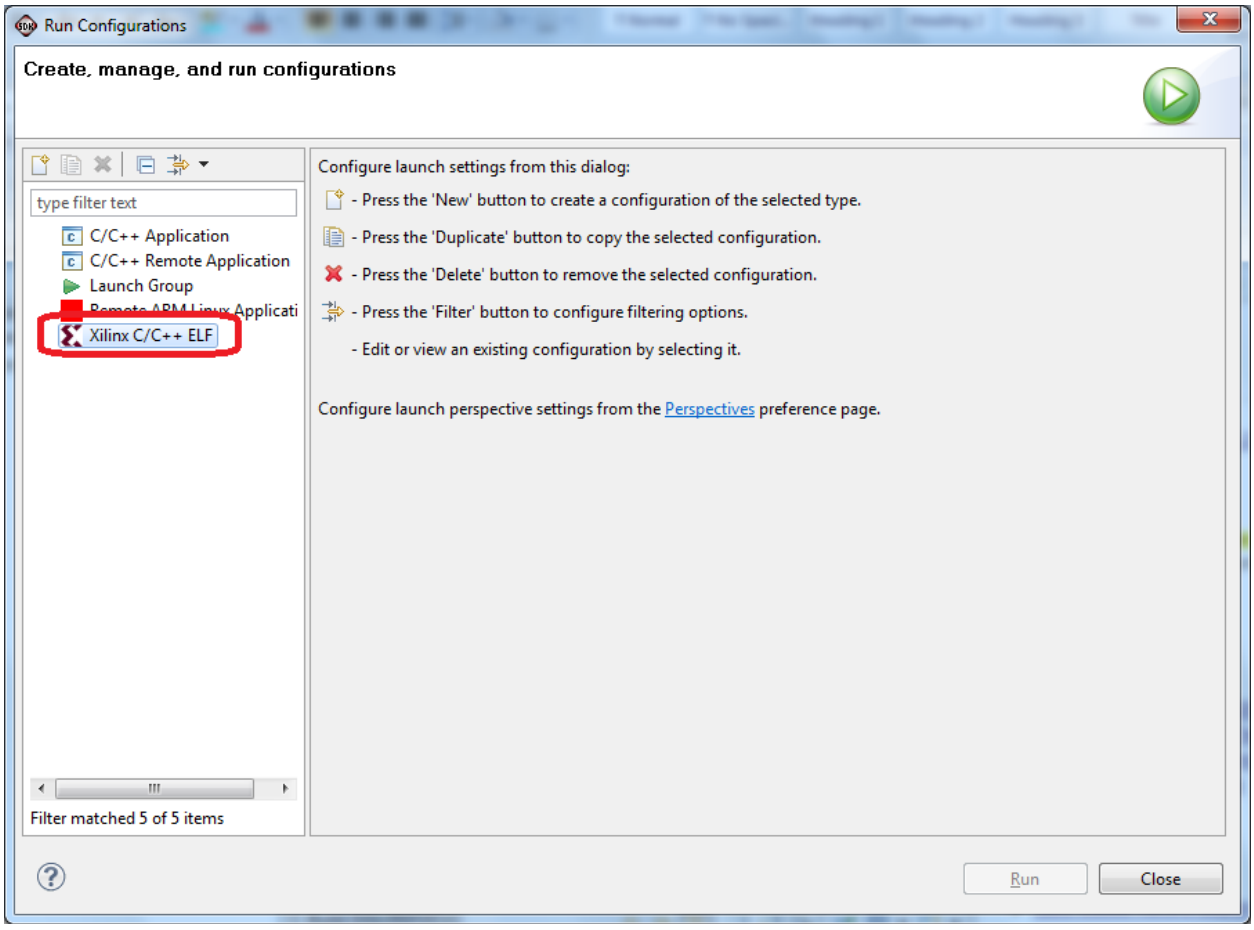
    **Note:** If the terminal program does not connect correctly at the baud rate above, drop the baud rate to 115.2kbps.

11. Use the Xilinx SDK to download and run the executable ELF (.ELF) file on the ARM Cortex-A9 processor using the following steps.

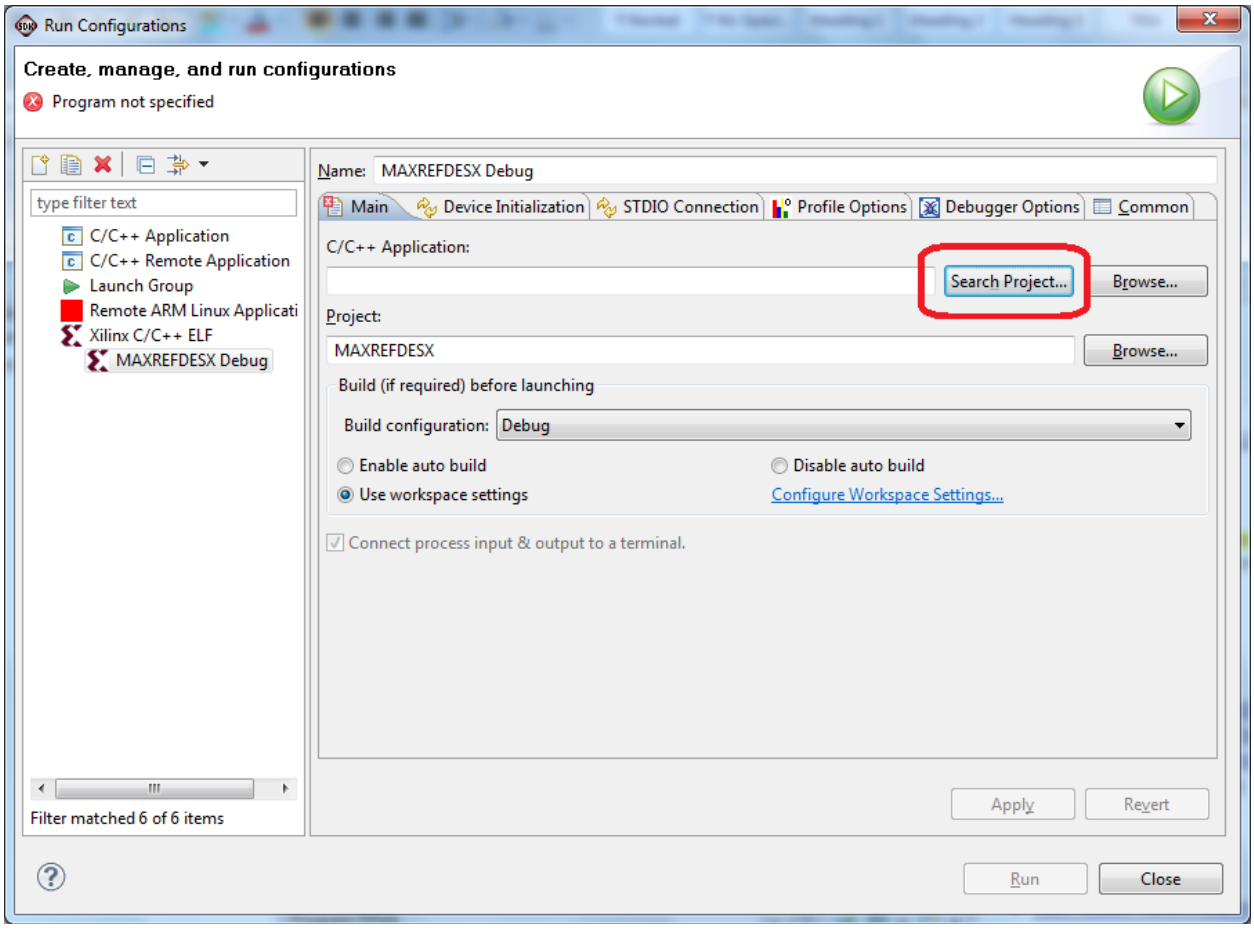
    Right-click the mouse while the **MAXREFDES6 C** project is selected, choose the **Run As** menu, and then **Run Configurations…** menu as shown below.



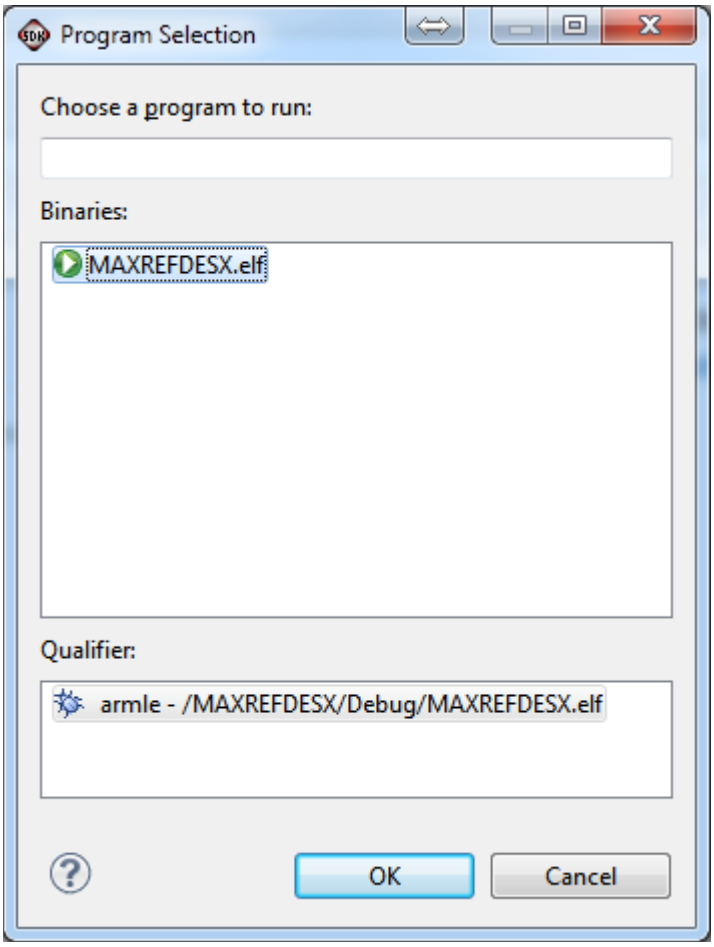
Next, double-click the mouse on the **Xilinx C/C++ ELF** menu.



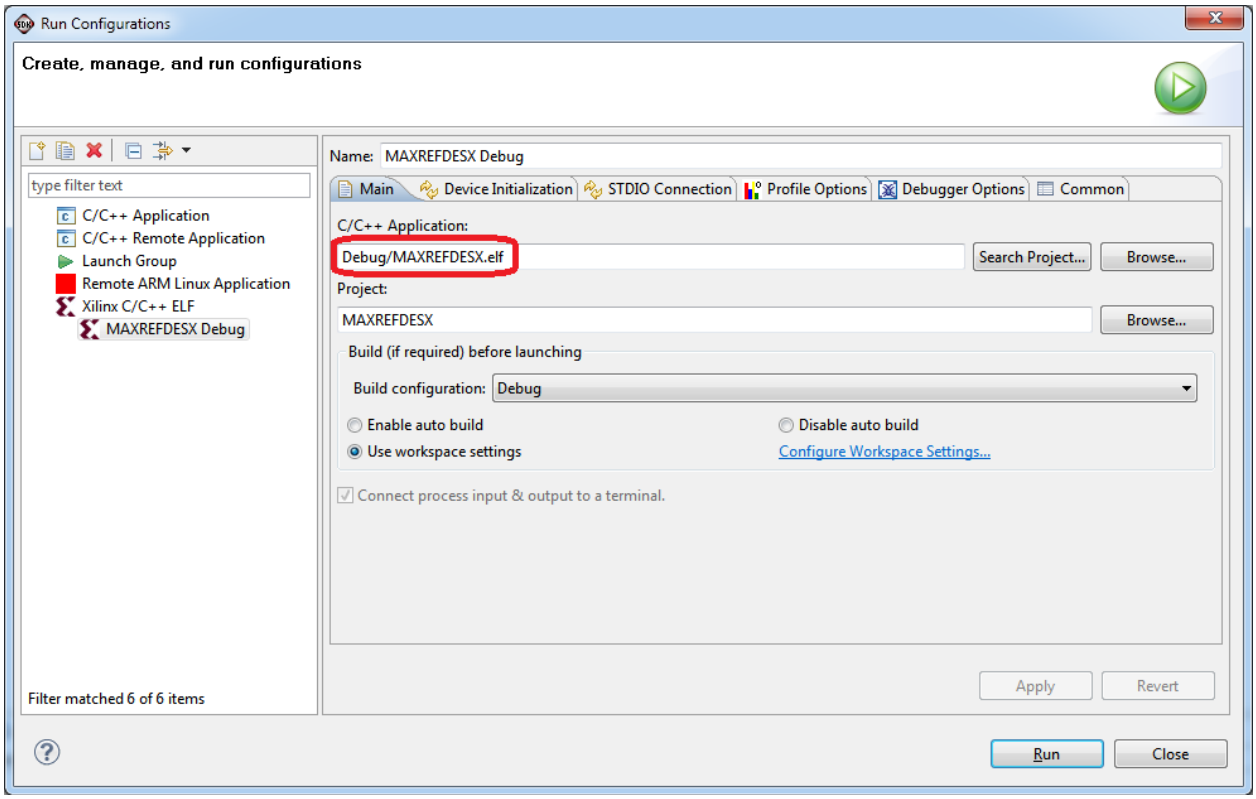
Next, press the **Search Project** button.



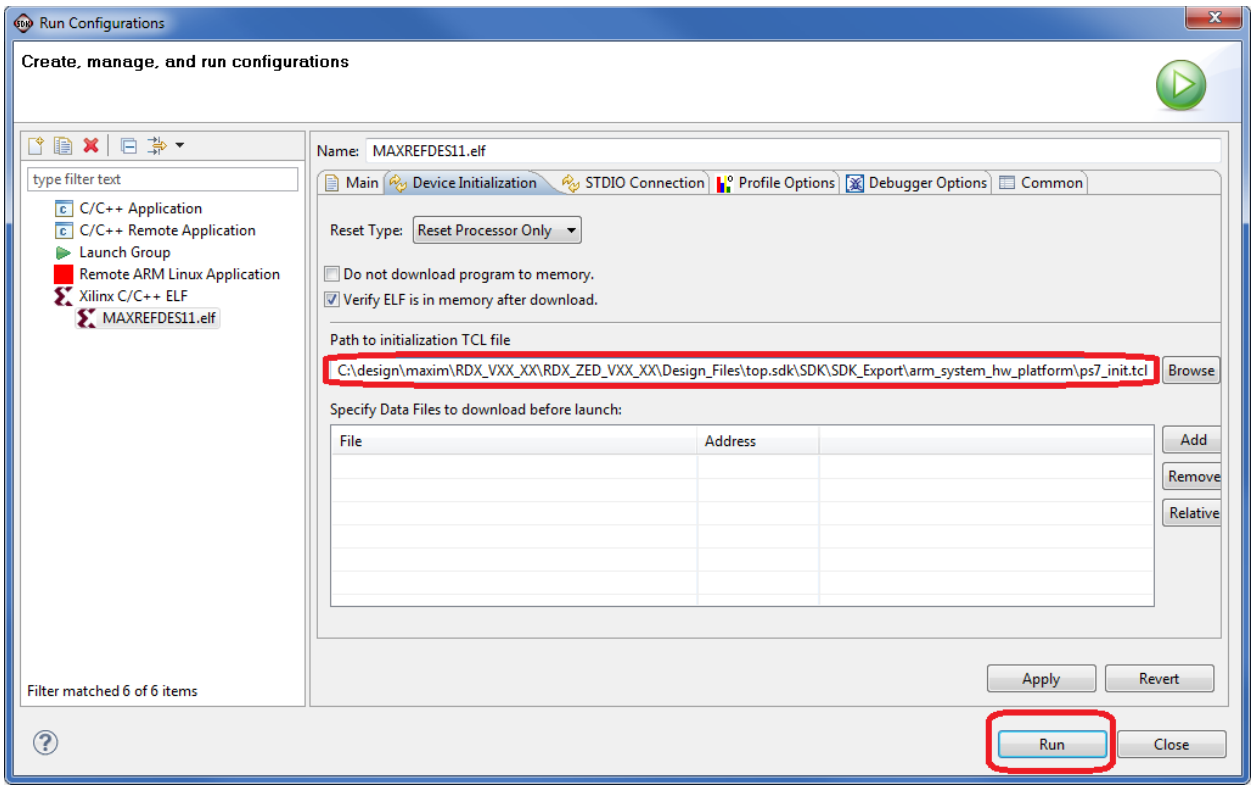
Double-click on the **MAXREFDES6.elf** binary.



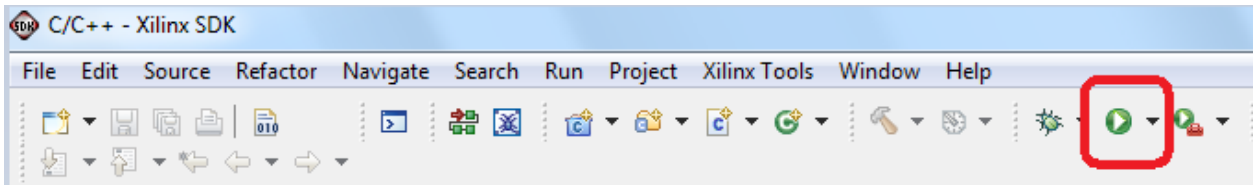
Verify the application is selected on the **Main** tab.



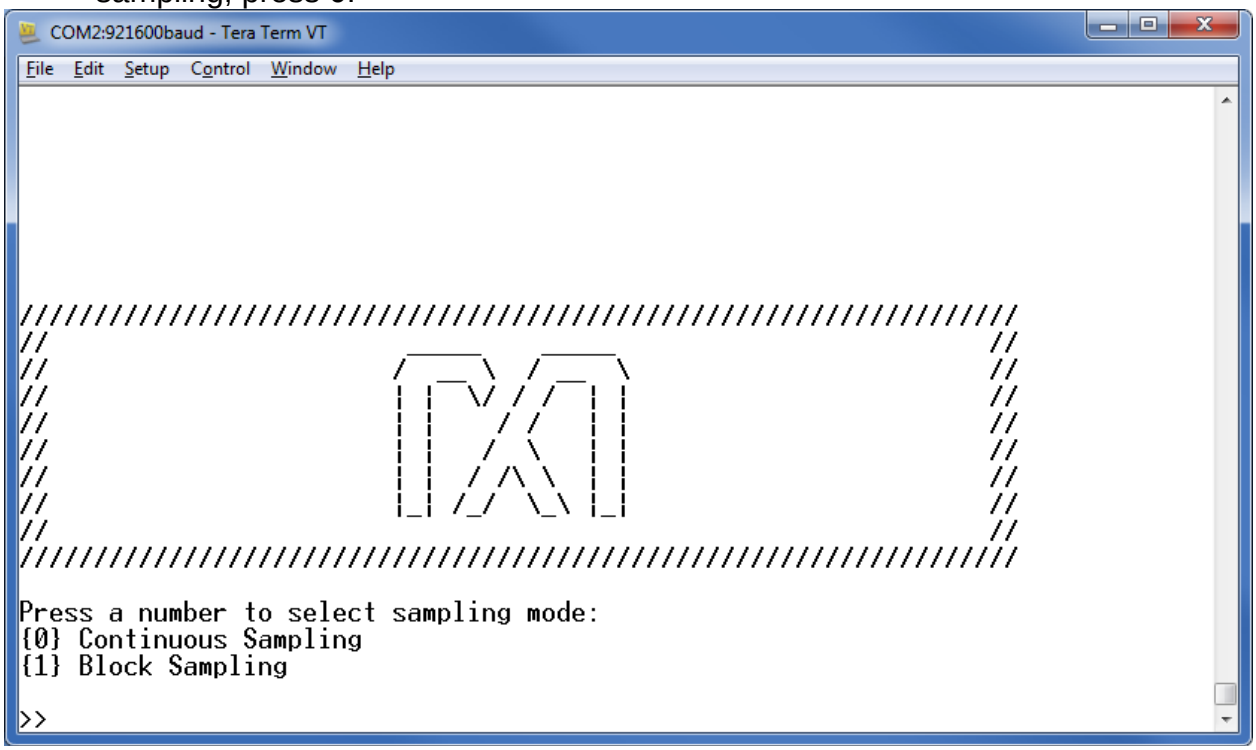
On the **Device Initialization** tab, click **Browse…** button to select the right initialization TCL file and press the **Run** button.




Once the Debug/MAXREFDES6 configuration is set up once, you just need to press the **Run** button if you ever want to run the program again.

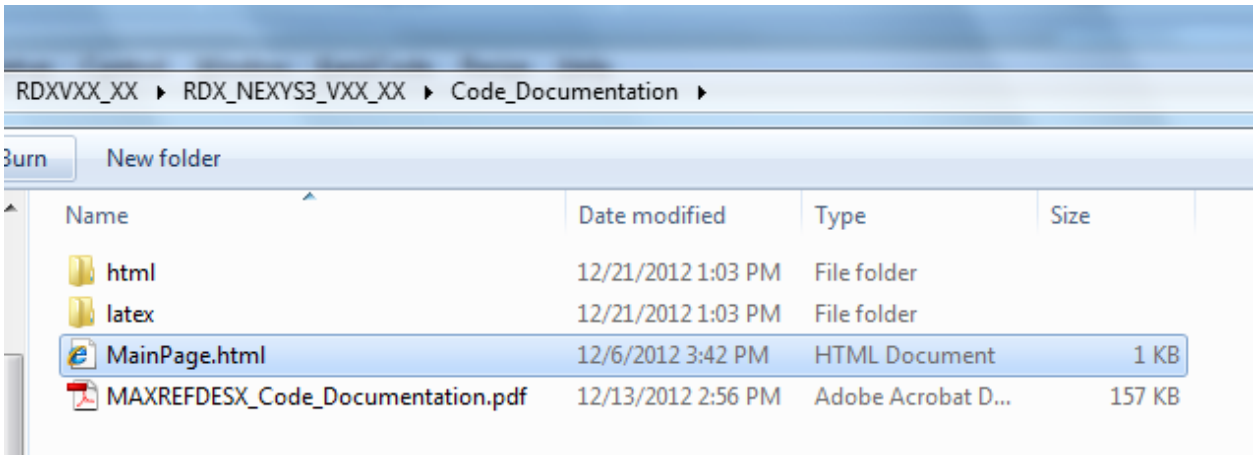


At this point, the application will be running on the Cortex-A9 and the terminal program should show the menu below. Make the desired selections by pressing the appropriate keys on the keyboard. For example, to select continuous sampling, press **0**.



# 5. Code Documentation

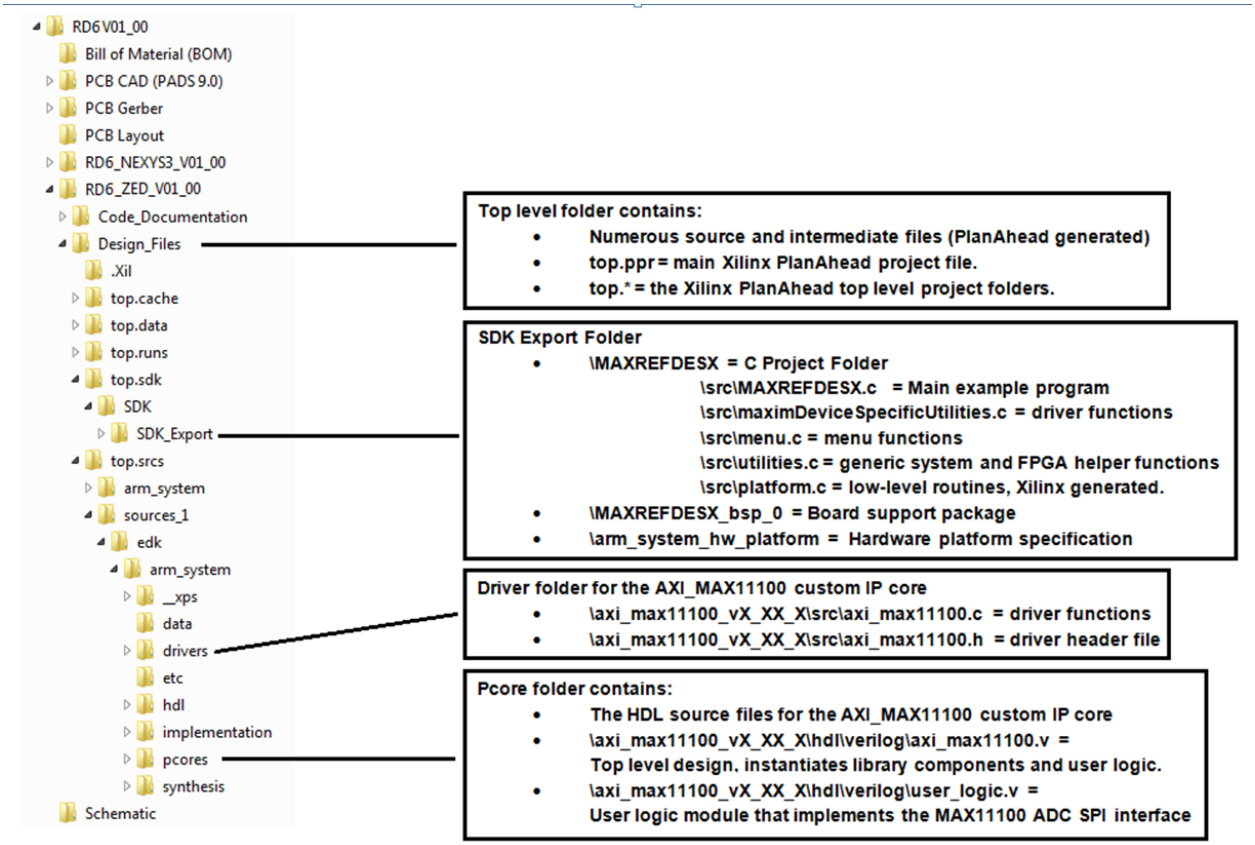
Code documentation can be found at:
**C:\...\RD6V01_00\RD6_ZED_V01_00\Code_Documentation**




To view the code documentation in HTML format with a browser, open the **MainPage.html** file.

To view the code documentation in .PDF format with a PDF reader, open the **MAXREFDES6_Code_Documentation.pdf** file.

# 6. Appendix A: Project Structure and Key Filenames

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Zynq is a registered trademark of Xilinx, Inc.

## 8. Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 9/13 | Initial release | — |