ATMEL WHITE PAPER

Single Cycle 8051 Core—AT89LP Family of High Performance & Low Power Flash Microcontrollers

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Summary

The Atmel AT89LP family of products features a single-cycle 8051 core within a highly integrated microcontroller allowing designers to achieve 6x to 12x more performance compared to classic 8051 devices. The 8051 architecture has been used in the industry for decades and remains very popular with system developers. AT89LP microcontrollers offer full binary code compatibility with the original MSC®51 instruction set, ensuring an easy migration path. The single-cycle core provides designers a unique opportunity to upgrade their application with more performance (up to 20 MIPS), less power consumption (up to 80% savings) and code size ranging from 2KB to 64KB. AT89LP microcontrollers reduce system cost and enable faster time-to-market by integrating more system features on chip.

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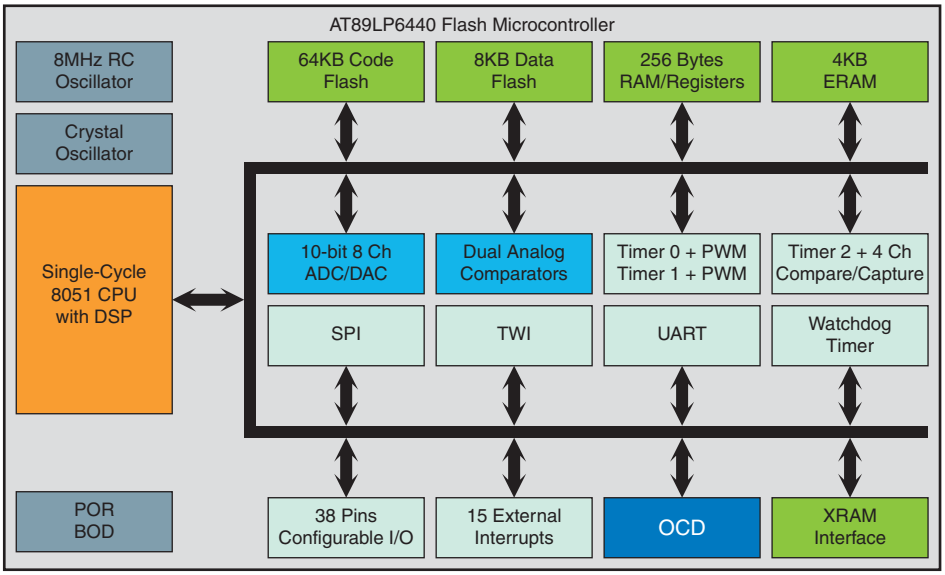
Introducing the Single-Cycle AT89LP Family

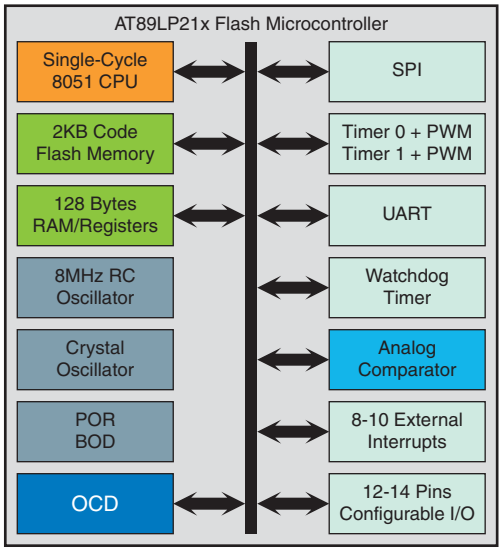
Atmel® introduced the first 8-bit Flash microcontroller in 1993. This first-generation Flash microcontroller was based on the classic 8051 core. The on-chip Flash memory retained its contents even after power was turned off, and was electrically erasable and programmable. Atmel 8051 8-bit microcontrollers were the industry's first Flash based microcontrollers featuring In-System Programming. Atmel was again the first to develop the In-Application Programming feature in its Flash microcontrollers thereby enabling remote upgrades.

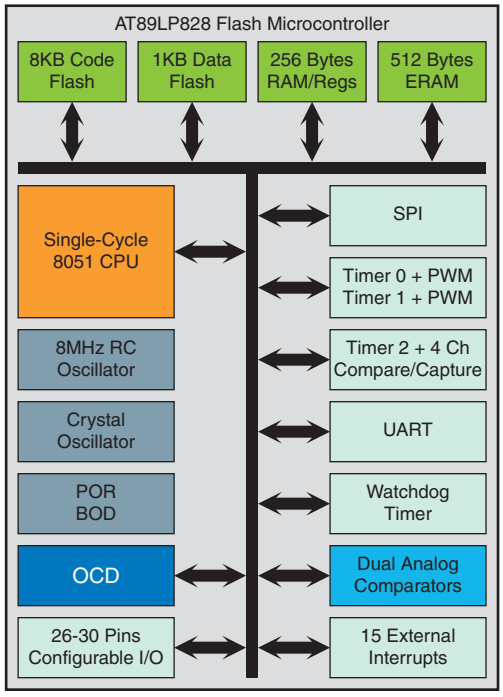
Now Atmel is writing a new chapter in 8051 history with its AT89LP series of next generation 8051 microcontrollers that offer higher performance and lower power than classic 8051s, plus easy migration and greater levels of system integration. The Atmel AT89LP family is based on a low-power, high-performance 8-bit single-cycle 8051 Core that is 100% binary compatible with the traditional 8051 instruction set and yet provides 6 to 12 times more throughput. AT89LP microcontrollers are optimized for low power and high performance applications. The AT89LP microcontrollers reduce system cost and enable faster time-to-market by providing such features as: In-Application Programmable

Flash, On-Chip Flash data, Pulse Width Modulation, 10-bit A/D Converter, Analog Comparator, Internal Oscillator, Watchdog Timer, SPI and On-Chip-Debug.

Figure 1. Example AT89LP Family Block Diagrams.







Key Advantages

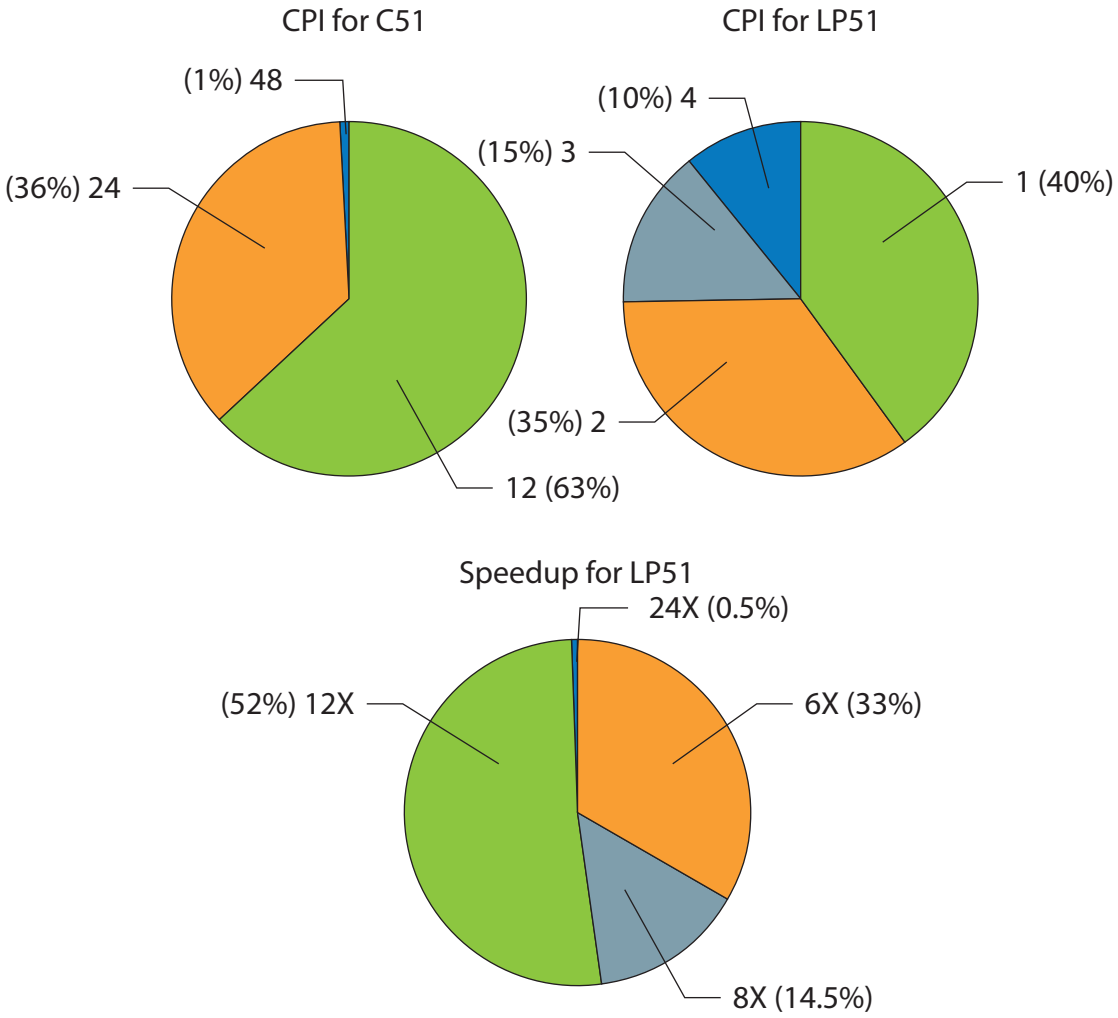
AT89LP microcontrollers have the following key advantages:

- Binary compatibility with the industry standard MCS®51 instruction set
- Access to a wide range of existing code libraries and development tools from several vendors
- Lower power consumption and reduced EMI for the same throughput as classic 8051s
- 6x to 12x quicker interrupt response times and faster pin toggling than classic 8051s
- Fully static CMOS logic implementation driven by a single system clock
- Totally deterministic response at 20 MIPS (no cache memory)
- Boolean processor (bit set/reset read-modify-write instructions execute in two-cycles)
- Power saving modes of operation (Idle and Power-down) with multiple interrupt-based wake-up sources
- Fast programming time using Page Mode
- In-Application Programming for the added power of self-modifying code
- DSP-grade CPU speed using built-in hardware multiplier and fast dual data pointers
- Small footprints for space constrained applications
- Wide voltage operating range to meet a variety of needs
- Upward migration path to devices with larger memories or more I/Os
- On-Chip Debug system allows development of firmware within the target system

Improved Performance

The Atmel AT89LP family is based on a low-power, high-performance 8-bit single-cycle 8051 core. The classic 8051 CPU requires 12 clock cycles for every instruction byte fetch, whereas the new AT89LP CPU employs a simple two-stage pipeline that requires only one clock cycle for every byte fetch. Instructions run on the AT89LP family need only 1 to 4 clock cycles to complete, whereas the classic 8051 requires 12 to 48 clocks, thereby providing 6-12 times or higher throughput than the classic 8051. Seventy percent of the instructions execute in the same number of clock cycles as the number of bytes to be fetched, allowing up to 1 MIPS per MHz of system frequency. At 20 MHz maximum clock frequency the AT89LP core is capable of 20 MIPS throughput. In comparison, the classic 8051 architecture delivers less than 2 MIPS at 20 MHz. Figure 2 shows a comparison of cycles per instruction between a standard 8051 and an AT89LP microcontroller.

Figure 2. Comparison of Cycles Per Instruction (CPI) between C51 and LP51 over all 255 instructions



In addition to the single-cycle CPU core, the AT89LP family of devices offers other enhanced features that improve performance. The following key architectural improvements make the AT89LP family devices fit for low power, yet high performance applications.

- **Hardware Multiplier:** Every AT89LP device includes a 2-cycle hardware multiplier (8x8) with a 24 times speedup from the classic 48-clock MUL instruction. Some devices also support signed/unsigned multiply support.
- **DSP:** The AT89LP6440 introduced a multiply and accumulate (MAC) instruction with a 16x16 signed multiplier feeding a 40-bit accumulator. Along with FIFO addressing this opens the 8051 world to low cost 16-bit digital signal processing applications with the ability to perform FIR or IIR filtering routines at audio rates.

- **Dual Data Pointers:** Some AT89LP devices have native support for dual data pointers with fast context switching, allowing faster access to RAM for memory intensive applications like DSP.
- **Extra RAM:** Some AT89LP devices include on-chip extra RAM that can be accessed in half the time of external memory.
- **Extended Stack:** Devices with on-chip extra RAM also provide an extended stack option for more stack space than the standard 256-byte RAM. For example, the AT89LP6440 supports up to 4KB of extended stack memory, allowing more flexibility when developing with a high-level language like C.
- **Timer/Counters:** The Timer/Counters on AT89LP can increment at a rate of once per clock cycle. This compares to once every 12 clocks in the classic 8051. This allows for higher frequency waveform generation and faster data rates on the UART.
- **Interrupts:** AT89LP devices provide a higher event sampling rate, quicker response to interrupts and faster completion of service routines.
- **I/O Ports:** The I/O ports may be configured in four different modes: input-only (tristated), full CMOS output, open-drain output and quasi-bidirectional (classic 8051). Full CMOS mode allows for higher current sourcing that standard 8051s.

Low Power

The Atmel AT89LP Family was designed not only with performance in mind, but also power consumption. How can an architecture designed for high performance also be low power? Typical dynamic power is often written with the following equation where C is the capacitance toggled, Vcc is the supply voltage and f is the operating frequency:

$$P_{dynamic} = C \cdot V_{CC}^2 \cdot f$$

Power consumption can be reduced by decreasing any of these three parameters. The AT89LP family reduces all three, with the core directly affecting both the C and f factors. The AT89LP core was designed to limit the number of events occurring during an instruction simply by reducing the number of clocks per instruction. The core also reduces the amount of logic toggling during an instruction (the C factor).

Reducing the number of clocks per instruction also affects the frequency (f factor) in two ways. A given instruction on an AT89LP takes less time than the same instruction on a classic 8051 at the same frequency. This is critical for battery-powered applications that spend the majority of their time in a sleep mode. An AT89LP microcontroller can complete its active processing tasks faster than a classic 8051 and therefore spend more of its time in a low power sleep mode for the same workload. The inverse relationship also benefits applications that make less use of a sleep mode and have a workload that takes a fixed amount of time. The AT89LP can complete the work in the same time as a classic 8051, but at a much lower frequency, thereby reducing the total power consumption. For example, an AT89LP at 2 MHz can produce the same throughput of a classic 8051 running at 12 MHz for a power reduction of 6X.

The third factor, the supply Voltage (Vcc), can have the greatest impact on power due to the exponential relationship; however, it is often application dependent. For those applications that are flexible in choice of operating voltage, the AT89LP family offers operation down to 2.4V at speeds of up to 20 MHz.

A comparison between the power consumption of the classic AT89S52 and the single-cycle AT89LP52 is listed in Table 1.

Table 1. Power Comparison of AT89S52 and AT89LP52

	AT89S52	AT89LP52
Active Supply Current @ 12MHz, 5V	25 mA	7 mA
Idle Supply Current @ 12 MHz, 5V	6.5 mA	3 mA
Power-down Current @ 5V	50 uA	2 uA
MIPS (maximum) @ 12 MHz	1	12
mA per MIPS	25	0.58

Ease of Migration

Atmel AT89LP microcontrollers are built around an enhanced 8051 CPU that delivers more performance and yet remains 100% fully binary compatible with the industry standard MCS®51 instruction set. Keeping the same instruction set allows legacy code already written for the 8051 architecture to run on an AT89LP. The large body of existing code libraries will work with an AT89LP microcontroller. Furthermore, the Special Function Register (SFR) addresses and bit assignments are compatible with current Atmel 8051 microcontrollers for greater software portability.

In some cases software compatibility alone is not sufficient when moving to a new device. The 8051 is used in a wide range of applications with many different requirements and firmware developers can be very creative. For example, it is common on the 8051 to use software delay loops and bit banging where the timing of the instructions is also critical. Starting with the AT89LP52, Atmel has introduced a patent-pending 12-clock compatibility mode for its AT89LP family. Devices with this feature can operate either as a single-cycle 8051 for higher performance or as a classic 12-clock 8051 with instruction timing that is backwards compatible with older devices. The AT89LP52 in compatibility mode, for example, can replace an AT89S52 with no software changes. Of course the developer is always free to take advantage of new features and improved performance.

System Integration

Atmel AT89LP microcontrollers are built around an enhanced single-cycle 8051 CPU paired with on-chip RAM and a range of integrated peripherals. Peripherals range from 8051 standards like timers and UARTs to system supervisory functions, advanced analog functions and Controller Area Network (CAN) interfaces. The high level of system integration on AT89LP devices provides reduced system cost, lower power consumption and faster time-to-market.

Timer/Counters

AT89LP microcontrollers have two or more 16-bit timers for use as system timers or event counters. Timer 0 and Timer 1 can independently generate 8-bit pulse width modulation waveforms. Timer 2 on the AT89LP828 and AT89LP6440 is paired with a 4 channel Compare/Capture Array (CCA) to capture events and perform measurements on multiple channels or to generate multi-phasic PWM waveforms for advanced motor control.

Serial Communication

AT89LP microcontrollers may include a full Serial Peripheral Interface (SPI) bus for high-speed serial communication with both master and slave modes; an enhanced UART with automatic address recognition and framing error detection; and an I2C-comptaible master-slave Two-Wire Interface (TWI).

Analog Peripherals

AT89LP microcontrollers may include one or more analog comparators with selectable interrupt modes and a tunable digital debouncer. Some devices also include an integrated 10-bit analog-to-digital converter (ADC) with multiple input channels and single-ended or fully differential operation, plus a digital-to-analog (DAC) operating mode.

Configurable I/O

Each pin of an AT89LP microcontroller is independently configurable in one of four modes: input-only (high impedance), open-drain, push-pull CMOS output, or Quasi-bidirectional (8051-style). These modes can allow on-chip pull-ups to be disabled to reduce power, the use of Port 0 without external pull-ups or greater current sourcing capabilities. In addition, all pins of Port 1 may be configured to generate an interrupt for a variety of edge or level conditions.

Supervisory Functions

AT89LP microcontrollers integrate several supervisory functions on chip, including Power-on Reset, Brown-out Detection, Software Reset, and a Watchdog Timer.

Clock Selection

The AT89LP devices can be clocked from several clock sources, including:

- External clock source
- On-chip crystal oscillator in high or low frequency mode
- Internal RC oscillators with ±5% or better accuracy

Power Reduction

AT89LP microcontrollers include two power-saving modes of operation: Idle and Power-down. These modes can be exited through a variety of interrupt conditions.

Example Applications

The majority of embedded applications continue to be based on 8-bit devices. AT89LP microcontrollers provide high levels of integration leading to reduced system cost, lower power consumption, smaller packages, and faster time-to-market. These devices are ideal for communications, consumer, and industrial products, ranging from battery-powered devices to white goods. Some example uses include:

- Protocol Conversion
  - Create a low-cost SPI—UART bridge.
  - Convert the parallel port of a legacy device to an SPI bus .
- Intelligent Electronics
  - Replace discrete logic components and programmable logic devices in control systems with an AT89LP device for the added flexibility of a microcontroller.
  - Create smart sensors using the integrated ADC.
  - Configure intelligent displays using the high current capability of the I/O drivers.
  - Incorporate a low-cost, small package AT89LP device into disposable electronics for medical or drug testing.
- Waveform Capture and Generation
  - Capture and process multi-channel events with the Compare/Capture Array.
  - Drive electric motors with the up to four-phasic PWM.
  - Use the on-chip timers for pulse generation, programmable frequency sources, or remote control encoders.
  - Encode speech waveforms for direct digital speaker drive.
- Industrial Communication
  - Automate and network equipment with CAN

Device Overview

Table 2. Parametric Device Table

Device	Flash CODE Memory	Flash DATA Memory	EEPROM	RAM	12-Clock Compatibility	DSP	CAN Mailboxes	16-Bit Timers	PWM Outputs	Compare/Capture Ch	UART	SPI	TWI	Analog Comparators	ADC	Crystal Oscillators	Pins	Availability
AT89LP213	2K			128				2	2		N	Y	N	1	N	1	14	Now
AT89LP214	2K			128				2	2		Y	Y	N	1	N	1	14	Now
AT89LP216	2K			128				2	2		Y	Y	N	1	N	1	16	Now
AT89LP2052	2K			256				2	2		Y	Y	N	1	N	1	20	Now
AT89LP4052	4K			256				2	2		Y	Y	N	1	N	1	20	Now
AT89LP428	4K	512		768				3	6	4	Y	Y	N	2	N	1	28/32	Now
AT89LP828	8K	1K		768				3	6	4	Y	Y	N	2	N	1	28/32	Now
AT89LP51	4K	256		256	Y			3			Y	N	N		N	1	40/44	Now
AT89LP52	8K	256		256	Y			3			Y	N	N		N	1	40/44	Now
AT89LP3240	32K	8K		4352		Y		3	6	4	Y	Y	Y	2	10-bit	1	40/44	Now
AT89LP6440	64K	8K		4352		Y		3	6	4	Y	Y	Y	2	10-bit	1	40/44	Now
AT89LP51RB2	20K			1280	Y	Y		4	7	5	Y	Y	Y		10-bit	1	40/44	11Q4
AT89LP51RC2	32K			1280	Y	Y		4	7	5	Y	Y	Y		10-bit	1	40/44	11Q4
AT89LP51RD2	64K			2304	Y	Y		4	7	5	Y	Y	Y	2	10-bit	1	40/44	11Q3
AT89LP51ED2	64K		4K	2304	Y	Y		4	7	5	Y	Y	Y	2	10-bit	1	40/44	11Q3
AT89LP51IC2	32K			1280	Y	Y		4	7	5	Y	Y	Y	2	10-bit	2	44	11Q4
AT89LP51ID2	64K		4K	2304	Y	Y		4	7	5	Y	Y	Y	2	10-bit	2	44	11Q3
AT89LP51CC01	32K		4K	2304	Y	Y	16	4	7	5	Y	Y	N	2	10-bit	1	44	12Q1
AT89LP51CC03	64K		4K	2304	Y	Y	16	4	7	5	Y	Y	N	2	10-bit	1	44	12Q1

Conclusion

The AT89LP family devices are cost-effective 8-bit microcontrollers ideal for applications requiring low power and high performance. These new microcontrollers reduce system cost with a variety of on-chip features enabling faster time-to-market. Ideal for Power Management, White Goods, and Universal Remote Control applications, the AT89LP family devices provide greater system-level integration. With the new AT89LP devices, system designers can enjoy up to 80% decrease in power consumption compared to classic 8051 microcontrollers at the same MIPS performance level. Consequently, the EMC characteristics also improve significantly.

Binary compatibility with the standard 8051-instruction set allows upward migration from multi-clock cycle 8051 cores to the higher performance AT89LP-series. Atmel's Single-Cycle AT89LP Flash Microcontrollers are easy to use, and offer a rich and powerful CISC instruction set at RISC performance.

References

1. Atmel 8051 datasheets and product documentation, Web http://www.atmel.com

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