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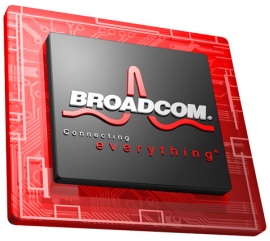
BCM8706 PRODUCT Brief



XAUI™ TO SERIAL 10G BASE-LRM TRANSCEIVER

FEATURES

- **Meets and exceeds industry standard**
  - IEEE 802.3ae
  - IEEE802.3aq
- **High-performance mode supports 300m of MMF fiber.**
- **Low-power mode supports 220m of MMF, as specified in the 802.3aq standard.**
- **Integrated AGC with a dynamic range of 60 mV–700 mV**
- **Multiple interface support**
  - 4 Lane XAUI™ (3.125 Gbps)
  - XFP/XFI
  - Programmable amplitude control on 10G serial transmitter
  - PMD
    - Serial 10.3125-Gbps CML
- **Receive equalization on XAUI and 10G serial interfaces**
- **Power dissipation: < 1.5W (Low-power mode)**
- **Core Supply: 1.0V; I/O: 3.3V**
- **Reference clock output for XFP module reference clock**
- **Loss-of-signal detection**
- **Link activity indicator outputs**
- **XAUI transmit pre-emphasis for transmission over backplanes**

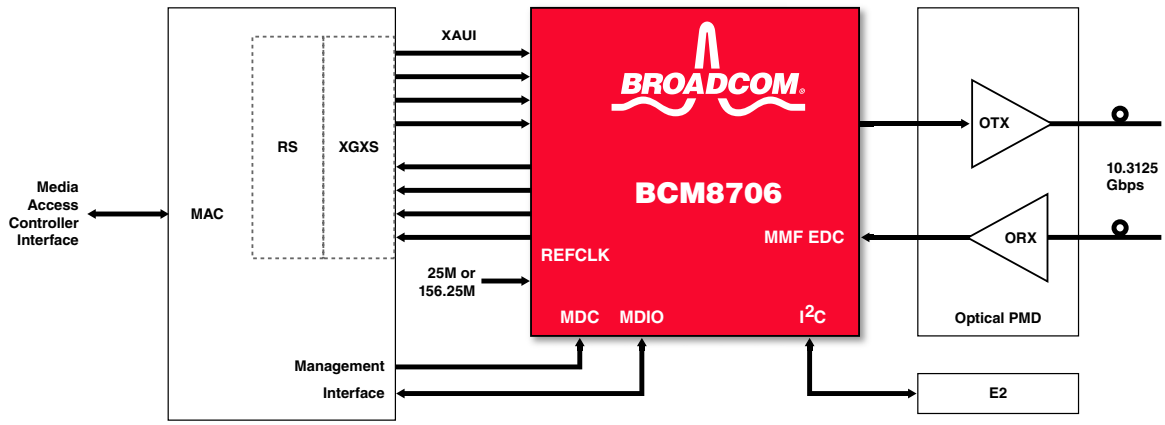
SUMMARY OF BENEFITS

- **MDIO interface compliant to IEEE 802.3ae Clause 45 with extended indirect address register access**
- **Single reference clock input, enables use of low-cost 25-MHz crystal or 156.25-MHz oscillator.**
- **Integrated micro-controller, no external memory required**
- **Support for XENPAK/X2 3.0 and XPAK MSA Optical Module standards and the emerging SFP+ standard**
- **Simplifies manufacturability with integrated built-in self test (BIST) and loopback modes on the 10-G serial and XAUI interfaces.**
- **Standard I^2C serial interface support for external E2 and XFP.**
- **XAUI link synchronization/deskew**
- **XGXS 8B/10B error detection ENDEC**
- **PCS 64B/66B scrambler/descrambler**

APPLICATIONS

- **XENPAK, X2 Modules for LRM**
- **Direct attach to SFP+ modules**
- **Network interface cards (NICs)**

BCM8706 Functional Block Diagram



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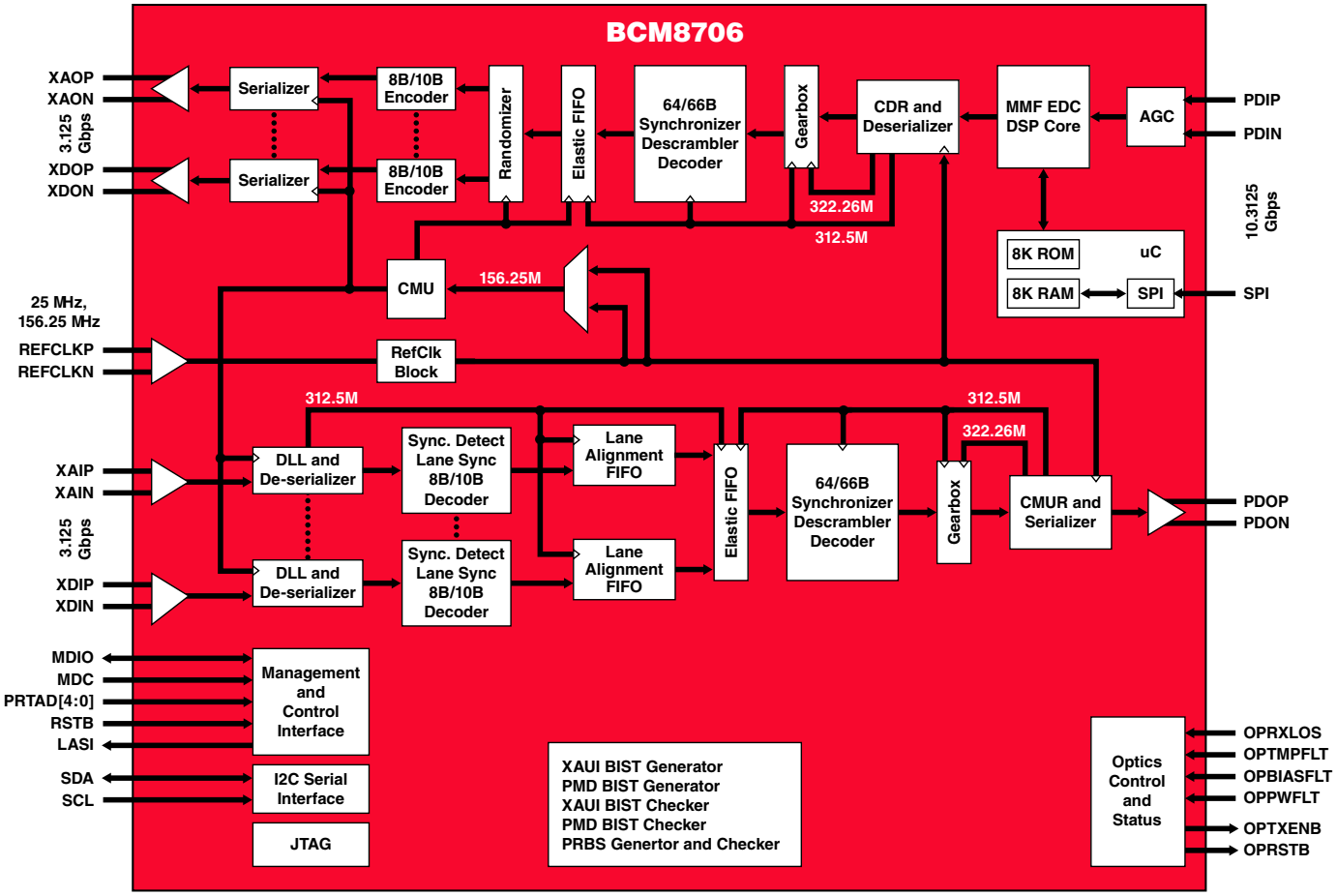

BCM8706 Reference Design

The BCM8706 incorporates a receive equalizer that supports Electronic Dispersion Compensation (EDC) over multimode fiber (MMF). The EDC equalizer is designed for applications over MMF covering distances up to 220m of OM1, OM2, OM3 fiber as per the IEEE standard. The BCM8706 will be fully compliant with the IEEE802.3aq standard. In enhanced performance mode, the BCM8706 is capable of supporting up to 300m over OM1, OM2, and OM3 fiber.

An onboard microcontroller implements the control algorithm for the MMF EDC DSP Core.

On-chip clock synthesis is performed by the high-frequency low-jitter phase-locked loops for the PMD and XAUI output retimers. Individual PMD and XAUI clock recovery is performed on the device by synchronizing directly to the respective incoming data streams. An external 25-MHz or 156.25-MHz oscillator is required for the reference clock input.

The BCM8706 Ethernet LRM PHY is a fully integrated SerDes (10.3125 Gbps) interface device performing the extension functions for a 10-GbE Reconciliation Sublayer (RS) interface. The XGXS, PCS, and PMA functions include 8B/10B coding, 64B/66B coding, SerDes, Clock Multiplication Unit (CMU), and Clock and Data Recovery (CDR).

The BCM8706 is available in a 13 mm × 13 mm, 256-pin FBGA, RoHS compliant package.

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BROADCOM CORPORATION
16215 Alton Parkway, P.O. Box 57013
Irvine, California 92619-7013

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Phone: 949-450-8700
Fax: 949-450-8710
E-mail: info@broadcom.com
Web: www.broadcom.com