



Product Change Notification / SYST-17BFQQ972

Date:

18-Sep-2020

Product Category:

Microprocessors

PCN Type:

Document Change

Notification Subject:

Data Sheet - SAMA5D2 Series Datasheet

Affected CPNs:

[SYST-17BFQQ972_Affected_CPN_09182020.pdf](#)

[SYST-17BFQQ972_Affected_CPN_09182020.csv](#)

Notification Text:

SYST-17BFQQ972

Microchip has released a new Product Documents for the SAMA5D2 Series Datasheet of devices. If you are using one of these devices please read the document located at [SAMA5D2 Series Datasheet](#).

Notification Status: Final

Description of Change:

I. Revision DS60001476F. Restored arrayed bit fields and registers (pdf generation error). No content changes from DS60001476E.

II. Revision DS60001476E

- 1) All section. Editorial changes throughout
- 2) Editorial changes throughout.
- 3) Microchip Recommended Power Management Solutions. New section.
- 4) Reset Controller (RSTC). Updated NRST Manager.
- 5) Power Management Controller (PMC).
 - a) Updated Embedded Characteristics.
 - b) Updated Divider and PLLA Block and figure.
 - c) Updated Divider and Phase Lock Loop Programming.

- 6) Parallel Input/Output Controller (PIO).
 - a) Description: modified
 - b) PIO Controller Block Diagram: modified.
 - c) I/O Line Control Logic: modified.
 - d) Added figure PIO Interrupt Management.
 - e) PIO_CFGRx: reset value modified.
 - f) S_PIO_CFGRx: reset value and PCFS bit description modified.
- 7) External Memories Description: updated DDR2 supply.
- 8) DMA Controller (XDMAC)
 - a) Transfer Hierarchy Diagrams: removed figure "XDMAC Peripheral Transfer Hierarchy".
 - b) Added Peripheral to Memory Transfer and Memory to Peripheral Transfer.
- 9) Ethernet MAC (GMAC)
 - a) References to Partial Store and Forward mode deleted from Packet Buffer DMA, Receive Buffers, Transmit Buffers, DMA Packet Buffers, Transmit Packet Buffer, Receive Packet Buffer, GMAC DMA Configuration Register.
 - b) Deleted sections Partial Store and Forward Using Packet Buffer DMA, GMAC TX Partial Store and Forward Register and GMAC RX Partial Store and Forward Register.
 - c) Modified Receive BuffersDMA Bursting on the System Bus, Receive Packet Buffer, GMAC Receive Buffer Queue Base Address Register, GMAC Transmit Buffer Queue Base Address Register.
 - d) Updated Block Diagram.
 - e) Updated Data Paths with Packet Buffers Included.
- 10) Flexible Serial Communication Controller (FLEXCOM)
 - a) Throughout: Reworked sections regarding asynchronous partial wake-up.
 - b) Updated Description.
 - c) Updated TWI Compatibility with I2C Standard.
 - d) Updated TWI/SMBus Characteristics.
 - e) Updated Modes of Operation.
 - f) FLEX_US_MR: USART_MODE bit description table modified.
 - g) USART: modified content and some section and figure titles: Overview, TXEMPTY, TXRDY and RXRDY Behavior, FIFO Single Data Access, FIFO Multiple Data Access, TXRDY and RXRDY Configuration, FIFO Pointer Error.
 - h) SPI: modified content and some section and figure titles: Overview, TXEMPTY, TDRE and RDRF Behavior, SPI Single Data Access, SPI Multiple Data Access, TDRE and RDRF Configuration, DMAC_PDC, FIFO Pointer Error.
 - i) TWI: modified content and some section and figure titles: Overview, Sending Data with FIFO Enabled, Receiving Data with FIFO Enabled, TXRDY and RXRDY Behavior, TWI Single Data Access, TWI Multiple Data Access, TXRDY and RXRDY Configuration, DMAC_PDC, FIFO Pointer Error, FIFO Thresholds.
 - j) USART FIFO Mode Register, SPI FIFO Mode Register, TWI FIFO Mode Register: bitfield descriptions modified.
- 11) Image Sensor Controller (ISC)
 - a) Reworked:
 - Image Sensor Controller Functional Diagram
 - Image Sensor Controller Clock Domain Diagram
 - Image Sensor Controller Typical Use Cases
 - b) Added I/O Lines Description.
 - c) Updated I/O Lines, Power Management.
 - e) Updated ISC Clock Management.
 - f) Renamed and reworked Contrast, Brightness, Hue and Saturation.
- 12) Pulse Width Modulation Controller (PWM)
 - a) Updated PWM Controller Block Diagram.
 - b) Added External Trigger Inputs.
 - c) External PWM Reset Mode: Power Factor Correction Application, External PWM Start Mode: Buck DC/DC Converter, Cycle-By-Cycle Duty Mode: LED String Control: modified.
- 13) Advanced Encryption Standard (AES) AES_CR: index 0 now populated with START
- 14) Electrical Characteristics
 - a) Maximum SPI Frequency: updated Slave Write Mode equation.
 - b) DDR3/DDR3L-SDRAM: added note after table.

Impacts to Data Sheet: None

Reason for Change: To Improve Manufacturability

Change Implementation Status: Complete

Date Document Changes Effective: 18 Sep 2020

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

[SAMA5D2 Series Datasheet](#)

Please contact your local [Microchip sales office](#) with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

ATSAMA5D27C-D5M-CU
ATSAMA5D27C-D5M-CUR
ATSAMA5D225C-D1M-CU
ATSAMA5D225C-D1M-CUR
ATSAMA5D27C-D1G-CU
ATSAMA5D28C-D1G-CU
ATSAMA5D27C-D1G-CUR
ATSAMA5D28C-D1G-CUR
ATSAMA5D28A-CU
ATSAMA5D27A-CU
ATSAMA5D24A-CU
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