SY89809AL

3.3V LVPECL/HSTL to HSTL 1:9 High-Performance Clock Driver with LVTTL Clock Select and Enable

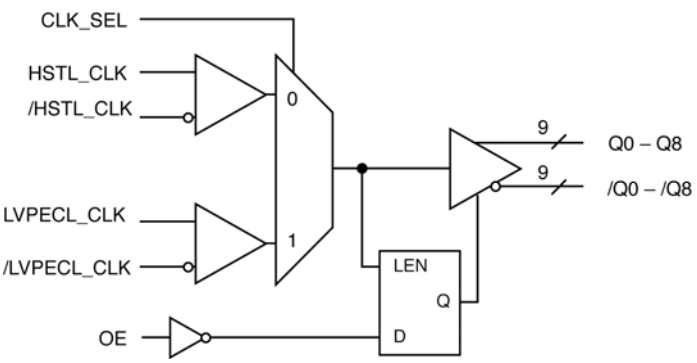
General Description

The SY89809AL is a high-performance bus clock driver with nine differential High-Speed Transceiver Logic (HSTL) output pairs. The part is designed for use in low-voltage (3.3V/1.8V) applications, which require a large number of outputs to drive precisely aligned, ultra-low skew signals to their destination. The input is multiplexed from either HSTL or Low-Voltage Positive-Emitter-Coupled Logic (LVPECL) by the CLK_SEL pin. The Output Enable (OE) is synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state. This avoids any chance of generating a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control.

The SY89809AL features low pin-to-pin skew (15ps typical) and low part-to-part skew (100ps typical). The SY89809AL is available in a single space-saving package, enabling a lower overall cost solution.

Datasheets and support documentation can be found on Micrel's web site at: www.micrel.com.

Block Diagram



Precision Edge®

Features

- 3.3V core supply, 1.8V output supply for reduced power
- LVPECL and HSTL inputs
- Nine differential HSTL (low-voltage swing) output pairs
- HSTL outputs drive 50Ω-to-ground with no offset voltage
- 750MHz maximum clock frequency
- Low part-to-part skew (100ps typical)
- Low pin-to-pin skew (15ps typical)
- Available in 32-pin TQFP

Applications

- High-performance PCs
- Workstations
- Parallel processor-based systems
- Other high-performance computing
- Communications

Level	Direction	Signal
HSTL	Input	HSTL_CLK, /HSTL_CLK
HSTL	Output	Q0 – Q8, /Q0 – /Q8
LVPECL	Input	LVPECL_CLK, /LVPECL_CLK
LVCMOS/LVTTL	Input	CLK_SEL, OE

Table 1. Signal Groups

OE[1]	CLK_SEL	Q0 – Q8	/Q0 – /Q8
0	0	LOW	HIGH
0	1	LOW	HIGH
1	0	HSTL_CLK	/HSTL_CLK
1	1	LVPECL_CLK	/LVPECL_CLK

Table 2. Truth Table

Note:

1. The OE (output enable) signal is synchronized with the low level of the HSTL_CLK and LVPECL_CLK signal.

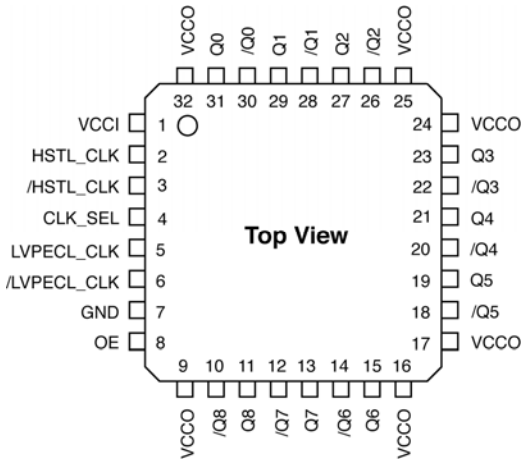
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89809ALTZ[3]	T32-1	Commercial	SY89809ALTZ with Pb-Free bar-line indicator	Matte-Sn Pb-Free
SY89809ALTZTR[2, 3]	T32-1	Commercial	SY89809ALTZ with Pb-Free bar-line indicator	Matte-Sn Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

Pin Configuration



32-Pin TQFP (T32-1)

Pin Description

Pin Number	Pin Name	Type	Pin Function
2, 3	HSTL_CLK, /HSTL_CLK	HSTL Input	Differential clock input selected by CLK_SEL. Can be left floating if not selected. Floating input, if selected, produces a LOW at HSTL_CLK and a HIGH at /HSTL_CLK. HSTL input signal requires external termination 50Ω-to-ground.
5, 6	LVPECL_CLK, /LVPECL_CLK	LVPECL Input	Differential clock input selected by CLK_SEL. Can be left floating if not selected. Floating input, if selected, produces a LOW at LVPECL_CLK and a HIGH at /LVPECL_CLK. Non-inverted input has a 75kΩ pull-down. Inverted input has a 75kΩ pull-down and a 37.5kΩ pull-up.
4	CLK_SEL	LVTTL Input	Selected HSTL_CLK input when LOW and LVPECL_CLK output when HIGH. 37.5kΩ pull-up.
8	OE	LVTTL Input	Enable input synchronized internally to prevent glitching of the Q0-Q8 and /Q0-/Q8 outputs. OE high-to-low transition ensures outputs remain disabled during the next clock cycle. OE low-to-high transition enables normal operation of the next input clock. 37.5kΩ pull-up.
31, 29, 27, 23, 21, 19, 15, 13, 11	Q0 – Q8	HSTL Output	Differential clock outputs from HSTL_CLK when CLK_SEL = LOW and and from LVPECL outputs when CLK_SEL = HIGH. HSTL outputs must be terminated with 50Ω to GND. Q0-Q8 outputs are static LOW when OE = LOW. Unused output pairs may be left floating.

Pin Description (Continued)

Pin Number	Pin Name	Type	Pin Function
30, 28, 26, 22, 20, 18, 14, 12, 10	/Q0 – /Q8	HSTL Output	Differential clock outputs from HSTL_CLK when CLK_SEL = LOW and from LVPECL outputs when CLK_SEL = HIGH. HSTL outputs must be terminated with 50Ω to GND. /Q0-/Q8 outputs are static HIGH when OE = LOW. Unused output pairs may be left floating.
1	VCCI	VCC Core Power	Core V_{CC} connected to 3.3V supply. Bypass with 0.1µF in parallel with 0.01µF low ESR capacitors as close to V_{CCI} pin as possible.
9, 16, 17, 24, 25, 32	VCCO	VCC Output Power	Output Buffer VCC connected to 1.8V supply. Bypass with 0.1µF in parallel with 0.01µF low ESR capacitors as close to V_{CCO} pins as possible. All V_{CCO} pins should be connected together on the PCB.
7	GND	Ground	Ground.

Absolute Maximum Ratings[1]

Input Voltage (V_{IN}) ..... –0.5V to V_{CCI}
V_{CC} Pin Potential to Ground Pin
(V_{CCI}, V_{CCO}) ..... –0.5V to +4.0V
Output Current (I_{OUT}) .....
Continuous 50mA
Surge 100mA
Lead Temperature (soldering, 20sec.) ..... 260°C
Storage Temperature (T_s) ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage
(V_{CCI}) ..... +3.0V to +3.6V
(V_{CCO}) ..... +1.6V to +2.0V
Ambient Temperature (T_A) ..... 0°C to +85°C
Package Thermal Resistance
TQFP (θ_{JA})
–Still-Air ..... 50°C/W
–500lfpm ..... 42°C/W
TQFP (θ_{JC}) ..... 20°C/W

DC Electrical Characteristics

T_A = 0°C to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Power Supply						
V_{CCI}	V_{CC} Core		3.0	3.3	3.6	V
V_{CCO}	V_{CC} Output		1.6	1.8	2.0	V
I_{CCI}	I_{CC} Core			65	90	mA
HSTL						
V_{OH}	Output HIGH Voltage[3]		1.0		1.2	V
V_{OL}	Output LOW Voltage[3]		0.1		0.4	V
V_{IH}	Input HIGH Voltage		V_X +0.1		1.6	V
V_{IL}	Input LOW Voltage		–0.3		V_X – 0.1	V
V_X	Input Crossover Voltage		0.68		0.9	V
I_{IH}	Input HIGH Current		–350		20	µA
I_{IL}	Input LOW Current		–500			µA
V_{IHCMR}	Input HIGH Voltage Common Mode Range(Differential Configuration)		0.6		1.6	V
LVPECL						
V_{IH}	Input HIGH Voltage		V_{CCI} – 1.145		V_{CCI} – 0.895	V
V_{IL}	Input LOW Voltage		V_{CCI} – 1.945		V_{CCI} – 1.695	V
I_{IH}	Input HIGH Current		–150		150	µA
I_{IL}	Input LOW Current		–150		150	µA
V_{IHCMR}	Input HIGH Voltage Common Mode Range(Differential Configuration) [4]		1.2		V_{CCI}	V

Notes:

1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Outputs loaded with 50Ω to ground.
4. V_{IHCMR} max varies 1:1 with V_{CCI}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

hbwhelp@micrel.com or (408) 955-1690

DC Electrical Characteristics

T_A = 0°C to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
LVCMOS/LVTTL						
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current		–150		150	µA
I_{IL}	Input LOW Current		–300		300	µA

AC Electrical Characteristics[5]

T_A = 0°C to +85°C, unless otherwise noted.

Symbol	Parameters	0			25°C			85°C			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{Opp}	Differential Output Voltage										
	F_{OUT} < 100MHz	600	800		600	800		600	800		
	F_{OUT} < 500MHz	600	700		600	700		600	700		mV
	F_{OUT} < 750MHz	450	510		450	510		450	510		
t_{PLH} t_{PHL}	Propagation Delay (Differential Configuration)										
	LVPECL_CLK to Q	680	800	930	700	820	950	780	920	1070	ps
	HSTL_CLK to Q	690	830	990	700	850	1000	790	950	1110	
t_{Skew}	Pin-to-Pin Skew[6]		15	25		15	25		15	25	
	Part-to-Part Skew[7]		100	200		100	200		100	200	ps
t_{JITTER}	Random Clock Jitter (RMS)		1.4	3		1.4	3		1.4	3	ps
V_{PP}	Input Voltage Swing[8]										
	LVPECL	200			200			200			mV
	HSTL	200		1900	200		1900	200		1900	
t_S	OE Set-Up Time[9]	0.5			0.5			0.5			ns
t_H	OE Hold Time	0.5			0.5			0.5			ns
t_r, t_f	Output Rise/Fall Times (20% to 80%) Q, /Q	350		600	350	450	600	350		600	ps

Notes:

5. Outputs loaded with 50Ω to ground. Airflow ≥ 500lfpm.
6. The Pin-to-Pin skew is defined as the worst-case difference between any two similar delay paths within a single device operating at the same voltage and temperature.
7. The Part-to-Part skew is defined as the absolute worst-case difference between any two delay paths on any two devices operating at the same voltage and temperature.
8. V_{PP} is the Input Voltage swing required to maintain AC characteristics listed herein. It represents the input voltage swing for CLK or /CLK.
9. OE set-up time is defined with respect to the rising edge of the clock. OE HIGH-to-LOW transition ensures outputs remain disabled during the next clock cycle.

Output Waveforms

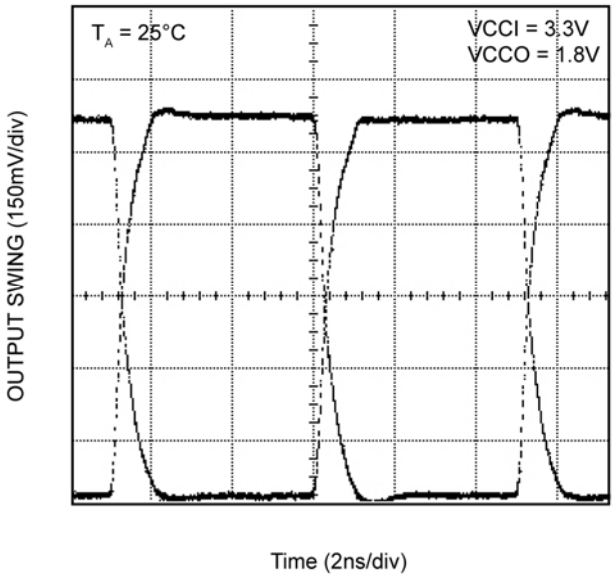


Figure 1. 100MHz Output Waveform

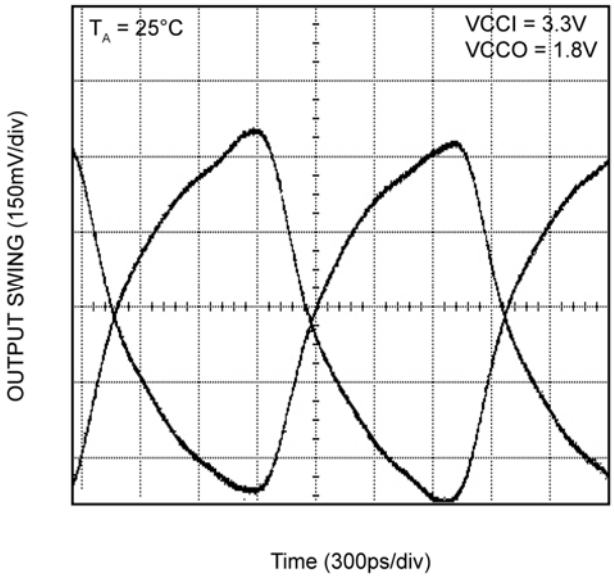
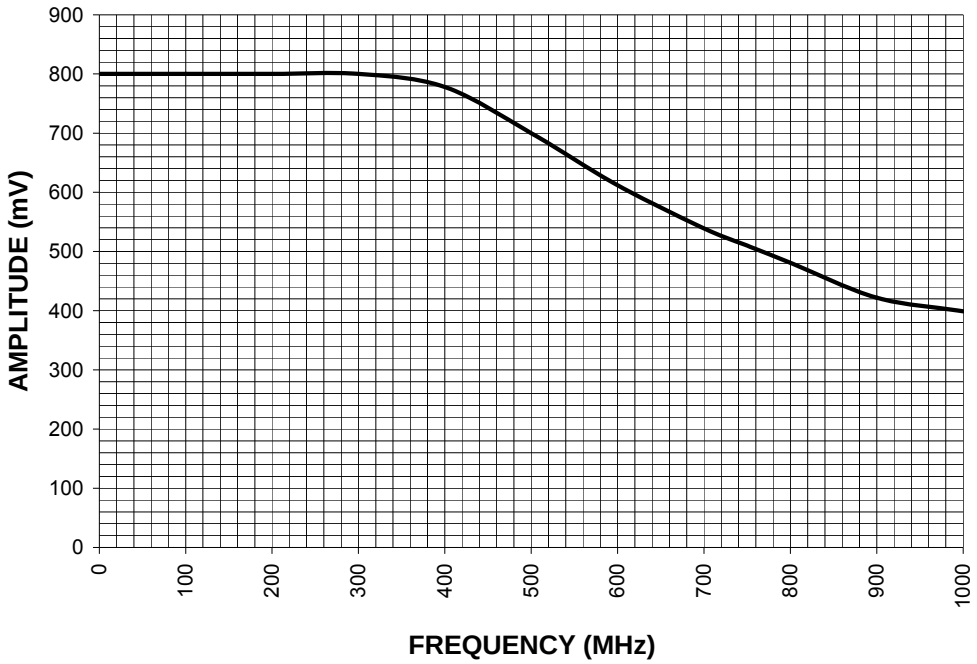


Figure 2. 500MHz Output Waveform

Frequency vs. Amplitude



hbwhelp@micrel.com or (408) 955-1690

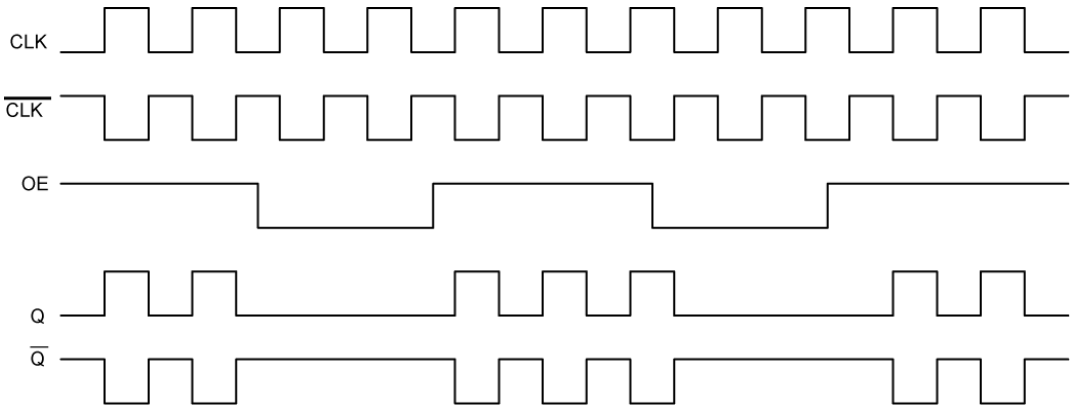
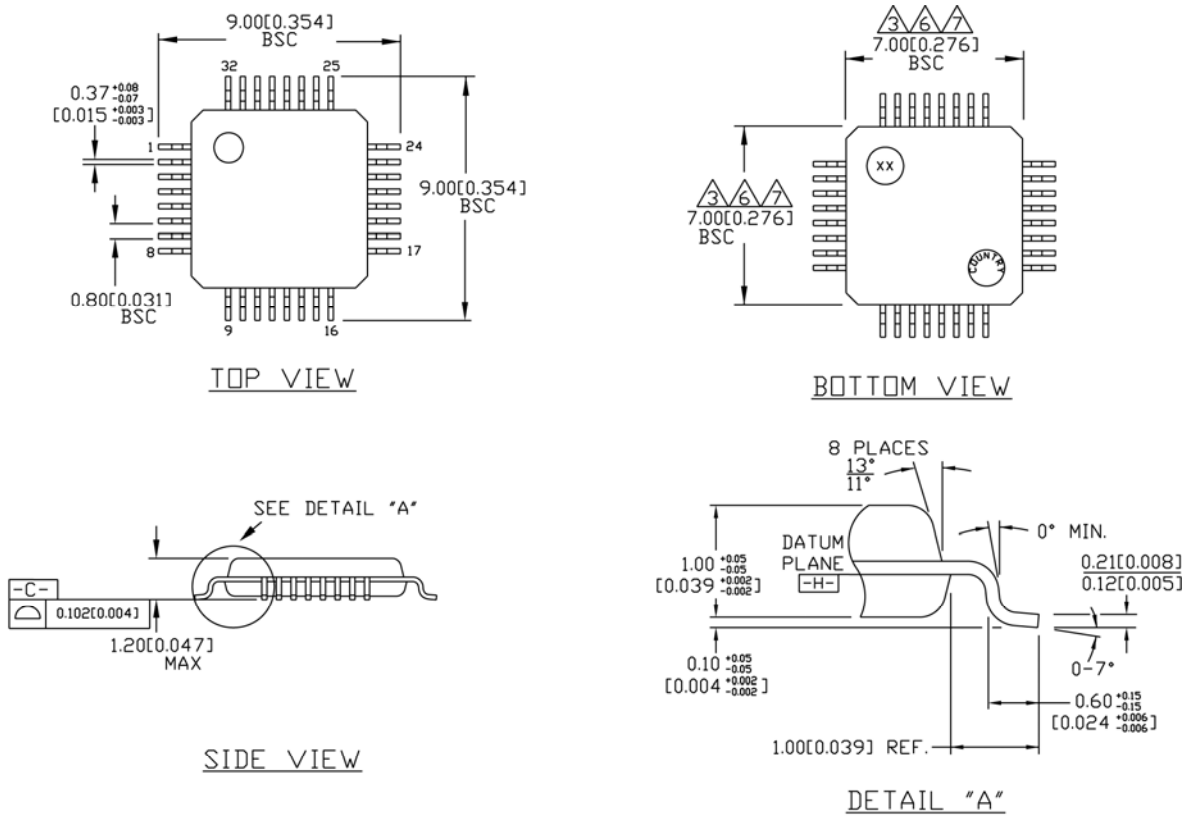


Figure 3. Output Enable Timing Diagram

Package Information



NOTES:
1. DIMENSIONS ARE IN MM[INCHES].
2. CONTROLLING DIMENSION: MM.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.254 [0.010].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN.
6. THESE DIMENSIONS TO BE DETERMINED AT DATUM PLANE -H-
7. PACKAGE TOP DIMENSIONS ARE SMALLER THAN BOTTOM DIMENSIONS AND TOP OF PACKAGE WILL NOT OVERHANG BOTTOM OF PACKAGE.

32-Pin TQFP (T32-1)

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http://www.micrel.com