NAU8501
24-bit Stereo Audio ADC with Differential Microphone Inputs

GENERAL DESCRIPTION

The NAU8501 is a low power, high quality audio input system for portable applications. In addition to precision 24-bit stereo ADCs, this device integrates a broad range of additional functions to simplify implementation of complete audio systems. The NAU8501 includes low-noise stereo differential high gain microphone inputs with wide range programmable amplifiers, separate line inputs, and an analog bypass/side tone line level stereo output.

Advanced on-chip digital signal processing includes a limiter/ALC (Automatic Level Control), 5-band equalizer, notch filter, and a high-pass filter for speech optimization and wind noise reduction. The digital interface can operate as either a master or a slave. Additionally, an internal Fractional-N PLL is available to accurately generate any audio sample rate clock for the ADCs derived using any available system clock from 8MHz through 33MHz.

The NAU8501 operates with analog supply voltages from 2.5V to 3.6V, while the digital core can operate as low as 1.7V to conserve power. Internal control registers enable flexible power conserving modes, shutting down or reducing power in sub-sections of the chip under software control.

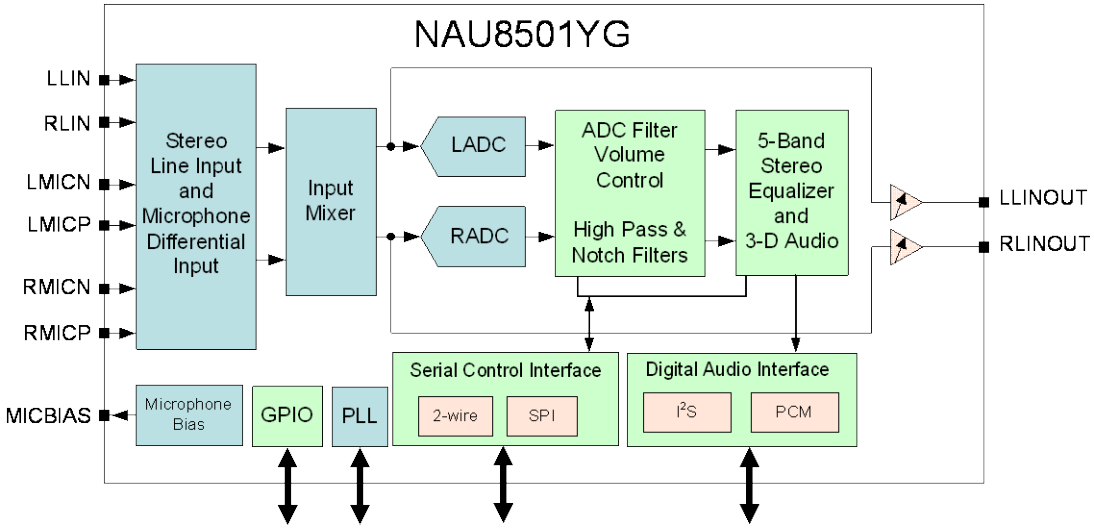
The NAU8501 is specified for operation from -40°C to +85°C. AEC-Q100 & TS16949 compliant device is available upon request.

FEATURES

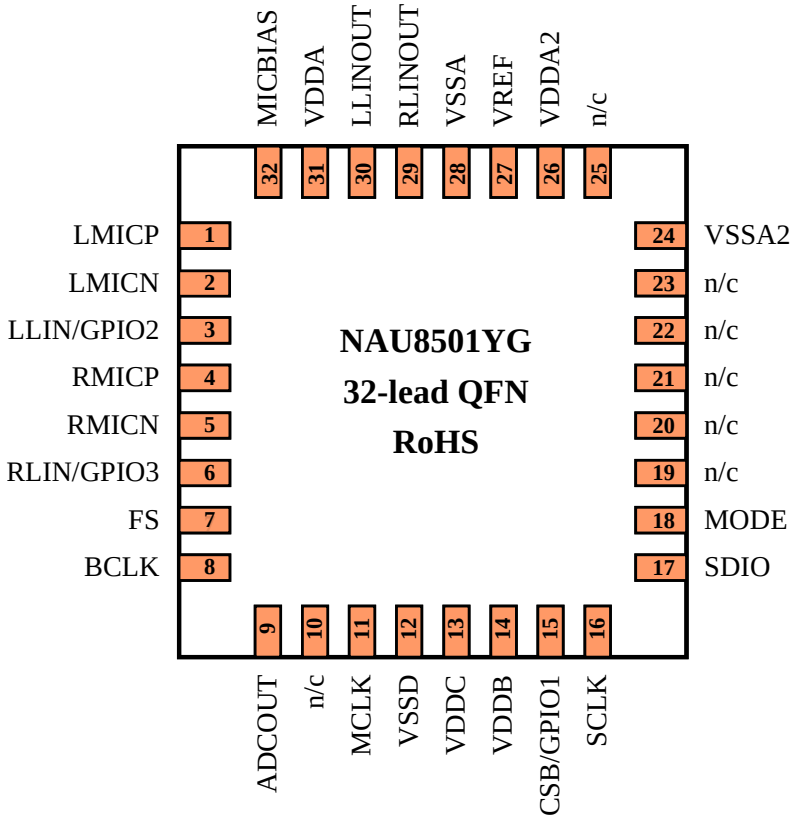
- ADC: 90dB SNR and -80dB THD ("A" weighted)
- Stereo differential input microphone amplifiers
- Very wide range programmable input amplifier
- Stereo line inputs with gain options and mixing
- Stereo line outputs with gain control and mute
- On-chip high resolution Fractional-N PLL
- Integrated DSP with specific functions:
  - 5-band equalizer
  - High pass filter / wind noise reduction
  - Automatic level control / limiter
  - Programmable notch filter
- Serial control interfaces with read/write capability
- Standard audio interfaces: PCM and I^2S
- Supports any sample rate from 8kHz to 48kHz
- Read/Write control register interface

Applications

- Audio Recording Devices
- Security Systems
- Video and Still Cameras
- Enhanced Audio Inputs for SOC products
- Audio Input Accessory Products
- Gaming Systems



Pinout



Part Number	Dimension	Package	Package Material
NAU8501YG	5 x 5 mm	32-QFN	Pb-Free

Pin Descriptions

Pin #	Name	Type	Functionality
1	LMICP	Analog Input	Left MICP Input (common mode)
2	LMICN	Analog Input	Left MICN Input
3	LLIN/GPIO2	Analog Input / Digital I/O	Left Line Input / alternate Left MICP Input / GPIO2
4	RMICP	Analog Input	Right MICP Input (common mode)
5	RMICN	Analog Input	Right MICN Input
6	RLIN/GPIO3	Analog Input / Digital I/O	Right Line Input/ alternate Right MICP Input / Digital Output In 4-wire mode: Must be used for GPIO3
7	FS	Digital I/O	Digital Audio DAC and ADC Frame Sync
8	BCLK	Digital I/O	Digital Audio Bit Clock
9	ADCOUT	Digital Output	Digital Audio ADC Data Output
10	n/c		Not internally connected
11	MCLK	Digital Input	Master Clock Input
12	VSSD	Supply	Digital Ground
13	VDDC	Supply	Digital Core Supply
14	VDDB	Supply	Digital Buffer (Input/Output) Supply
15	CSB/GPIO1	Digital I/O	3-Wire MPU Chip Select or General Purpose I/O
16	SCLK	Digital Input	3-Wire MPU Clock Input / 2-Wire MPU Clock Input
17	SDIO	Digital I/O	3-Wire MPU Data Input / 2-Wire MPU Data I/O
18	MODE	Digital Input	Control Interface Mode Selection Pin
19	n/c		Not internally connected
20	n/c		Not internally connected
21	n/c		Not internally connected
22	n/c		Not internally connected
23	n/c		Not internally connected
24	VSSA2	Supply	Secondary analog ground connection for minimum noise
25	n/c		Not internally connected
26	VDDA2	Supply	Secondary analog power connection for minimum noise
27	VREF	Reference	Decoupling for Midrail Reference Voltage
28	VSSA	Supply	Analog Ground
29	RLINOUT	Analog Output	Right Line Level Output
30	LLINOUT	Analog Output	Left Line Level Output
31	VDDA	Supply	Analog Power Supply
32	MICBIAS	Analog Output	Programmable Low Noise Supply for Microphone Biasing

Notes

1. The 32-QFN package includes a bulk ground connection pad on the underside of the chip. This bulk ground should be thermally tied to the PCB as much as possible, and electrically tied to the analog ground (VSSA, pin 28).
2. Unused analog input pins should be left as no-connection.
3. Unused digital input pins should be tied to ground.
4. Pins designated as NC (Not Internally Connected) should be left as no-connection

Block Diagram

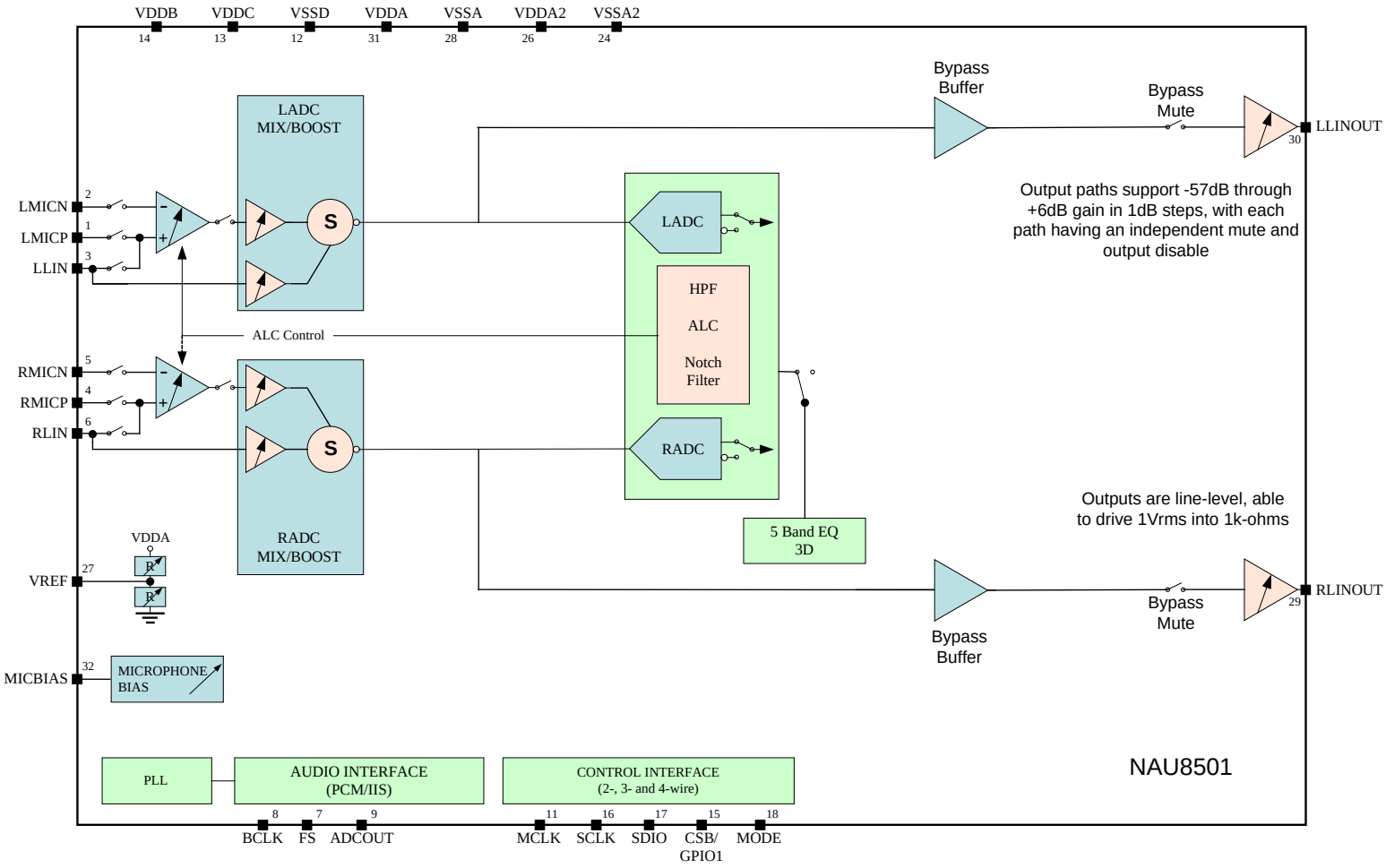


Figure 1: NAU8501 Block Diagram

Electrical Characteristics

Conditions: VDDC = 1.8V, VDDA = VDDB = VDDA2 = 3.3V, MCLK = 12.288MHz, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data, 64X oversampling rate, unless otherwise stated.

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Analog to Digital Converter (ADC)						
Full scale input signal [1]	V_{INFS}	PGABST = 0dB PGAGAIN = 0dB		1.0 0		Vrms dBV
Signal-to-noise ratio	SNR	Gain = 0dB, A-weighted	tbd	90		dB
Total harmonic distortion [2]	THD+N	Input = -3dB FS input		-80	tbd	dB
Channel separation		1kHz input signal		103		dB
Microphone Inputs (LMICP, LMICN, RMICP, RMICN, LLIN, RLIN) and Programmable Gain Amplifier (PGA)						
Full scale input signal [1]		PGABST = 0dB PGAGAIN = 0dB		1.0 0		Vrms dBV
Programmable gain			-12		35.25	dB
Programmable gain step size		Guaranteed Monotonic		0.75		dB
Mute Attenuation				120		dB
Input resistance		Inverting Input PGA Gain = 35.25dB PGA Gain = 0dB PGA Gain = -12dB Non-inverting Input Line Inputs Line Path Gain = +6dB Line In Gain = 0dB Line In Gain = -12dB		 1.6 47 75 94 20 40 159		 kΩ kΩ kΩ kΩ kΩ kΩ kΩ
Input capacitance				10		pF
PGA equivalent input noise		0 to 20kHz, Gain set to 35.25dB		120		µV
Input Boost Mixer						
Gain boost		Boost disabled Boost enabled		0 20		dB dB
Line Input to boost/mixer gain			-12		6	dB
Line Input step size to boost/mixer				3		dB
Microphone Bias						
Bias voltage	$V_{MICBIAS}$	See Figure 3		0.50, 0.60,0.65, 0.70, 0.75, 0.85, or 0.90		VDDA VDDA
Bias current source	$I_{MICBIAS}$			3		mA
Output noise voltage	V_n	1kHz to 20kHz		14		nV/√Hz

Electrical Characteristics, cont'd.

Conditions: VDDC = 1.8V, VDDA = VDDB = VDDA2 = 3.3V, MCLK = 12.288MHz, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data, 64X oversampling rate, unless otherwise stated.

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Line Output (RLINOUT and LLINOUT with 1k-Ω load)						
0dB full scale output voltage			VDDA / 3.3			V_{rms}
Signal-to-noise ratio	SNR	A-weighted		92		dB
Total harmonic distortion [2]	THD+N	VDDA = 3.3V		85		dB
Channel separation		1kHz signal		99		dB
Power supply rejection ratio (50Hz – 22kHz)	PSRR			53		dB
Automatic Level Control (ALC) and Limiter						
Target record level			-22.5		-1.5	dBFS
Programmable gain			-12		35.25	dB
Gain hold time [3]	t_{HOLD}	Doubles every gain step, with 16 steps total	0 / 2.67 / 5.33 / … / 43691			ms
Gain ramp-up (decay) [3]	t_{DCY}	ALC Mode ALC = 0	4 / 8 / 16 / … / 4096			ms
		Limiter Mode ALC = 1	1 / 2 / 4 / … / 1024			ms
Gain ramp-down (attack) [3]	t_{ATK}	ALC Mode ALC = 0	1 / 2 / 4 / … / 1024			ms
		Limiter Mode ALC = 1	0.25 / 0.5 / 1 / … / 128			ms
Mute Attenuation				120		dB
Digital Input/Output						
Input HIGH level	V_{IL}		0.7 * VDDB			V
Input LOW level	V_{IH}				0.3 * VDDB	V
Output HIGH level	V_{OH}	I_{Load} = 1mA	0.9 * VDDB			V
Output LOW level	V_{OL}	I_{Load} = -1mA			0.1 * VDDB	V
Input capacitance				10		pF

Notes

1. Full Scale is relative to the magnitude of VDDA and can be calculated as FS = VDDA/3.3.
2. Distortion is measured in the standard way as the combined quantity of distortion products plus noise. The signal level for distortion measurements is at 3dB below full scale, unless otherwise noted.
3. Time values scale proportionally with MCLK. Complete descriptions and definitions for these values are contained in the detailed descriptions of the ALC functionality.

Absolute Maximum Ratings

Condition	Min	Max	Units
VDDB, VDDC, VDDA, VDDA2 supply voltages	-0.3	+3.61	V
Core Digital Input Voltage range	VSSD – 0.3	VDDC + 0.30	V
Buffer Digital Input Voltage range	VSSD – 0.3	VDDB + 0.30	V
Analog Input Voltage range	VSSA – 0.3	VDDA + 0.30	V
Industrial operating temperature	-40	+85	°C
Storage temperature range	-65	+150	°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely influence product reliability and result in failures not covered by warranty.

Operating Conditions

Condition	Symbol	Min	Typical	Max	Units
Digital supply range (Core)	VDDC	1.65		3.60	V
Digital supply range (Buffer)	VDDB	1.65		3.60	V
Analog supply range	VDDA, VDDA2	2.50		3.60	V
Ground	VSSD VSSA VSSA2		0		V

1. VDDA must be ≥ VDDB.

2. VDDB must be ≥ VDDC.

Table of Contents

1 General Description

The NAU8501 is a stereo device with identical left and right channel differential microphone inputs, and also, line level inputs that share common support elements. Additionally, two-line level outputs are included that enable monitoring of the analog signals present at the ADC inputs. A powerful set of integrated programmable signal processing features are included.

1.1.1 Analog Inputs

All inputs include individual muting functions with excellent channel isolation and off-isolation from all outputs. All inputs are suitable for full quality, high bandwidth signals.

Each of the left-right stereo channels includes a low noise programmable differential PGA amplifier. This may be used for a microphone level through line level source signals. Gain may be set from +35.25db through -12dB at the analog difference-amplifier type programmable amplifier input stage. A separate additional 20dB analog gain is available on this input path, between the PGA output and ADC mixer input. The output of the ADC mixer may be routed to the ADC and/or analog bypass to the analog line level output section.

Each channel also has a line level input. This input may be routed to the input PGA non-inverting input, and/or mixed directly to the ADC input mixer. The mixing path into the ADC input mixer includes programmable gain from -12dB through +6dB in 3dB steps.

1.1.2 Analog Outputs

There are two-line level analog audio outputs. These outputs are useful for providing “side tone” in telephony applications, or more generally to monitor the analog input signal that is available at the input of the ADCs. Each output has an independently programmable gain function, output mute function, and output disable function. The gain can be programmed from -57dB through +6dB in 1dB steps.

A programmable low-noise MICBIAS microphone bias supply output is included. The VREF pin voltage reference is buffered and then scaled to provide a wide range of possible low-noise microphone bias DC voltages. This microphone bias supply is suitable for both conventional electret (ECM) type microphones, and to power the newer MEMS all-silicon type microphones. A small internal series resistance is optionally programmable at the output of the device. This greatly increases the effectiveness of the external output filter capacitor in reducing high frequency noise on the microphone bias output, and is a unique feature not present in most audio codec products.

1.1.3 ADC Function and Digital Signal Processing

Each left and right channel has an independent high quality ADC associated with it. These are high performance, 24-bit delta-sigma converters that are suitable for a very wide range of applications.

Each ADC is supported by an analog input mixer to select/mix the inputs available to that ADC. The output of the ADC is supported by an advanced digital signal processing subsystem (DSP) that enables a very wide range of programmable signal conditioning and signal optimizing functions. All digital processing is with 24-bit precision, as to minimize processing artifacts and maximize the audio dynamic range supported by the NAU8501.

The available DSP features include a wide range, mixed-mode Automatic Level Control (ALC), a high pass filter, a notch filter, scaling in decibels, and a digital mute function. All of these features are optional and highly programmable. The high pass filter function includes a very low frequency DC-blocking feature, or optionally, an application mode feature for low frequency audio noise reduction, such as to reduce unwanted ambient noise or "wind noise" on a microphone input. The notch filter may be programmed over a very wide frequency range and notch depth to greatly reduce a specific frequency band or frequency. Typically, this is used to reject a certain frequency such as a 50Hz, 60Hz, or 217Hz unwanted noise, but may also be used to eliminate an unwanted housing resonance or noise such as from camera motors.

Digital signal processing is also provided for a 3D Audio Enhancement function, and for a 5-Band Equalizer. These features are optional, and are programmable over wide ranges.

1.1.4 Digital Interfaces

Command and control of the device is accomplished using a 2-wire/3-wire/4-wire serial control interface. This is a simple, but highly flexible interface that is compatible with many commonly used command and control serial data protocols and host drivers.

Digital audio input/output data streams are transferred to and from the device separately from command and control. The digital audio data interface supports either I2S or PCM audio data protocols, and is compatible with commonly used industry standard devices that follow either of these two serial data formats.

1.1.5 Clock Requirements

The clocking signals required for the audio signal processing, audio data I/O, and control logic may be provided externally, or by optional operation of a built-in PLL (Phase Locked Loop).

The PLL is provided as a low cost, zero external component count optional method to generate required clocks in almost any system. The PLL is a fractional-N divider type design, which enables generating accurate desired audio sample rates derived from a very wide range of commonly available system clocks.

The frequency of the system clock provided as the PLL reference frequency may be any stable frequency in the range between 8MHz and 33MHz. Because the fractional-N multiplication factor is a very high precision 24-bit value, any desired sample rate supported by the NAU8501 can be generated with very high accuracy, typically limited by the accuracy of the external reference frequency. Reference clocks and sample rates outside of these ranges are also possible, but may involve performance tradeoffs and increased design verification.

2 Power Supply

This device has been designed to operate reliably using a wide range of power supply conditions and power-on/power-off sequences. There are no special requirements for the sequence or rate at which the various power supply pins change. Any supply can rise or fall at any time without harm to the device. However, pops and clicks may result from some sequences. Optimum handling of hardware and software power-on and power-off sequencing is described in more detail in the Applications section of this document.

2.1.1 Power-On Reset

The NAU8501 does not have an external reset pin. The device reset function is automatically generated internally when power supplies are too low for reliable operation. The internal reset is generated any time that either VDDA or VDDC is lower than is required for reliable maintenance of internal logic conditions. The reset threshold voltage for VDDA and VDDC is approximately 0.5Vdc. If both VDDA and VDDC are being reduced at the same time, the threshold voltage may be slightly lower. Note that these are much lower voltages than are required for normal operation of the chip. These values are mentioned here as general guidance as to overall system design.

If either VDDA or VDDC is below its respective threshold voltage, an internal reset condition is asserted. During this time, all registers and controls are set to the hardware determined initial conditions. Software access during this time will be ignored, and any expected actions from software activity will be invalid.

When both VDDA and VDDC reach a value above their respective thresholds, an internal reset pulse is generated which extends the reset condition for an additional time. The duration of this extended reset time is approximately 50 microseconds, but not longer than 100 microseconds. The reset condition remains asserted during this time. If either VDDA or VDDC at any time becomes lower than its respective threshold voltage, a new reset condition will result. The reset condition will continue until both VDDA and VDDC again higher than their respective thresholds. After VDDA and VDDC are again both greater than their respective threshold voltage, a new reset pulse will be generated, which again will extend the reset condition for not longer than an additional 100 microseconds.

2.1.2 Power Related Software Considerations

There is no direct way for software to determine that the device is actively held in a reset condition. If there is a possibility that software could be accessing the device sooner than 100 microseconds after the VDDA and VDDC supplies are valid, the reset condition can be determined indirectly. This is accomplished by writing a value to any register other than register 0x00, with that value being different than the power-on reset initial values. The optimum choice of register for this purpose may be dependent on the system design, and it is recommended the system engineer choose the register and register test bit for this purpose. After writing the value, software will then read back the same register. When the register test bit reads back as the new value, instead of the power-on reset initial value, software can reliably determine that the reset condition has ended.

Although it is not required, it is strongly recommended that a Software Reset command should be issued after power-on and after the power-on reset condition is ended. This will help insure reliable operation under every power sequencing condition that could occur.

If there is any possibility that VDDA or VDDC could be unreliable during system operation, software may be designed to monitor whether a power-on reset condition has happened. This can be accomplished by writing a test bit to a register that is different from the power-on initial conditions. This test bit should be a bit that is never used for any other reason, and does not affect desired operation in any way. Then, software at any time can read this bit to determine if a power-on reset condition has occurred. If this bit ever reads back other than the test value, then software can reliably know that a power-on reset event has occurred. Software can subsequently re-initialize the device and the system as required by the system design.

2.1.3 Software Reset

All chip registers can be reset to power-on default conditions by writing any value to register 0, using any of the control modes. Writing valid data to any other register disables the reset, but all registers need to have the correct operating data written. See the applications section on powering NAU8501 up for information on avoiding pops and clicks after a software reset.

3 Input Path Detailed Descriptions

The NAU8501 provides multiple inputs to acquire and process audio signals from microphones or other sources with high fidelity and flexibility. There are left and right input paths, each with three input pins, which can be used to capture signals from single-ended, differential or dual-differential microphones. These input channels each include a programmable gain amplifier (PGA). The outputs of the PGAs, plus two additional line level inputs, are then connected to the input boost/mix stages for maximum flexibility handling various signal sources.

All inputs are maintained at a DC bias at approximately ½ of the VDDA supply voltage. Connections to these inputs should be AC-coupled by means of DC blocking capacitors suitable for the device application.

3.1 Differential microphone input (MICN & MICP pins)

The NAU8501 features a low-noise, high common mode rejection ratio (CMRR), differential microphone input pair, MICP and MICN, which are connected to a PGA gain stage. The differential input structure is essential in noisy digital systems where amplification of low-amplitude analog signals is necessary such as in portable digital media devices and cell phones. Differential inputs very useful to reduce ground noise in systems in which there are ground voltage differences between different chips and other components. When properly implemented, the differential input architecture offers an improved power-supply rejection ratio (PSRR) and higher ground noise immunity.

3.2 Programmable Gain Amplifier (PGA)

Each PGA supports three possible inputs, MICP, MICN, and LIN. These are the microphone differential pair and a separate line level input. The PGA has a gain range of -12dB through +35.25dB in evenly spaced decibel increments of 0.75dB. Operation of the PGA is subject to control by the following registers:

R2 Power management controls for the left and right PGA
R2 Power management controls for ADC Mix/Boost (must be “on” for any PGA path to function)
R7 Zero crossing timeout control
R32 Automatic Level Control (ALC) for the left and right PGA
R44 Input selection options for the left and right PGA
R45 Volume (gain), mute, update bit, and zero crossing control for the left PGA
R46 Volume (gain), mute, update bit, and zero crossing control for the right PGA

Important: The R45 and R46 update bits are write-only bits. The primary intended purpose of the update bit is to enable simultaneous changes to both the left and right PGA volume values, even though these values must be written sequentially. When there is a write operation to either R45 or R46 volume settings, but the update bit is not set (value = 0), the new volume setting is stored as pending for the future, but does not go into effect. When there is a write operation to either R45 or R46 and the update bit is set (value = 1), then the new value in the register being written is immediately put into effect, and any pending value in the other PGA volume register is put into effect at the same time.

Note: If the ALC automatic level control is enabled, the function of the ALC is to automatically adjust the R45 or R46 volume setting. If ALC is enabled for the left or right, or both channels, then software should avoid changing the volume setting for the affected channel or channels. The reason for this is to avoid unexpected volume changes caused by competition between the ALC and the direct software control of the volume setting.

Zero-Crossing controls are implemented to suppress clicking sounds that may occur when volume setting changes take place while an audio input signal is active. When the zero crossing function is enabled (logic = 1), any volume change for the affected channel will not take place until the audio input signal passes through the zero point in its peak-to-peak swing. This prevents any instantaneous voltage change to the audio signal caused by volume setting changes. If the zero crossing function is disabled (logic = 0), volume changes take place instantly on condition of the Update Bit, but without regard to the instantaneous voltage level of the affected audio input signal.

The R7 zero crossing timeout control is an additional feature to limit the amount of time that a volume change to the PGA is delayed pending a zero crossing event. If the input signal is such that there are no zero crossing events, and the timeout control is enabled (level = 1), any new volume setting to either PGA will automatically be put into effect after between 2.5 and 3.5 periods of the Slow Timer Clock (see description under “Miscellaneous Functions”).

3.2.1 Zero Crossing Example

This drawing shows in a graphical form the problem and benefits of using the zero crossing feature. There is a major audible improvement as a result of using the zero crossing feature.

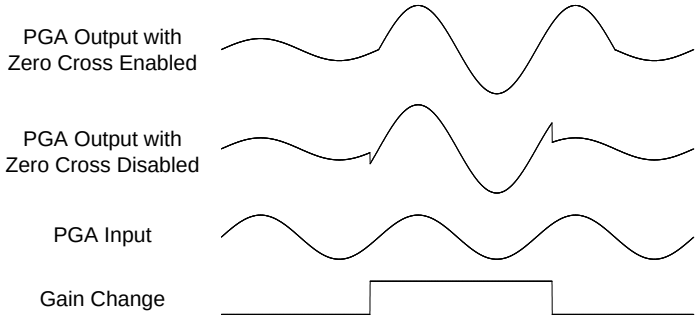


Figure 2: Zero Crossing Gain Update Operation

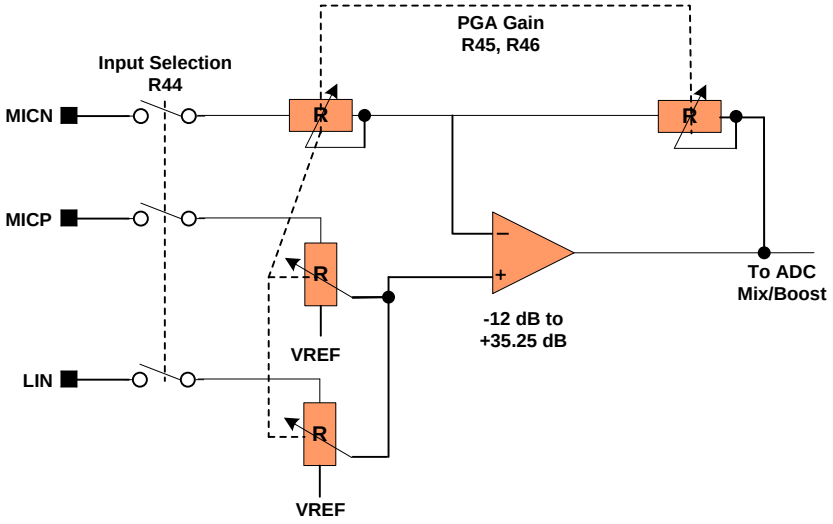


Figure 3: PGA Input Structure Simplified Schematic

3.3 Positive Microphone Input (MICP)

The positive (non-inverting) microphone input (MICP) can be used separately, or as part of a differential input configuration. This input pin connects to the positive (non-inverting) terminal of the PGA amplifier under control of register R44. When the R44 associated control bit is set (logic = 1), a switch connects MICP to the PGA input. When the associated control bit is not set (logic = 0), the MICP pin is connected to a resistor of approximately 30kΩ which is tied to VREF. The purpose of the tie to VREF is to reduce any pop or click sound by keeping the DC level of the MICP pin close to VREF at all times.

Note: If the MICP signal is not used differentially with MICN, the PGA gain values will be valid only if the MICN pin is terminated to a low impedance signal point. This termination should normally be an AC coupled path to signal ground.

This input impedance is constant regardless of the gain value. The nominal input impedance for this input is given by the following table. Impedance for specific gain values not listed in this table can be estimated through interpolation between listed values.

Nominal Input Impedance	Gain (dB)	Impedance (kΩ)
LMICP & RMICP to non-inverting PGA input or LLIN & RLIN to non-inverting PGA input	-12	94
	-9	94
	-6	94
	-3	94
	0	94
	3	94
	6	94
	9	94
	12	94
	18	94
	30	94
	35.25	94

Table 1: Microphone and Line Non-Inverting Input Impedances

3.4 Negative Microphone Input (MICN)

The negative (inverting) microphone input (MICN) can be used separately, or as part of a differential input configuration. This input pin connects to the negative (inverting) terminal of the PGA amplifier under control of register R44. When the R44 associated control bit is set (logic = 1), a switch connects MICP to the PGA input. When the associated control bit is not set (logic = 0), the MICN pin is connected to a resistor of approximately 30kΩ which is tied to VREF. The purpose of the tie to VREF is to reduce any pop or click sound by keeping the DC level of the MICN pin close to VREF at all times.

It is important for a system designer to know that the MICN input impedance varies as a function of the selected PGA gain. This is normal and expected for a difference amplifier type topology. The nominal resistive impedance values for this input over the possible gain range are given by the following table. Impedance for specific gain values not listed in this table can be estimated through interpolation between listed values.

Nominal Input Impedance	Gain (dB)	Impedance (kΩ)
LMICN or RMICN to inverting PGA input	-12	75
	-9	69
	-6	63
	-3	55
	0	47
	3	39
	6	31
	9	25
	12	19
	18	11
	30	2.9
	35.25	1.6

Table 2: Microphone Inverting Input Impedances

System designers should also note that at the highest gain values, the input impedance is relatively low. For most inputs, the best strategy if higher gain values are needed is to use the input PGA in combination with the +20dB gain boost available on the PGA Mix/Boost stage that immediately follows the PGA output. A good guideline is to use the PGA gain for up to around 20dB of gain. If more gain than this is required and the lower input impedance of the PGA at high gains is a problem, a combination of the PGA and boost stage should be used. In this type of

combined gain configuration, it is preferred to have at least 6dB gain at the PGA input stage to benefit from the PGA low noise characteristics.

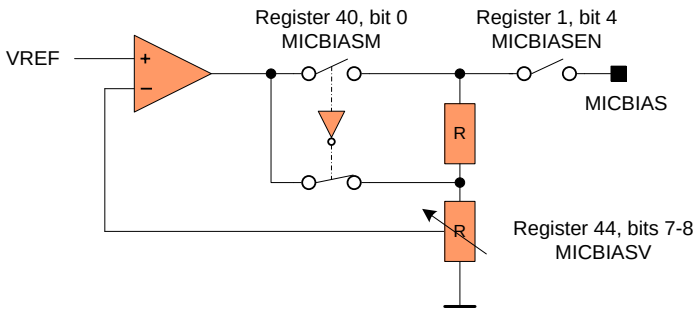
3.5 Microphone biasing

The MICBIAS pin provides a low-noise microphone DC bias voltage as may be required for operation of an external microphone. This built-in feature can typically provide up to 3mA of microphone bias current. This DC bias voltage is suitable for powering either traditional ECM (electret) type microphones, or for MEMS types microphones with an independent power supply pin.

Seven different bias voltages are available for optimum system performance, depending on the specific application. The microphone bias pin normally requires an external filtering capacitor as shown on the schematic in the Application section. The microphone bias function is controlled by the following registers:

R1 Power control for MICBIAS feature (enabled when bit 4 = 1)
R40 Optional low-noise mode and different bias voltage levels (enabled when bit 0 = 1)
R44 Primary MICBIAS voltage selection

The low-noise feature results in greatly reduced noise in the external MICBIAS voltage by placing a resistor of approximately 200-ohms in series with the output pin. This creates a low pass filter in conjunction with the external micbias filter capacitor, but without any additional external components. The low noise feature is enabled when the mode control bit 0 in register R40 is set (level = 1)



Register 44, Bits 7-8	Register 40, Bit 0	Microphone Bias Voltage
00	0	0.90 * VDDA
01	0	0.65 * VDDA
10	0	0.75 * VDDA
11	0	0.50 * VDDA
00	1	0.85 * VDDA
01	1	0.60 * VDDA
10	1	0.70 * VDDA
11	1	0.50 * VDDA

Figure 4: Microphone Bias Generator

3.6 Line Input Impedance and Variable Gain Stage Topology

Except for the input PGAs, other variable gain stages are implemented similarly to the simplified schematic shown here. The gain value changes affect input impedance in the ranges detailed in the description of each type of input path. If a path is in the “not selected” condition, then the input impedance will be in a high impedance condition. If an external input pin is not used anywhere in the system, it will be coupled to a DC tie-off of approximately 30kΩ coupled to VREF. The unused input/output tie-off function is explained in more detail in the Application Information section of this document.

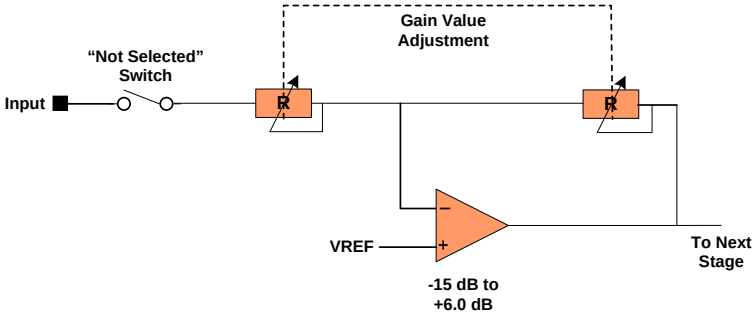


Figure 4: Variable Gain Stage Simplified Schematic

The input impedance presented to these inputs depends on the input routing choices and gain values. If an input is routed to more than one internal input node, then the effective input impedance will be the parallel combination of the impedance of the multiple nodes that are used. The impedance looking into the PGA non-inverting input is constant as listed in the section discussing the microphone input PGAs. The nominal resistive input impedances looking into the ADC Mix/Boost input inputs are listed in the following table:

Inputs	Gain (dB)	Impedance (kΩ)
LLIN & RLIN to L/RADC MIX/BOOST amp	Not Selected	High-Z
	-12	159
	-9	113
	-6	80
	-3	57
	0	40
	3	28
	6	20

Table 3: MIX/BOOST Amp Impedances

3.7 Left and Right Line Inputs (LLIN and RLIN)

A third possible input to the left or right PGA is an optional associated LIN left or right line level input. These inputs may be routed to the PGA non-inverting input, and/or connect directly to the ADC Mixer/Boost stage. If routed to the PGA, this signal is processed as an alternate pin for the MICP signal. LIN may be received differentially in relation to the MICN pin and has available the same gain range as for MICP. As in the operational case of using the MICP input, the MICN input must have a low impedance path to signal ground, so that the gain values chosen in the PGA are valid.

Note: It not recommended that both the LIN line input path to the PGA and the MICP path to the PGA be enabled at the same time. This will cause the differential gain to be unbalanced, and result in poor common mode rejection. Also, this will result in the LIN and MICP signals being connected together through internal chip resistors.

The line input pins, may alternatively be configured to operate as a GPIO (General Purpose Input/Output) logic input pin. This intended purpose is static logic voltage level sensing to determine if a headset is present or not as part of a physical detection of a possible external headset. Only one GPIO pin at any one time can be assigned for this purpose.

Registers that affect operation of the LLIN and RLIN inputs are:

R2 ADC Mix/Boost power control (must be “on” for any LIN path to function)
R9 GPIO selection for headset detect function
R44 PGA input selection control bits
If selected, all other PGA control registers (see PGA description)
R47 Left line input ADC Mix/Boost volume and mute (bits 4, 5, and 6)
R48 Right line input ADC Mix/Boost volume and mute (bits 4, 5, and 6)

3.8 ADC Mix/Boost Stage

The left and right channels each have an independent ADC Mix/Boost stage. The analog input signals must pass through the ADC Mix/Boost stage before use anywhere else in this device.

The ADC mixer stage has the LIN input and PGA output as its two inputs. The PGA input is an internal connection to the associated programmable gain amplifier servicing the microphone and line inputs.

Each input to the ADC Mix/Boost stage can be independently muted, and both inputs have independent gain controls. The LIN inputs have an available gain range of -12dB through +6dB in 3dB steps. The PGA input path has a choice of 0dB or 20dB of gain in addition to the gain in the PGA.

Registers that affect the ADC Mix/Boot stage are:

R2 Power control for left and right channels
R45 mute function for left channel PGA (bit 6 = 0 = muted condition)
R46 mute function for right channel PGA (bit 6 = 0 = muted condition)
R47 gain and mute control for left channel LIN path
R48 gain and mute control for right channel LIN path

3.9 Input Limiter / Automatic Level Control (ALC)

The input section of the NAU8501 is supported by additional combined digital and analog functionality which implement an Automatic Level Control (ALC) function. This can be very useful to automatically manage the analog input gain to optimize the signal level at the output of the programmable amplifier. The ALC can automatically amplify input signals that are too small, or decrease the amplitude if the signals are too loud. This system also helps to prevent clipping (overdrive) at the input of the ADC while maximizing the full dynamic range of the ADC.

The ALC may be operated in the normal mode just described, on in a special limiter mode of operation. The limiter mode is a faster mode of operation, the primary purpose of which is to limit too-loud signals. The limiter mode of operation is described after this section which provides details on the normal mode of operation.

The functional block architecture for the ALC is shown below. The ALC monitors the output of the ADC, measured after the digital decimator. The ADC output is fed into a peak detector, which updates the measured peak value whenever the absolute value of the input signal is higher than the current measured peak. The measured peak gradually decays to zero unless a new peak is detected, allowing for an accurate measurement of the signal envelope. The peak value is used by a logic algorithm to determine whether the PGA input gain should be increased, decreased, or remain the same.

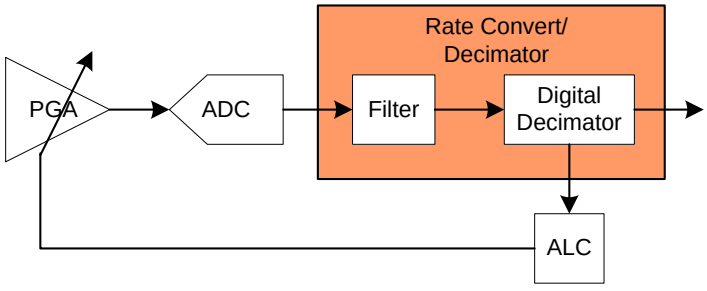


Figure 5: ALC Block Diagram

3.9.1 Normal Mode Example Operation

Immediately following is a simple example of the ALC operation. In the steady state at the beginning of the example time sequence, the PGA gain is at a steady value which results in the desired output level from the ADC. When the input signal suddenly becomes louder, the ALC reduces volume at a register determined rate and step size. This continues until the output level of the ADC is again at the desired target level. When the input signal suddenly becomes quiet, the ALC increases volume at a register determined rate and step size. When the output level from the ADC again reaches the target level, and now the input remains at a constant level, the ALC remains in a steady state.

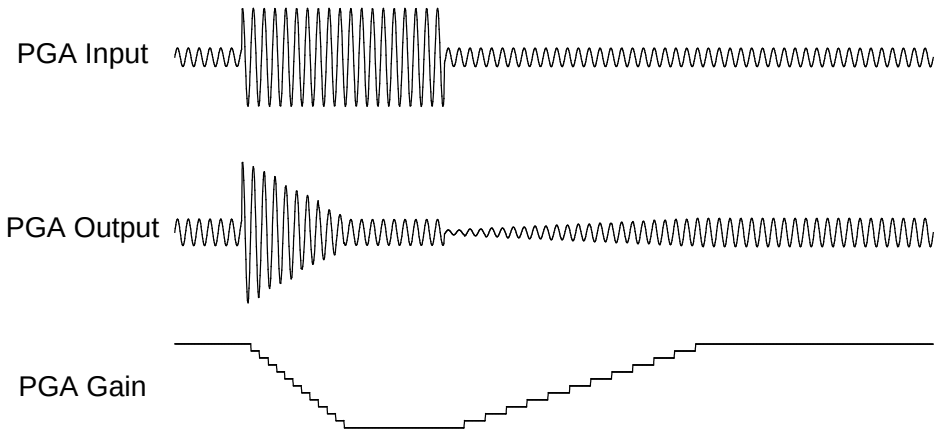


Figure 6: ALC Normal Mode Operation

3.9.2 ALC Parameter Definitions

Automatic level and volume control features are complex and have difficult to understand traditional names for many features and controls. This section defines some terms so that the explanations of this subsystem are more clear.

ALC Maximum Gain: Register 32 (ALCMXGAIN) This sets the maximum allowed gain in the PGA during normal mode ALC operation. In the Limiter mode of ALC operation, the ALCMXGAIN value is not used. In the Limiter mode, the maximum gain allowed for the PGA is set equal to the pre-existing PGA gain value that was in effect at the moment in time that the Limiter mode is enabled.

ALC Minimum Gain: Register 32 (ALCMNGAIN) This sets the minimum allowed gain in the PGA during all modes of ALC operation. This is useful to keep the AGC operating range close to the desired range for a given application scenario.

ALC Target Value: Register 33 (ALCSL) Determines the value used by the ALC logic decisions comparing this fixed value with the output of the ADC. This value is expressed as a fraction of Full Scale (FS) output from the ADC. Depending on the logic conditions, the output value used in the comparison may be either the instantaneous value of the ADC, or otherwise a time weighted average of the ADC peak output level.

ALC Attack Time: Register 34 (ALCATK) Attack time refers to how quickly a system responds to an increasing volume level that is greater than some defined threshold. Typically, attack time is much faster than decay time. In the NAU8501, when the absolute value of the ADC output exceeds the ALC Target Value, the PGA gain will be reduced at a step size and rate determined by this parameter. When the peak ADC output is at least 1.5dB lower than the ALC Target Value, the stepped gain reduction will halt.

ALC Decay Time: Register 34 (ALCDCY) Decay time refers to how quickly a system responds to a decreasing volume level. Typically, decay time is much slower than attack time. When the ADC output level is below the ALC Target value by at least 1.5dB, the PGA gain will increase at a rate determined by this parameter. The decay time constant is determined by the setting in register 34, bits 4 to 7 (ALCDCY), which sets the delay between increases in gain. In Limiter mode, the time constants are faster than in ALC mode. (See Detailed Register Map.)

ALC Hold Time Register 33 (ALCHLD) Hold time refers to a duration of time when no action is taken. This is typically to avoid undesirable sounds that can happen when an ALC responds too quickly to a changing input signal. The use and amount of hold time is very application specific. In the NAU8501, the hold time value is the duration of time that the ADC output peak value must be less than the target value before there is an actual gain increase.

3.10 ALC Peak Limiter Function

To reduce clipping and other bad audio effects, all ALC modes include a peak limiter function. This implements an emergency PGA gain reduction when the ADC output level exceeds a built-in maximum value. When the ADC output exceeds 87.5% of full scale, the ALC block ramps down the PGA gain at the maximum ALC Attack Time rate, regardless of the mode and attack rate settings, until the ADC output level has been reduced below the emergency limit threshold. This limits ADC clipping if there is a sudden increase in the input signal level.

3.10.1 ALC Normal Mode Example Using ALC Hold Time Feature

Input signals with different characteristics (e.g., voice vs. music) may require different settings for this parameter for optimum performance. Increasing the ALC hold time prevents the ALC from reacting too quickly to brief periods of silence such as those that may appear in music recordings; having a shorter hold time, may be useful in voice applications where a faster reaction time helps to adjust the volume setting for speakers with different volumes. The waveform below shows the operation of the ALCHLD parameter.

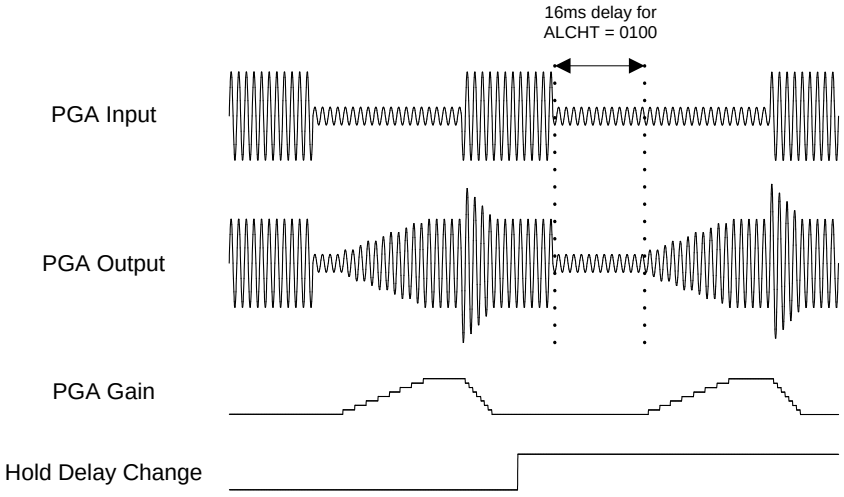


Figure 7: ALC Hold Delay Change

3.11 Noise Gate (Normal Mode Only)

A noise gate threshold prevents ALC amplification of noise when there is no input signal, or no signal above an expected background noise level. The noise gate is enabled by setting register 35, bit 3 (NGEN), HIGH, and the threshold level is set in register 35, bits 0 to 2 (NGTH). This does not remove noise from the signal; when there is no signal or a very quiet signal (pause) composed mostly of noise, the ALC holds the gain constant instead of amplifying the signal towards the target threshold. The NAU8501 accomplishes this by comparing the input signal level against the noise gate threshold. The noise gate only operates in conjunction with the ALC and only in Normal mode. The noise gate is asserted when:

Equation 1: (Signal at ADC – PGA gain – MIC Boost gain) < NGTH (Noise Gate Threshold Level)

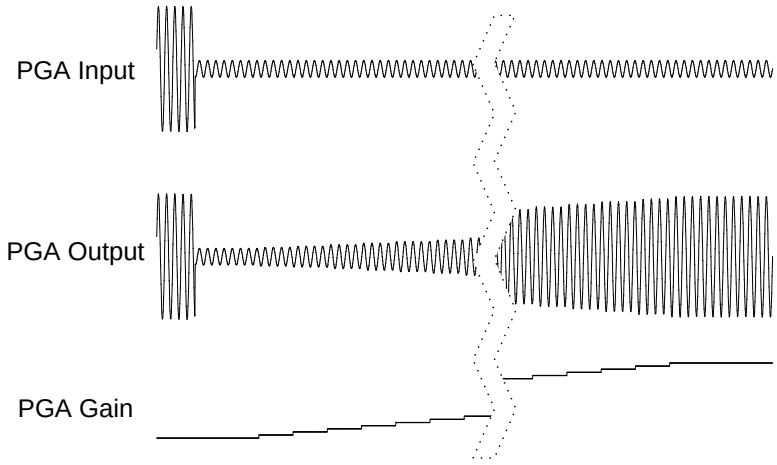


Figure 8: ALC Operation Without Noise Gate

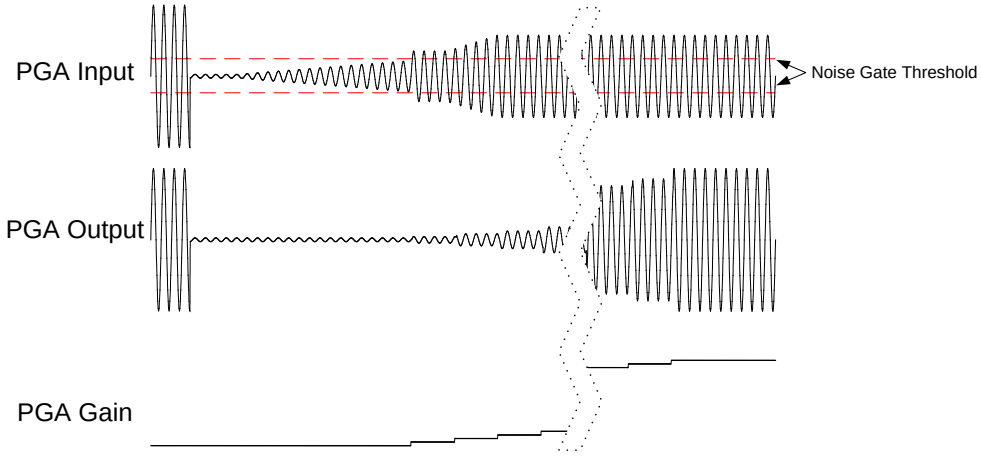
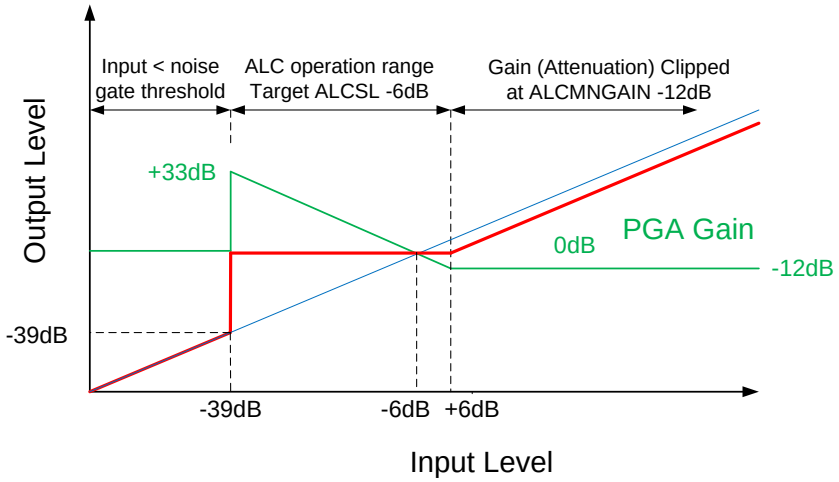


Figure 9: Noise Gate Operation

3.12 ALC Example with ALC Min/Max Limits and Noise Gate Operation

The drawing below shows the effects of ALC operation over the full scale signal range. The drawing is color coded to be more clear as follows:

Blue Original Input signal (linear line from zero to maximum)
Green PGA gain value over time (inverse to signal in target range)
Red Output signal (held to a constant value in target range)



Register	Bits	Name	Value	Description
32	7-8	ALCSEL	11	ALC enabled both channels
32	3-5	ALCMAXGAIN	111	Max ALC gain @ 35.25dB
32	0-2	ALCMINGAIN	000	Min ALC gain @ -12dB
33	0-3	ALCLVL	1011	Target ALC gain @ -6dBFS
35	3	NGEN	1	Noise gate enabled
35	0-2	NGTH	000	Noise gate @ -39dB

Figure 10: ALC Response Envelope

3.12.1 ALC Register Map Overview

ALC can be enabled for either or both the left and right ADC channels. All ALC functions and mode settings are common to the left and right channels. When either the right or left PGA is disabled, the respective PGA will remain at the most recent gain value as set by the ALC. Registers that control the ALC features and functions are:

R32 Enable left/right ALC functions; set maximum gain, minimum gain
R33 ALC hold time, ALC target signal level
R34 ALC limiter mode selection, attack parameters, decay parameters
R35 Enable noise gate, noise gate parameters
R70 Selection of signal level averaging options and ALC table options
R70 Realtime readout of left channel gain value in use by ALC (same as left in stereo operation)
R71 Realtime readout of right channel gain value in use by ALC (same as right in stereo operation)
R76 Realtime readout of input signal level from averaging peak-to-peak input signal detector
R77 Realtime readout of input signal level from averaging input signal peak detector

The following table shows some of the ALC parameter values and their ranges. The complete list of settings and values is included in the Detailed Register Map.

Parameter	Register	Bits	Name	Default Setting	Value	Programmable Range
Minimum Gain of PGA	32	0-2	ALCMINGAIN	000	-12dB	Range: -12dB to +30dB @ 6dB increments
Maximum Gain of PGA	32	3-5	ALCMAXGAIN	111	35.25dB	Range: -6.75dB to +35.25dB @ 6dB increments
ALC Function	32	7-8	ALCEN	00	Disabled	00 = Disable 01 = Enable right channel 10 = Enable left channel 11 = Enable both channels
ALC Target Level	33	0-3	ALCLVL	1011	-6dBFS	Range: -22.5dB to -1.5dBFS @ 1.5dB increments
ALC Hold Time	33	4-7	ALCHLD	0000	0ms	Range: 0ms to 1024ms at 1010 and above (times are for 0.75dB steps, and double with every step)
ALC Attack time	34	0-3	ALCATK	0010	500µs	ALCM=0 – Range: 125µs to 128ms ALCM=1 – Range: 31µs to 32ms (times are for 0.75dB steps, and double with every step)
ALC Decay Time	34	4-7	ALCDCY	0011	4ms	ALCM = 0 – Range: 500µs to 512ms ALCM = 1 – Range: 125µs to 128ms (times are for 0.75dB steps, and double with every step)
Limiter Function	34	8	ALCMODE	0	Disabled	0 = ALC mode 1 = Limiter mode

Table 4: Registers associated with ALC and Limiter Control

3.13 Limiter Mode

When register 34, bit 8, is HIGH and ALC is enabled in register 32, bits 7-8 (ALCEN), the ALC block operates in limiter mode. In this mode, the PGA gain is constrained to be less than or equal to the PGA gain setting when the limiter mode is enabled. In addition, attack and decay times are faster in limiter mode than in normal mode as indicated by the different lookup tables for these parameters for limiter mode. The following waveform illustrates the behavior of the ALC in limiter mode in response to changes in various ALC parameters.

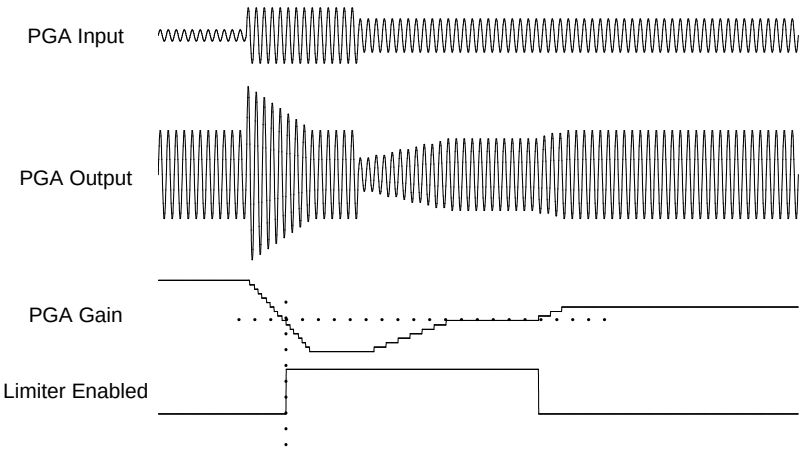
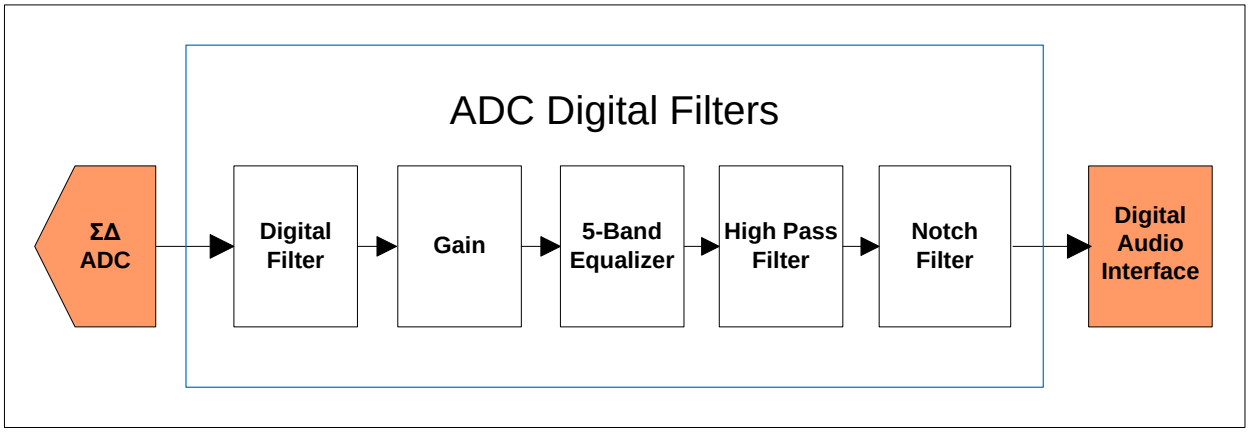


Figure 11: ALC Limiter Mode Operation

4 ADC Digital Block



The ADC digital block performs 24-bit analog-to-digital conversion and signal processing, making available a high quality audio sample stream the audio path digital interface. This block consists of a sigma-delta modulator, digital decimator/ filter, 5-band graphic equalizer, 3D effects, high pass filter, and a notch filter. The equalizer and 3D audio function block is a single resource that may be used by either the ADC or DAC, but not both at the same time. The ADC coding scheme is in twos complement format and the full-scale input level is proportional to VDDA. With a 3.3V supply voltage, the full-scale level is $1.0V_{RMS}$.

Registers that affect the ADC operation are:

R2 Power management enable/disable left/right ADC
R5 Digital passthrough of ADC output data into DAC input
R7 Sample rate indication bits (affect filter frequency scaling)
R14 Oversampling, polarity inversion, and filter controls for left/right ADC
R14 ADC high pass filter Audio Mode or Application Mode selection
R15 Left channel ADC digital volume control and update bit function
R16 Right channel ADC digital volume control and update bit function

4.1 Sampling / Oversampling Rate, Polarity Control, Digital Passthrough

The audio sample rate of the ADC is determined entirely by the IMCLK internal Master Clock frequency, which is 128 times the base audio sample rate. A technique known as oversampling is used to improve noise and distortion performance of the ADC, but this does not affect the final audio sample rate. The default oversampling rate of the ADC is 64X (64 times the audio sample rate), but this can be changed to 128X for greatly improved audio performance. The higher rate increases power consumption by only approximately three milliwatts per channel, so for most applications, the improved quality is a good choice. There is almost zero increased power to also run the DACs at 128X oversampling, and the best overall quality will be achieved when both the DACs and ADCs are operated at the same oversampling rate.

The polarity of either ADC output signal can be changed independently on either ADC logic output as a feature sometimes useful in management of the audio phase. This feature can help minimize any audio processing that may be otherwise required as the data are passed to other stages in the system.

Digital audio passthrough allows the output of the ADCs to be directly sent to the DACs as the input signal to the DAC for DAC output. In this mode of operation, the output data from the ADCs are still available on the ADCOUT logic pin. However, any external input signal for the DAC will be ignored. The passthrough function is useful for many test and application purposes, and the DAC output may be utilized in any way that is normally supported for the DAC analog output signals.

4.2 ADC Digital Volume Control and Update Bit Functionality

The effective output audio volume of each ADC can be changed using the digital volume control feature. This processes the output of the ADC to scale the output by the amount indicated in the volume register setting. Included is a "digital mute" value which will completely mute the signal output of the ADC. The digital volume setting can range from 0dB through -127dB in 0.5dB steps.

Important: The R15 and R16 update bits are write-only bits. The primary intended purpose of the update bit is to enable simultaneous changes to both the left and right ADC volume values, even though these values must be written sequentially. When there is a write operation to either R15 or R16 volume settings, but the update bit is not set (value = 0), the new volume setting is stored as pending for the future, but does not go into effect. When there is a write operation to either R15 or R16 and the update bit is set (value = 1), then the new value in the register being written is immediately put into effect, and any pending value in the other ADC volume register is put into effect at the same time.

4.3 ADC Programmable High Pass Filter

Each ADC is optionally supported by a high pass filter in the digital output path. Filter operation and settings are always the same for both left and right channels. The high pass filter has two different operating modes. In the audio mode, the filter is a simple first order DC blocking filter, with a cut-off frequency of 3.7Hz. In the application specific mode, the filter is a second order audio frequency filter, with a programmable cut-off frequency. The cutoff frequency of the high pass filter is scaled depending on the sampling frequency indicated to the system by the setting in Register 7.

Registers that affect operation of the programmable high pass filter are:

R7 Sample rate indication to the system (affects filter coefficient internal scaling)
R14 High-pass enable/disable, operating mode, and cut-off frequency

The following table provides the exact cutoff frequencies with different sample rates as indicated to the system by means of Register 7. The table shows the assumed actual numerical sample rates as determined by the system clocks. Detailed response curves are provided in the Appendix section of this document.

Register 14, bits 4 to 6 (HPF)	Sample Rate in kHz (FS)								
	R7(SMPLR) = 101 or 100			R7(SMPLR) = 011 or 010			R7(SMPLR) = 001 or 000		
	8	11.025	12	16	22.05	24	32	44.1	48
000	82	113	122	82	113	122	82	113	122
001	102	141	153	102	141	153	102	141	153
010	131	180	156	131	180	156	131	180	156
011	163	225	245	163	225	245	163	225	245
100	204	281	306	204	281	306	204	281	306
101	261	360	392	261	360	392	261	360	392
110	327	450	490	327	450	490	327	450	490
111	408	563	612	408	563	612	408	563	612

Table 5: High Pass Filter Cut-off Frequencies in Hz (with HPFAM register 14, bit 7 = 1)

4.4 Programmable Notch Filter

Each ADC is optionally supported by a notch filter in the digital output path. Filter operation and settings are always the same for both left and right channels. A notch filter is useful to a very narrow band of audio frequencies in a stop band around a given center frequency. The notch filter is enabled by setting register 27, bit 7 (NFCEN), to 1. The center frequency is programmed by setting registers 27, 28, 29, and 30, bits 0 to 6 (NFA0[13:7], NFA0[6:0], NFA1[13:7], NFA1[6:0]), with two's compliment coefficient values calculated using table __.

Registers that affect operation of the notch filter are:

R27 Notch filter enable/disable
R27 Notch filter a0 coefficient high order bits and update bit
R28 Notch filter a0 coefficient low order bits and update bit
R29 Notch filter a1 coefficient high order bits and update bit
R30 Notch filter a1 coefficient low order bits and update bit

Important: The register update bits are write-only bits. The update bit function is important so that all filter coefficients actively being used are changed simultaneously, even though these register values must be written sequentially. When there is a write operation to any of the filter coefficient settings, but the update bit is not set (value = 0), the value is stored as pending for the future, but does not go into effect. When there is a write operation to any coefficient register, and the update bit is set (value = 1), then the new value in the register being written is immediately put into effect, and any pending coefficient value is put into effect at the same time.

Coefficient values are in the form of 2's-complement integer values, and must be calculated based upon the desired filter properties. The mathematical operations for calculating these coefficients are detailed in the following table.

A_0	A_1	Notation	Register Value (DEC)
$\frac{1-\tan\left(\frac{2\ \pi\ f_b}{2\ f_s}\right)}{1+\tan\left(\frac{2\ \pi\ f_b}{2\ f_s}\right)}$	$-\left(1+A_0\right)\ x\ \cos\left(\frac{2\ \pi\ f_c}{f_s}\right)$	f_c = center frequency (Hz) f_b = -3dB bandwidth (Hz) f_s = sample frequency (Hz)	NFCA0 = $-A_0 \times 2^{13}$ NFCA1 = $-A_1 \times 2^{12}$ Note: Values are rounded to the nearest whole number and converted to 2's complement

Table 6: Equations to calculate notch filter coefficients

4.5 5-Band Equalizer

The NAU8501 includes a 5-band graphic equalizer with low distortion, low noise, and wide dynamic range. The equalizer is applied to both left and right channels. The equalizer is grouped with the 3D Stereo Enhancement signal processing function. Both functions may be assigned to support either the ADC path, or the DAC path, but not both paths simultaneously.

Registers that affect operation of the 5-Band Equalizer are:

R18 Assign equalizer to DAC path or to ADC path (default = ADC path)
R18 Band 1 gain control and cut-off frequency
R19 Band 2 gain control, center cut-off frequency, and bandwidth
R20 Band 3 gain control, center cut-off frequency, and bandwidth
R21 Band 4 gain control, center cut-off frequency, and bandwidth
R22 Band 5 gain control and cut-off frequency

Each of the five equalizer bands is independently adjustable for maximum system flexibility, and each offers up to 12dB of boost and 12dB of cut with 1dB resolution. The high and the low bands are shelving filters (high-pass and low-pass, respectively), and the middle three bands are peaking filters. Details of the register value settings are described below. Response curve examples are provided in the Appendix of this document.

Register Value	Equalizer Band				
	1 (High Pass) Register 18 Bits 5 & 6 EQ1CF	2 (Band Pass) Register 19 Bits 5 & 6 EQ2CF	3 (Band Pass) Register 20 Bits 5 & 6 EQ3CF	4 (Band Pass) Register 21 Bits 5 & 6 EQ4CF	5 (Low Pass) Register 22 Bits 5 & 6 EQ5CF
00	80Hz	230Hz	650Hz	1.8kHz	5.3kHz
01	105Hz	300Hz	850Hz	2.4kHz	6.9kHz
10	135Hz	385Hz	1.1kHz	3.2kHz	9.0kHz
11	175Hz	500Hz	1.4kHz	4.1kHz	11.7kHz

Table 7: Equalizer Center/Cutoff Frequencies

Register Value		Gain	Registers
Binary	Hex		
00000	00h	+12db	Bits 0 to 4 in registers 18 (EQ1GC) 19 (EQ2GC) 20 (EQ3GC) 21 (EQ4GC) 22 (EQ5GC)
00001	01h	+11dB	
00010	02h	+10dB	
- - -	- -	Increments 1dB per step	
01100	0Ch	0dB	
01101	17h	-11dB	
- - -	- -	Increments 1dB per step	
11000	18h	-12dB	
11001 to 11111	19h to 1Fh	Reserved	

Table 8: Equalizer Gains

4.6 3D Stereo Enhancement

NAU8501 includes digital circuitry to provide flexible 3D enhancement to increase the perceived separation between the right and left channels, and has multiple options for optimum acoustic performance. The equalizer is grouped with the 3D Stereo Enhancement signal processing function. Both functions may be assigned to support either the ADC path, or the DAC path, but not both paths simultaneously.

Registers that affect operation of 3D Stereo Enhancement are:

R18 Assign equalizer to DAC path or to ADC path (default = ADC path)
R41 3D Audio depth enhancement setting

The amount of 3D enhancement applied can be programmed from the default 0% (no 3D effect) to 100% in register 41, bits 0 to 3 (DEPTH3D), as shown in Table __. Note: 3D enhancement uses increased gain to achieve its effect, so that the source signal may need to be attenuated by up to 6dB to avoid clipping.

Register 41 Bits 0 to 3 3DDEPTH	3D Effect
0000	0%
0001	6.7%dB
0010	13.4%dB
- - -	Increments 6.67% for each binary step in the input word
1110	93.3%
1111	100%

Table 9: 3D Enhancement Depth

4.7 Companding

Companding is used in digital communication systems to optimize signal-to-noise ratios with reduced data bit rates, using non-linear algorithms. These compress wide-range linear audio data into an 8-bit quasi-logarithmic quantization. The compressed data are then transmitted over a network, and then expanded back again into linear audio data. NAU8501 supports the compression feature of the two main telecommunications companding standards: A-law and µ-law. The A-law algorithm is primarily used in European communication systems and the µ-law algorithm is primarily used by North America, Japan, and Australia. . Companding converts 13-bits (µ-law) or 12-bits (A-law) of linear PCM codes into 8-bits using non-linear quantization, and then back again into linear PCM codes. The companded signal is an 8-bit word containing a sign (1-bit), exponent (3-bits) and mantissa (4-bits)

Following are the data compression equations set in the ITU-T G.711 standard and implemented in the NAU8501:

4.8 µ-law

$F(x) = \ln(1 + \mu|x|) / \ln(1 + \mu)$ $-1 \le x \le 1$

with µ=255 for the U.S. and Japan

4.9 A-law

$F(x) = A|x| / (1 + \ln A)$ for $x \le 1/A$

$F(x) = (1 + \ln A|x|) / (1 + \ln A)$ for $1/A \le x \le 1$

with A=87.6 for Europe

The register affecting companding operation is:

R5 Enable 8-bit mode; enable ADC companding

The compressed signal is an 8-bit word consisting of a sign bit, three bits for the exponent, and four bits for the mantissa. When compression is enabled, the PCM interface must be set to an 8-bit word length. When in 8-bit mode, the Register 4 word length control (WLEN) is ignored.

Compression Mode	Register 5			
	Bit 4	Bit3	Bit 2	Bit 1
No Compression (default)	0	0	0	0
ADC 1- law µ-law			 1 1	 1 0

Table 10: Companding Control

4.10 8-bit Word Length

Writing a 1 to register 5, bit 5 (CMB8), will cause the PCM interface to use 8-bit word length for data transfer, overriding the word length configuration setting in WLEN (register 4, bits 5 and 6.).

5 Analog Outputs

There are two line level analog audio outputs. These outputs are useful for monitoring the analog input signal that is available at the input of the ADCs. Each output has an independently programmable gain function, output mute function, and output disable function. The gain can be programmed from -24dB through +6dB in 2dB steps.

These outputs are derived from the signals at the inputs of the two ADC converters. These signals are then buffered, optionally muted, and then passed to the line level output driver.

Registers that affect operation of the line level output path are:

R3 Power control for the left and right internal buffer amplifier
R50 left AUX and ADC Mix/Boost source select, and gain settings
R51 right AUX and ADC Mix/Boost source select, and gain settings

5.1 Line Level Outputs (LLINOUT and RLINOUT)

These are high quality general purpose output drivers intended for driving medium impedance loads such as inputs to other amplifiers (such as a headphone amplifier) and long signal lines. The signal source for each of these outputs is from the associated left and right internal buffer from the inputs to the ADCs. Power for this section is provided from the VDDA pin.

Each driver may be selectively enabled/disabled as part of the power management features, and each output can be individually controlled over a gain range of -57dB through +6dB in 1dB steps. Gain changes for the two outputs can be coordinated through use of an update bit feature as part of the register controls. Additionally, clicks that could result from gain changes can be suppressed using an optional zero crossing feature.

Registers that affect the line outputs are:

R2 Power management control for the left and right line output amplifier
R52 Volume, mute, update, and zero crossing controls for left line output driver
R53 Volume, mute, update, and zero crossing controls for right line output driver

Important: The R52 and R53 update bits are write-only bits. The primary intended purpose of the update bit is to enable simultaneous changes to both the left and right line output volume values, even though these two register values must be written sequentially. When there is a write operation to either R52 or R53 volume settings, but the update bit is not set (value = 0), the new volume setting is stored as pending for the future, but does not go into effect. When there is a write operation to either R52 or R53 and the update bit is set (value = 1), then the new value in the register being written is immediately put into effect, and any pending value in the other line output volume register is put into effect at the same time.

Zero-Crossing controls are implemented to suppress clicking sounds that may occur when volume setting changes take place while an audio input signal is active. When the zero crossing function is enabled (logic = 1), any volume change for the affected channel will not take place until the audio input signal passes through the zero point in its peak-to-peak swing. This prevents any instantaneous voltage change to the audio signal caused by volume setting changes. If the zero crossing function is disabled (logic = 0), volume changes take place instantly on condition of the Update Bit, but without regard to the instantaneous voltage level of the affected audio input signal.

6 Miscellaneous Functions

6.1 Slow Timer Clock

An internal Slow Timer Clock is supplied to automatically control features that happen over a relatively periods of time, or time-spans. This enables the NAU8501 to implement long time-span features without any host/processor management or intervention.

Two features are supported by the Slow Timer Clock. These are an optional automatic time out for the zero-crossing holdoff of PGA volume changes, and timing for debouncing of the mechanical jack detection feature. If either feature is required, the Slow Timer Clock must be enabled.

The Slow Timer Clock is initialized in the disabled state. The Slow Timer Clock is controlled by only the following register:

R7 Sample rate indication select, and Slow Timer Clock enable

The Slow Timer Clock rate is derived from MCLK using an integer divider that is compensated for the sample rate as indicated by the R7 sample rate register. If the sample rate register value precisely matches the actual sample rate, then the internal Slow Timer Clock rate will be a constant value of 128ms. If the actual sample rate is, for example, 44.1kHz and the sample rate selected in R7 is 48kHz, the rate of the Slow Timer Clock will be approximately 10% slower in direct proportion of the actual vs. indicated sample rate. This scale of difference should not be important in relation to the dedicated end uses of the Slow Timer Clock.

6.2 General Purpose Inputs and Outputs (GPIO1, GPIO2, GPIO3) and Jack Detection

Three pins are provided in the NAU8501 that may be used for limited logic input/output functions. GPIO1 has multiple possible functions, and may be either a logic input or logic output. GPIO2 and GPIO3 may be either line level analog inputs, or logic inputs dedicated to the purpose of jack detection. GPIO2 and GPIO3 do not have any logic output capability or function. Only one GPIO can be selected for jack detection.

If a GPIO is selected for the jack detection feature, the Slow Timer Clock must be enabled. The jack detection function is automatically "debounced" such that momentary changes to the logic value of this input pin are ignored. The Slow Timer Clock is necessary for the debouncing feature.

Registers that control the GPIO functionality are:

R8 GPIO functional selection options
R9 Jack Detection feature input selection and functional options

If a GPIO is selected for the jack detection function, the required Slow Timer Clock determines the duration of the time windows for the input logic debouncing function. Because the logic level changes happen asynchronously to the Slow Timer Clock, there is inherently some variability in the timing for the jack detection function. A continuous and persistent logic change on the GPIO pin used for jack detection will result in a valid internal output signal within 2.5 to 3.5 periods of the Slow Timer Clock. Any logic change of shorter duration will be ignored.

The threshold voltage for a jack detection logic-low level is no higher than 1.0Vdc. The threshold voltage for a jack detection logic-high level is no lower than 1.7Vdc. These levels will be reduced as the VDDC core logic voltage pin is reduced below 1.9Vdc.

If the RLIN or LLIN input pin is used for the GPIO function, the analog signal path should be configured to be disconnected from its respective PGA input. This will not cause harm to the device, but could cause unwanted noise introduced through the PGA path.

6.3 Automated Features Linked to Jack Detection

Some functionality can be automatically controlled by the jack detection logic. This feature can be used to enable the internal analog amplifier bias voltage generator, and/or enable analog output drivers automatically as a result of detecting a logic change at a GPIO pin assigned to the purpose of jack detection. This eliminates any requirement for the host/processor to perform these functions.

The internal analog amplifier bias generator creates the VREF voltage reference and bias voltage used by the analog amplifiers. The ability to control it is a power management feature. This is implemented as a logical "OR" function of either the debounced internal jack detection signal, or the ABIASEN control bit in Register 1. The bias generator will be powered if either of these control signals is enabled (value = 1).

Power management control of the line outputs is also optionally and selectively subject to control linked with the jack detection signal. Register settings determine which outputs may be enabled, and whether they are enabled by a logic 1 or logic 0 value. Output control is a logical "AND" operation of the jack detection controls, and of the register control bits that normally control the outputs. Both controls must be in the "ON" condition for a given output to be enabled.

Registers that affect these functions are:

R9 GPIO pin selection for jack detect function, jack detection enable, VREF jack enable
R13 bit mapped selection of which outputs are to be enabled when jack detect is in a logic 1 state
R13 bit mapped selection of which outputs are to be enabled when jack detect is in a logic 0 state

7 Clock Selection and Generation

The NAU8501 has two basic clock modes that support the ADC data converters. It can accept external clocks in the slave mode, or in the master mode, it can generate the required clocks from an external reference frequency using an internal PLL (Phase Locked Loop). The internal PLL is a fractional type scaling PLL, and therefore, a very wide range of external reference frequencies can be used to create accurate audio sample rates.

Separate from this ADC clock subsystem, audio data are clocked to and from the NAU8501 by means of the control logic described in the Digital Audio Interfaces section. The audio bit rate and audio sample rate for this data flow are managed by the Frame Sync (FS) and Bit Clock (BCLK) pins in the Digital Audio Interface.

It is important to understand that the sampling rate for the ADC data converters is not determined by the Digital Audio Interface, and instead, this rate is derived exclusively from the Internal Master Clock (IMCLK). It is therefore a requirement that the Digital Audio Interface and data converters be operated synchronously, and that the FS, BCLK, and IMCLK signals are all derived from a common reference frequency. If these three clocks signals are not synchronous, audio quality will be reduced.

The IMCLK is always exactly 256 times the sampling rate of the data converters.

IMCLK is output from the Master Clock Prescaler. The prescaler reduces by an integer division factor the input frequency input clock. The source of this input frequency clock is either the external MCLK pin, or the output from the internal PLL Block.

Registers that are used to manage and control the clock subsystem are:

R1 Power management, enable control for PLL (default = disabled)
R6 Master/slave mode, clock scaling, clock selection
R7 Sample rate indication (scales DSP coefficients and timing – does NOT affect actual sample rate
R8 MUX control and division factor for PLL output on GPIO1
R36 PLL Prescaler, Integer portion of PLL frequency multiplier
R37 Highest order bits of 24-bit fraction of PLL frequency multiplier
R38 Middle order bits of 24-bit fraction of PLL frequency multiplier
R39 Lowest order bits of 24-bit fraction of PLL frequency multiplier

In Master Mode, the IMCLK signal is used to generate FS and BCLK signals that are driven onto the FS and BCLK pins and input to the Digital Audio Interface. FS is always IMCLK/256 and the duty cycle of FS is automatically adjusted to be correct for the mode selected in the Digital Audio Interface. The frequency of BCLK may optionally be divided to optimize the bit clock rate for the application scenario.

In Slave Mode, there is no connection between IMCLK and the FS and BCLK pins. In this mode, FS and BLCK are strictly input pins, and it is the responsibility of the system designer to insure that FS, BCLK, and IMCLK are synchronous and scaled appropriately for the application.

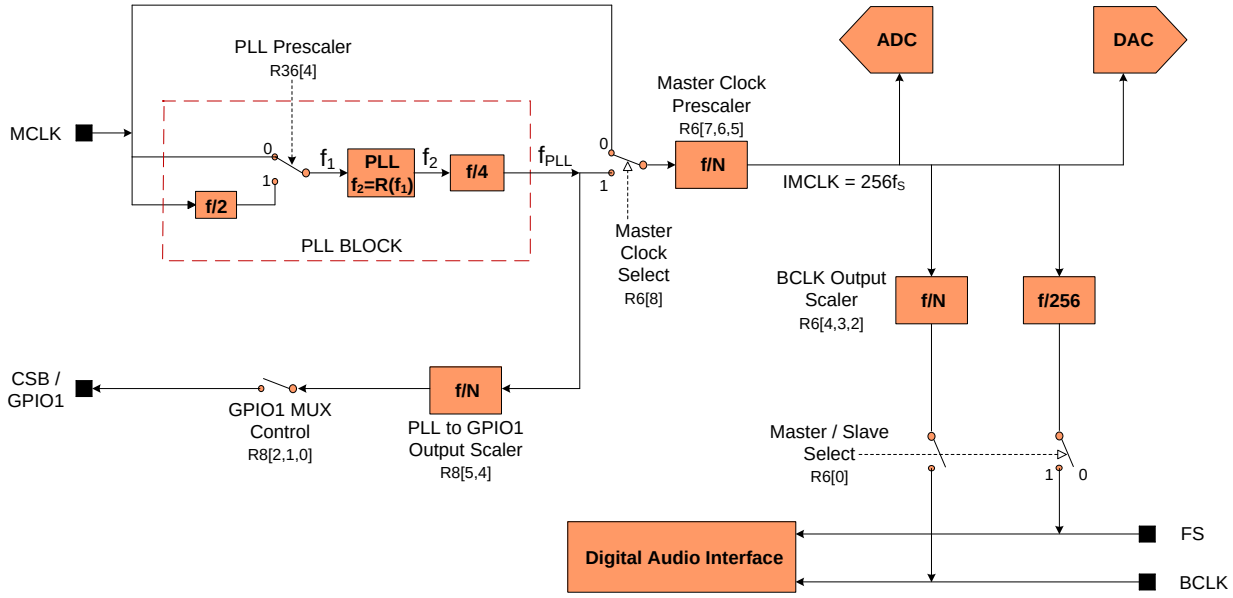


Figure 12: PLL and Clock Select Circuit

7.1 Phase Locked Loop (PLL) General Description

The PLL may be optionally used to multiply an external input clock reference frequency by a high resolution fractional number. To enable the use of the widest possible range of external reference clocks, the PLL block includes an optional divide-by-two prescaler for the input clock, a fixed divide-by-four scaler on the PLL output, and an additional programmable integer divider that is the Master Clock Prescaler.

The high resolution fraction for the PLL is the ratio of the desired PLL oscillator frequency (f_2), and the reference frequency at the PLL input (f_1). This can be represented as $R = f_2/f_1$, with R in the form of a decimal number: xy.abcdefgh. To program the NAU8501, this value is separated into an integer portion ("xy"), and a fractional portion, "abcdefgh". The fractional portion of the multiplier is a value that when represented as a 24-bit binary number (stored in three 9-bit registers on the NAU8501), very closely matches the exact desired multiplier factor.

To keep the PLL within its optimal operating range, the integer portion of the decimal number ("xy"), must be any of the following decimal values: 6, 7, 8, 9, 10, 11, or 12. The input and output dividers outside of the PLL are often helpful to scale frequencies as needed to keep the "xy" value within the required range. Also, the optimum PLL oscillator frequency is in the range between 90MHz and 100MHz, and thus, it is best to keep f_2 within this range.

In summary, for any given design, choose:

- IMCLK = desired Master Clock = (256)*(desired codec sample rate)
- f_2 = (4)*(P)(IMCLK), where P is the Master Clock Prescale integer value; optimal f_2: 90MHz< f_2 <100MHz
- f_1 = (MCLK)/(D), where D is the PLL Prescale factor of 1, or 2, and MCLK is the frequency at the MCLK pin
  note: The integer values for D and P are chosen to keep the PLL in its optimal operating range. It may be best to assign initial values of 1 to both D and P, and then by inspection, determine if they should be a different value.
- $R = f_2/f_1$ = xy.abcdefgh decimal value, which is the fractional frequency multiplication factor for the PLL
- N = xy truncated integer portion of the R value, and limited to decimal value 6, 7, 8, 9, 10, 11, or 12
- $K = (2^{24})*(0.abcdefgh)$, rounded to the nearest whole integer value, then converted to a binary 24-bit value
- R36 is set with the whole number integer portion, N, of the multiplier
- R37, R38, R39 are set collectively with the 24-bit binary fractional portion, K, of the multiplier
- R36 PLL Prescaler set as necessary
- R6 Master Clock Prescaler and BCLK Output Scaler set as necessary

7.1.1 Phase Locked Loop (PLL) Design Example

In an example application, a desired sample rate for the ADC is known to be 48.000kHz. Therefore, it is also known that the IMCLK rate will be 256fs, or 12.288MHz. Because there is a fixed divide-by-four scaler on the PLL output, then the desired PLL oscillator output frequency will be 49.152MHz.

In this example system design, there is already an available 12.000MHz clock from the USB 36ubsystem. To reduce system cost, this clock will also be used for audio. Therefore, to use the 12MHz clock for audio, the desired fractional multiplier ratio would be R = 49.152/12.000 = 4.096. This value, however, does not meet the requirement that the "xy" whole number portion of the multiplier be in the inclusive range between 6 and 12. To meet the requirement, the Master Clock Prescaler can be set for an additional divide-by-two factor. This now makes the PLL required oscillator frequency 98.304 MHz, and the improved multiplier value is now R = 98.304/12.000 = 8.192.

To complete this portion of the design example, the integer portion of the multiplier is truncated to the value, 8. The fractional portion is multiplied by 2^{24}, as to create the needed 24-bit binary fractional value. The calculation for this is: $(2^{24})(0.192) = 3221225.472$. It is best to round this value to the nearest whole value of 3221225, or hexadecimal 0x3126E9. Thus, the values to be programmed to set the PLL multiplier whole number integer and fraction are:

```
R36  0xnm8   ; integer portion of fraction,  (nm represents other settings in R36)
R37  0x00C   ; highest order 6-bits of 24-bit fraction
R38  0x093   ; middle 9-bits of 24-bit fraction
R39  0x0E9   ; lowest order 9-bits of 24-bit fraction
```

Below are additional examples of results for this calculation applied to commonly available clock frequencies and desired IMCLK 256fs sample rates.

MCLK (MHz)	Desired 256fs IMCLK rate (MHz)	PLL oscillator f_2 (MHz)	PLL Prescaler divider	Master Clock divider	Fractional Multiplier R = f_2/f_1	Integer Portion N (Hex)	Fractional Portion K (Hex)
12.0	11.28960	90.3168	1	2	7.526400	7	86C226
12.0	12.28800	98.3040	1	2	8.192000	8	3126E9
14.4	11.28960	90.3168	1	2	6.272000	6	45A1CA
14.4	12.28800	98.3040	1	2	6.826667	6	D3A06D
19.2	11.28960	90.3168	2	2	9.408000	9	6872B0
19.2	12.28800	98.3040	2	2	10.240000	A	3D70A3
19.8	11.28960	90.3168	2	2	9.122909	9	1F76F8
19.8	12.28800	98.3040	2	2	9.929697	9	EE009E
24.0	11.28960	90.3168	2	2	7.526400	7	86C226
24.0	12.28800	98.3040	2	2	8.192000	8	3126E9
26.0	11.28960	90.3168	2	2	6.947446	6	F28BD4
26.0	12.28800	98.3040	2	2	7.561846	7	8FD526

Table 11: PLL Frequency Examples

7.2 CSB/GPIO1 as PLL output

CSB/GPIO1 is a multi-function pin that may be used for a variety of purposes. If not required for some other purpose, this pin may be configured to output the clock frequency from the PLL subsystem. This is the same frequency that is available from the PLL subsystem as the input to the Master Clock Prescaler. This frequency may be optionally divided by an additional integer factor of 2, 3, or 4, before being output on GPIO1.

8 Control Interfaces

8.1 Selection of Control Mode

The NAU8501 features include a serial control bus that provides access to all of the device control registers. This bus may be configured either as a 2-wire interface that is interoperable with industry standard implementations of the I2C serial bus, or as a 3-wire/4-wire bus compatible with commonly used industry implementations of the SPI (Serial Peripheral Interface) bus.

Mode selection is accomplished by means of combination of the MODE control logic pin, and the SPIEN control bit in Register 7 or Register 73. The following table shows the three functionally different modes that are supported.

MODE Pin	SPIEN bit R7[8]	Description
0	0	2-Wire Interface, Read/Write operation
1	X "don't care"	SPI Interface 3-Wire Write-only operation
0	1	SPI Interface 4-Wire Read operation SPI Interface 4-Wire Write operation

Table 12: Control Interface Selection

The timing in all three bus configurations is fully static. This results in good compatibility with standard bus interfaces, and also, with software simulated buses. A software simulated bus can be very simple and low cost, such as by utilizing general purpose I/O pins on the host controller and software "bit banging" techniques to create the required timing.

8.2 2-Wire-Serial Control Mode (I^2C Style Interface)

The 2-wire bus is a bidirectional serial bus protocol. This protocol defines any device that sends data onto the bus as a transmitter (or master), and the receiving device as the receiver (or slave). The NAU8501 can function only as a slave device when in the 2-wire interface configuration.

8.3 2-Wire Protocol Convention

All 2-Wire interface operations must begin with a START condition, which is a HIGH-to-LOW transition of SDIO while SCLK is HIGH. All 2-Wire interface operations are terminated by a STOP condition, which is a LOW to HIGH transition of SDIO while SCLK is HIGH. A STOP condition at the end of a read or write operation places the device in a standby mode.

An acknowledge (ACK), is a software convention is used to indicate a successful data transfer. To allow for the ACK response, the transmitting device releases the SDIO bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDIO line LOW to acknowledge the reception of the eight bits of data.

Following a START condition, the master must output a device address byte. This consists of a 7-bit device address, and the LSB of the device address byte is the R/W (Read/Write) control bit. When R/W=1, this indicates the master is initiating a read operation from the slave device, and when R/W=0, the master is initiating a write operation to the slave device. If the device address matches the address of the slave device, the slave will output an ACK during the period when the master allows for the ACK signal.

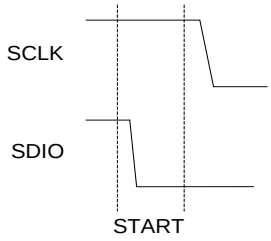


Figure 13: Valid START Condition

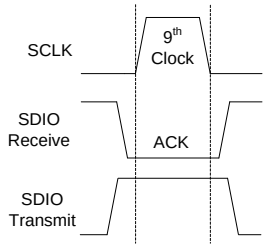


Figure 14: Valid Acknowledge

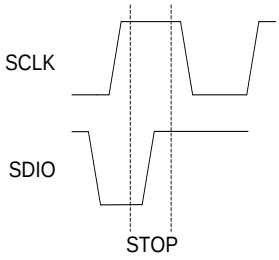


Figure 15: Valid STOP Condition

0	0	1	1	0	1	0	R/W	Device Address Byte
A7	A6	A5	A4	A3	A2	A1	A0	Control Address Byte
D7	D6	D5	D4	D3	D2	D1	D0	Data Byte

Figure 16: Slave Address Byte, Control Address Byte, and Data Byte

8.4 2-Wire Write Operation

A Write operation consists of a two-byte instruction followed by one or more Data Bytes. A Write operation requires a START condition, followed by a valid device address byte with R/W=0, a valid control address byte, data byte(s), and a STOP condition.

The NAU8501 is permanently programmed with “0011010” as the Device Address. If the Device Address matches this value, the NAU8501 will respond with the expected ACK signaling as it accepts the data being transmitted into it.

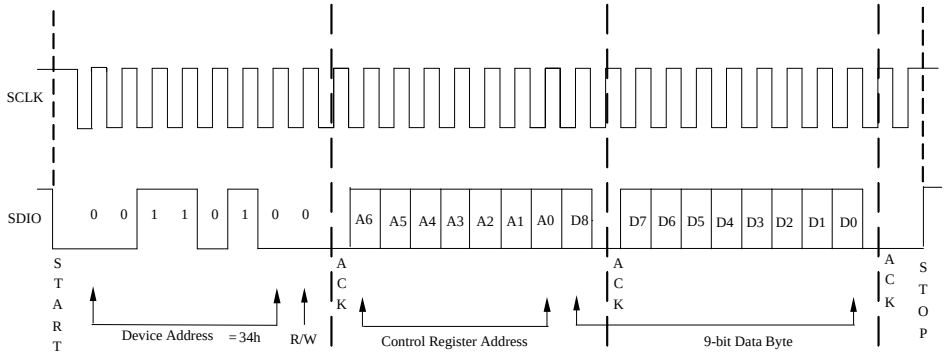


Figure 17: Byte Write Sequence

8.5 2-Wire Read Operation

A Read operation consists of a three-byte Write instruction followed by a Read instruction of one or more data bytes. The bus master initiates the operation issuing the following sequence: a START condition, device address byte with the R/W bit set to "0", and a Control Register Address byte. This indicates to the slave device which of its control registers is to be accessed.

The NAU8501 is permanently programmed with "0011010" as its device address. If the device address matches this value, the NAU8501 will respond with the expected ACK signaling as it accepts the Control Register Address being transmitted into it. After this, the master transmits a second START condition, and a second instantiation of the same device address, but now with R/W=1.

After again recognizing its device address, the NAU8501 transmits an ACK, followed by a two byte value containing the nine bits of data from the selected control register inside the NAU8501. Unused bits in the byte containing the MSB information from the NAU8501 are output by the NAU8501 as zeros.

During this phase, the master generates the ACK signaling with each byte transferred from the NAU8501. If there is no STOP signal from the master, the NAU8501 will internally auto-increment the target Control Register Address and then output the two data bytes for this next register in the sequence.

This process will continue as long as the master continues to issue ACK signaling. If the Control Register Address being indexed inside the NAU8501 reaches the value 0x7F (hexadecimal) and the value for this register is output, the index will roll over to 0x00. The data bytes will continue to be output until the master terminates the read operation by issuing a STOP condition.

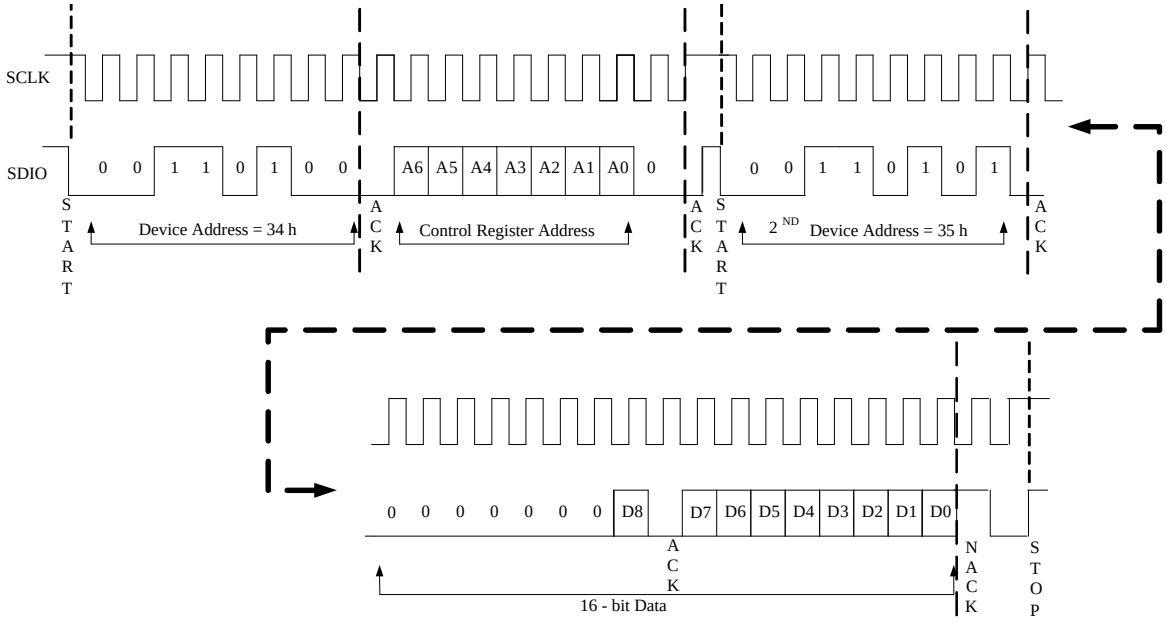


Figure 18: Read Sequence

8.6 SPI Control Interface Modes

The Serial Peripheral Interface (SPI) is a widely utilized interface protocol, and the NAU8501 supports two modes of SPI operation. When the MODE pin on the NAU8501 is in a logic HIGH condition, the device operates in the SPI 3-wire Write Mode. This is a write-only mode with a 16-bit transaction size. If the MODE pin is in a logic LOW condition, and the SPIEN control bit is set in Register 5, the SPI 4-wire Read/Write modes are enabled.

8.7 SPI 3-Wire Write Operation

Whenever the MODE pin on the NAU8501 is in the logic HIGH condition, the device control interface will operate in the 3-Wire Write mode. This is a write-only mode that does not require the fourth wire normally used to read data from a device on an SPI bus implementation. This mode is a 16-bit transaction consisting of a 7-bit Control Register Address, and 9-bits of control register data. In this mode, SDIO data bits are clocked continuously into a temporary holding register on each rising edge of SCLK, until the CSB pin undergoes a LOW-to-HIGH logic transition. At the time of the transition, the most recent 16-bits of data are latched into the NAU8501, with the 9-bit data value being written into the NAU8501 control register addressed by the Control Register Address portion of the 16-bit value.

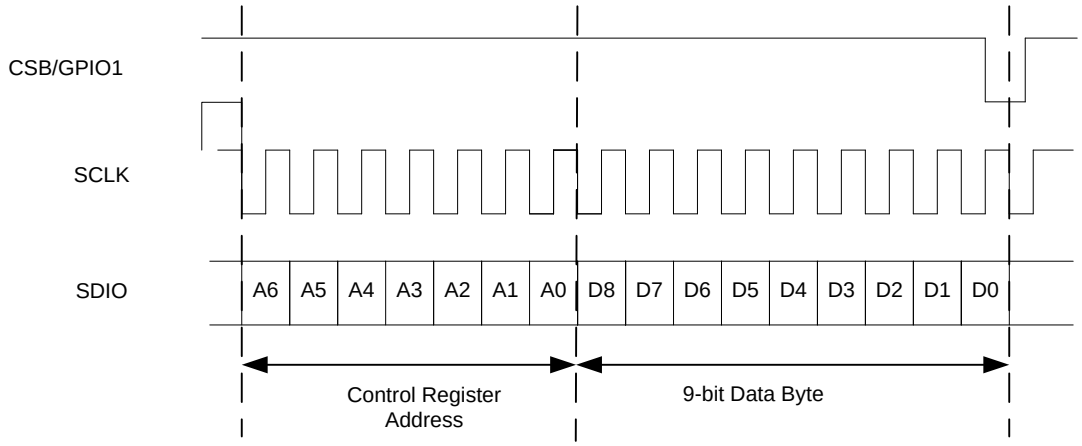


Figure 19: Register write operation using a 16-bit SPI Interface

8.8 SPI 4-Wire 24-bit Write and 32-bit Read Operation

The SPI 4-Wire Read/Write modes are enabled when the NAU8501 MODE pin is in a logic LOW condition, AND when the SPI Enable bit (SPIEN) is set in Register 7, Bit 8. Note that any time after either a hardware reset or software reset of the NAU8501 has occurred, the SPIEN bit must be set before the SPI 4-Wire Read/Write modes can be used. This must be done using either the SPI 3-Wire Write mode, or using the 2-Wire Write operation.

8.9 SPI 4-Wire Write Operation

The SPI 4-Wire write operation is a full SPI data transaction. However, only three wires are needed, as this is a write-only operation with no return data. A fourth wire is needed only when there are bi-directional data. The CSB/GPIO1 pin on the NAU8501 is used as the chip select function in the SPI transaction.

After CSB is held in a logic LOW condition, data bits from SDIO are clocked into the NAU8501 on every rising edge of SCLK. A write operation is indicated by the value 0x10 (hexadecimal) placed in the Device Address byte of the transaction. This byte is followed by a 7-bit Control Register Address and a 9-bit data value packed into the next two bytes of three-byte sequence. After the LSB of the Data Byte is clocked into the NAU8501, the 9-bit data value is automatically transferred into the NAU8501 register addressed by the Control Register Address value.

If only a single register is to be written, CSB/GPIO must be put into a logic HIGH condition after the LSB of the Data Byte is clocked into the device. If CSB/GPIO1 remains in a logic LOW condition, the NAU8501 will auto-index the Control Register Address value to the next higher address, and the next two bytes will be clocked into the next sequential NAU8501 register address. This will continue as long as CSB/GPIO1 is in the logic LOW condition. If the Control Register Address being indexed inside the NAU8501 reaches the value 0x7F (hexadecimal), and after the value for this register is written, the index will roll over to 0x00 and the process will continue.

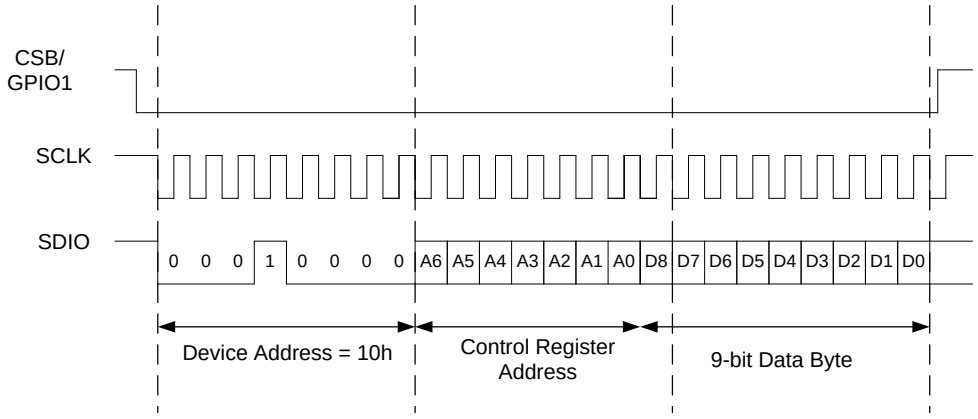


Figure 20: Register Write operation using a 24-bit SPI Interface

8.10 SPI 4-Wire Read Operation

The SPI 4-Wire Read operation is a full SPI data transaction with a two-byte address phase, and two-byte data phase. The CSB/GPIO1 pin on the NAU8501 is used as the chip select function in the SPI transaction.

After CSB is held in a logic LOW condition, data bits from SDIO are clocked into the NAU8501 on every rising edge of SCLK. A read operation is indicated by the value 0x20 (hexadecimal) placed in the Device Address byte of the transaction. This byte is followed by a 7-bit Control Register Address, padded by a non-used zero value in the LSB portion of the Control Register Address.

After the LSB of the Control Register Address is clocked, the NAU8501 will begin outputting its data on the GPIO3 pin, beginning with the very next SCLK rising edge. These data are transmitted in two bytes and contain the 9-bit value from the NAU8501 register selected by the Control Register Address. The data are transmitted MSB first, with the first 7-bits of the two byte value padded by zeros.

If only a single register is to be read, CSB/GPIO must be put into a logic HIGH condition after the LSB of the Data Byte 1 is clocked from the NAU8501. If CSB/GPIO1 remains in a logic LOW condition, the NAU8501 will auto-index the Control Register Address value to the next higher address, and the next two bytes will be clocked from the next sequential NAU8501 register address. This will continue as long as CSB/GPIO1 is in the logic LOW condition. If the Control Register Address being indexed inside the NAU8501 reaches the value 0x7F (hexadecimal), and after the value for this register is output, the index will roll over to 0x00 and the process will continue.

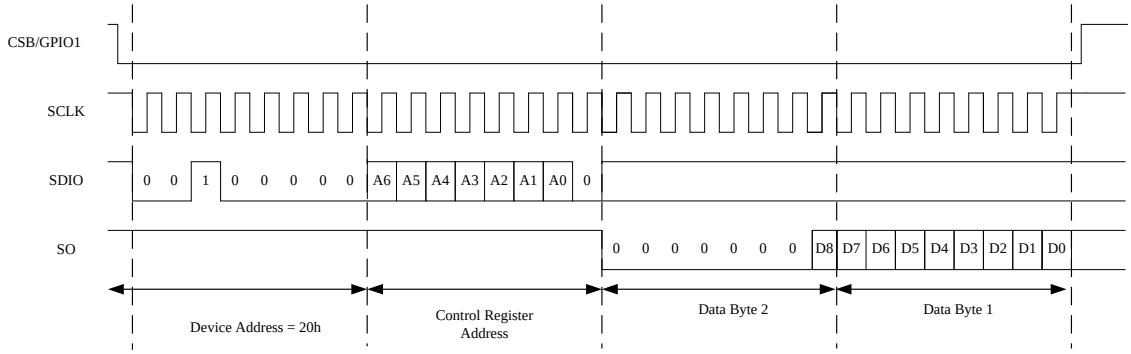


Figure 21: Register Read operation through a 32-bit SPI Interface

8.11 Software Reset

The entire NAU8501 and all of its control registers can be reset to default initial conditions by writing any value to Register 0, using any of the control interface modes. Writing to any other valid register address terminates the reset condition, but all registers will now be set to their power-on default values.

9 Product Family Digital Audio Interfaces

The NAU8501 is compatible with all parts in its product family, and can be configured as either the master or the slave, by setting register 6, bit 0, to 1 for master mode and to 0 for slave mode. Slave mode is the default if this bit is not written. In master mode, NAU8501 outputs both Frame Sync (FS) and the audio data bit clock (BCLK,) has full control of the data transfer. In the slave mode, an external controller supplies BCLK and FS. ADCOUT clocks out ADC the data on each high-to-low transistion of BLCK, and data are latched on each rising edge of BLCK.

When not transmitting data, ADCOUT pulls LOW in the default state. Depending on the application, the output can be configured to pull up or pull down. To configure the output to pull up, write a 1 to register 60, bit 3 (PUDPS). When the time slot function is enabled (see below), there are additional output state modes including controlled tri-state capability.

NAU8501 supports six audio formats as shown in table below, all with an MSB-first data format. The audio format default mode is I^2S.

PCM Mode	Register 4, bits 3 -4 AIFF	Register 4, bit 7 LRP	Register 60, bit 8 PCMTSEN
Right Justified	00	0	0
Left Justified	01	0	0
I^2S	10	0	0
PCM A	11	0	0
PCM B	11	1	0
PCM Time Slot	11	Don't care	1

Table 13: Digital Audio Interface Modes

9.1 Right-Justified Audio Data

In right-justified mode, the LSB is clocked on the last BCLK rising edge before FS transitions. When FS is HIGH, left channel data is transmitted and when FS is LOW, right channel data is transmitted. This is shown in the figure below.

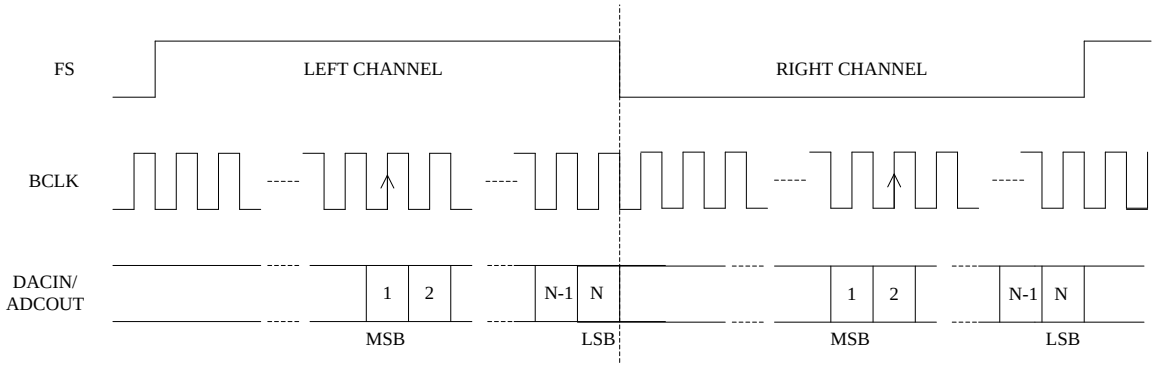


Figure 22: Right-Justified Audio Interface

9.2 Left-Justified Audio Data

In left-justified mode, the MSB is clocked on the first BCLK rising edge after FS transitions. When FS is HIGH, left channel data is transmitted and when FS is LOW, right channel data is transmitted. This is shown in the figure below.

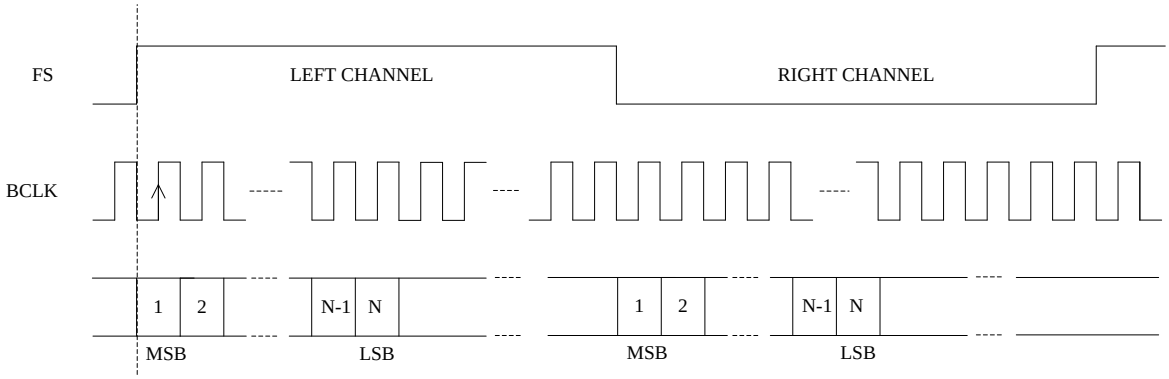


Figure 23: Left-Justified Audio Interface

9.3 I²S Audio Data

In I²S mode, the MSB is clocked on the second BCLK rising edge after FS transitions. When FS is LOW, left channel data is transmitted and when FS is HIGH, right channel data is transmitted. This is shown in the figure below.

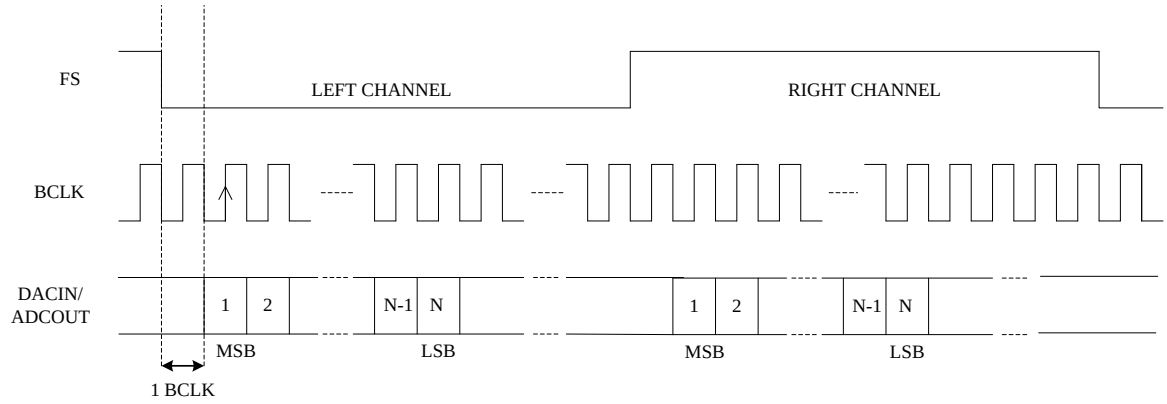


Figure 24: I2S Audio Interface

9.4 PCM A Audio Data

In the PCM A mode, left channel data is transmitted first followed immediately by right channel data. The left channel MSB is clocked on the second BCLK rising edge after the FS pulse rising edge, and the right channel MSB is clocked on the next SCLK after the left channel LSB. This is shown in the figure below.

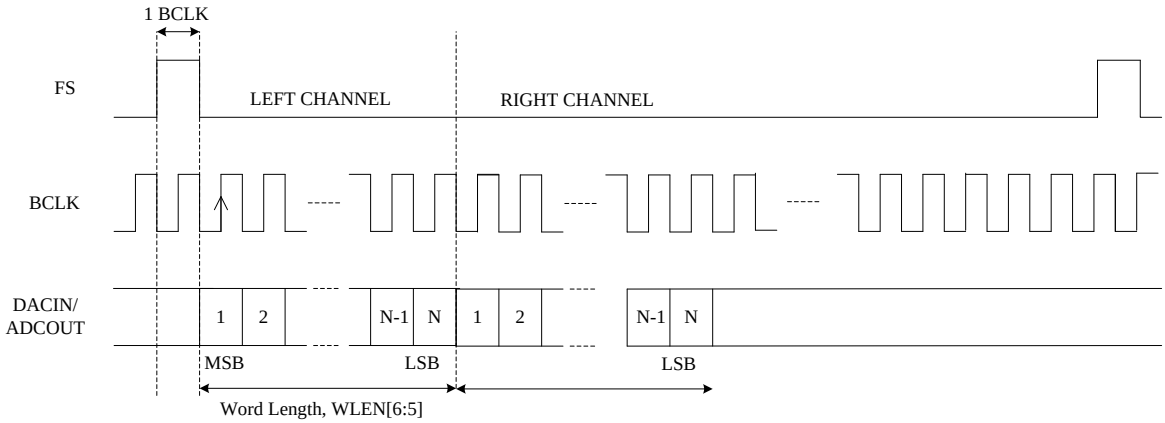


Figure 25: PCM A Audio Interface

9.5 PCM B Audio Data

In the PCM B mode, left channel data is transmitted first followed immediately by right channel data. The left channel MSB is clocked on the first BCLK rising edge after the FS pulse rising edge, and the right channel MSB is clocked on the next SCLK after the left channel LSB. This is shown in the figure below.

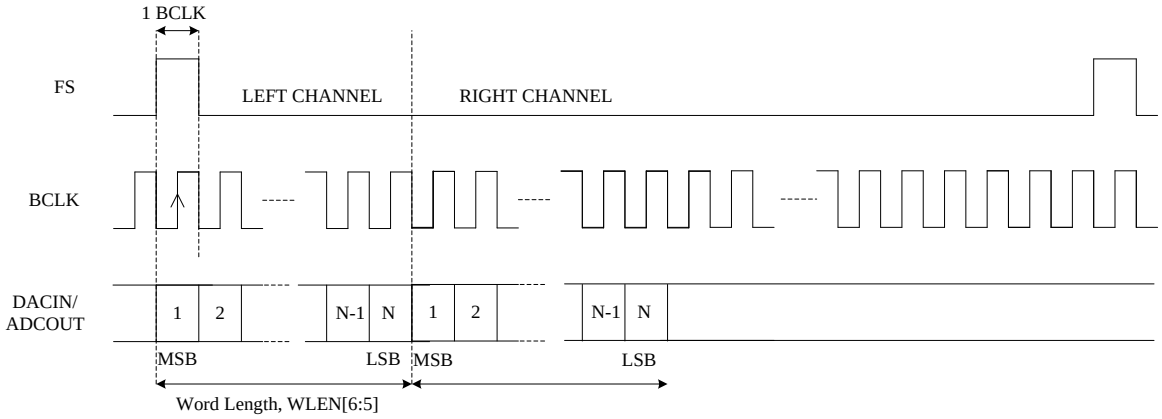


Figure 26: PCM-B Audio Interface

9.6 PCM Time Slot Audio Data

The PCM time slot mode is used to delay the time at which the DAC and/or ADC data are clocked. This increases the flexibility of the NAU8501 to be used in a wide range of system designs. One key application of this feature is to enable multiple NAU8501 or other devices to share the audio data bus, thus enabling more than two channels of audio. This feature may also be used to swap left and right channel data, or to cause both the left and right channels to use the same data.

Normally, the DAC and ADC data are clocked immediately after the Frame Sync (FS). In the PCM time slot mode, the audio data are delayed by a delay count specified in the device control registers. The left channel MSB is clocked on the BCLK rising edge defined by the delay count set in Registers 59 and 60. The right channel MSB is clocked on the BCLK rising edge defined by the delay count set in Registers 60 and 61.

Register 60 also controls ADCOUT output impedance options enabling the ADCOUT pin to share the same signal wire with other drivers. The default is the non-shared mode, with the output enable bit (PUDEN) set to logic=1. This results in the ADCOUT pin being actively driven at all times (never in a high-impedance state).

However, if PUDEN is logic=0, and PUDPE (pull-up/down enable) is logic=1, then ADCOUT will be pulled HIGH or LOW by means of an internal passive resistor. This enables wired-OR type bus sharing. The choice of passive pull-up, or passive pull-down is determined by the PUDPS (pull-up/down select) bit.

If PUDEN and PUDPE are both logic=0, ADCOUT is high impedance, except when actively transmitting left and right channel audio data. After outputting audio channel data, ADCOUT will return to high impedance on the BCLK negative edge during the LSB data period if Register 60, bit 7 (TRI), is HIGH, or on the BCLK positive edge of LSB if Register 60, bit 7 (TRI), is LOW. Tri-stating on the negative edge allows the transmission of data by multiple sources in adjacent timeslots with reduced risk of bus driver contention.

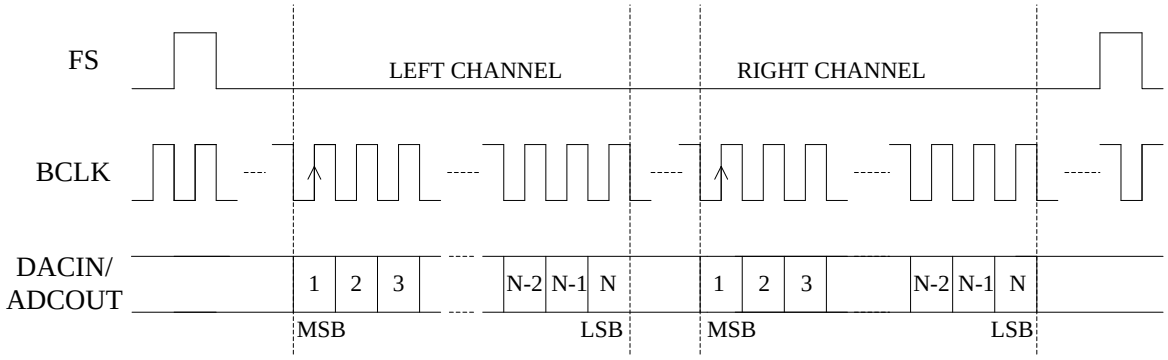


Figure 27: PCM Time Slot Audio Interface

9.7 Control Interface Timing

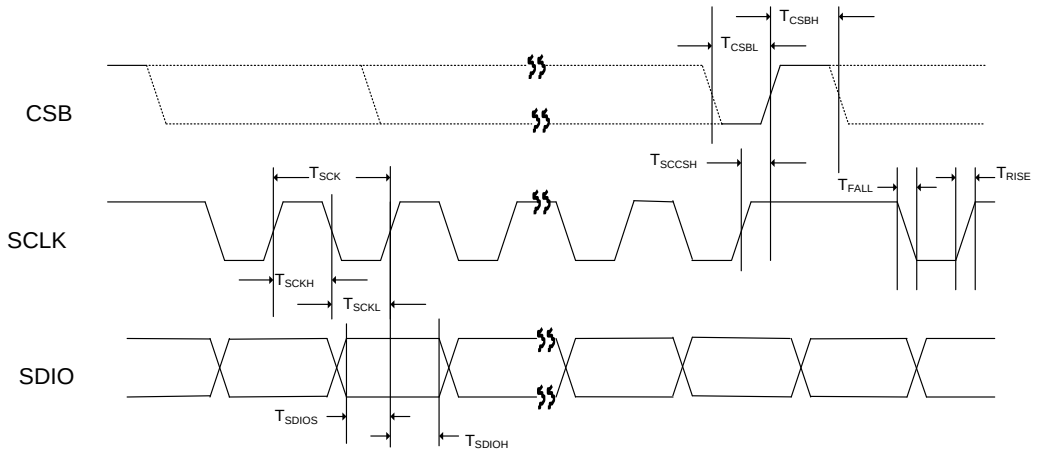


Figure 28: 3-wire Control Mode Timing

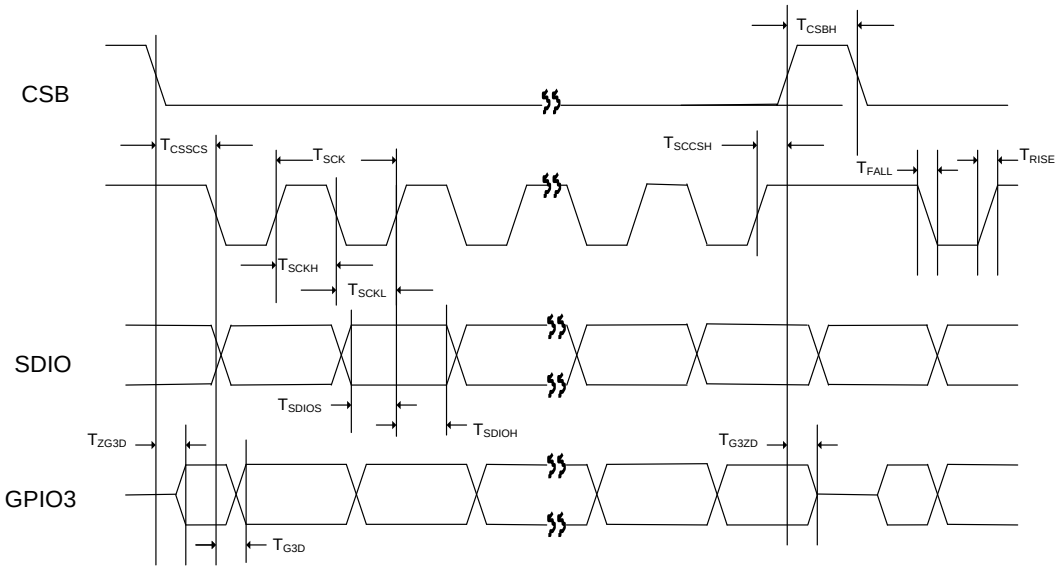


Figure 29: 4-wire Control Mode Timing

Symbol	Description	min	typ	max	unit
T_{SCK}	SCLK Cycle Time	80	-	-	ns
T_{SCKH}	SCLK High Pulse Width	35	-	-	ns
T_{SCKL}	SCLK Low Pulse Width	35	-	-	ns
T_{RISE}	Rise Time for all Control Interface Signals	-	-	10	ns
T_{FALL}	Fall Time for all Control Interface Signals	-	-	10	ns
T_{CSSCS}	CSB Falling Edge to 1st SCLK Falling Edge Setup Time (4 wire Mode Only)	30	-	-	ns
T_{SCCSH}	Last SCLK Rising Edge to CSB Rising Edge Hold Time	30	-	-	ns
T_{CSBL}	CSB Low Time	30	-	-	ns
T_{CSBH}	CSB High Time between CSB Lows	30	-	-	ns
T_{SDIOS}	SDIO to SCLK Rising Edge Setup Time	20	-	-	ns
T_{SDIOH}	SCLK Rising Edge to SDIO Hold Time	20	-	-	ns
T_{ZG3D}	Delay Time from CSB Falling Edge to GPIO3 Active (4 wire Mode Only)	--	--	15	ns
T_{G3ZD}	Delay Time from CSB Rising Edge to GPIO3 Tri-state (4-wire Mode Only)	--	--	15	ns
T_{G3D}	Delay Time from SCLK Falling Edge to GPIO3 (4-wire Mode Only)	-	-	15	ns

Table 14: Three- and Four Wire Control Timing Parameters

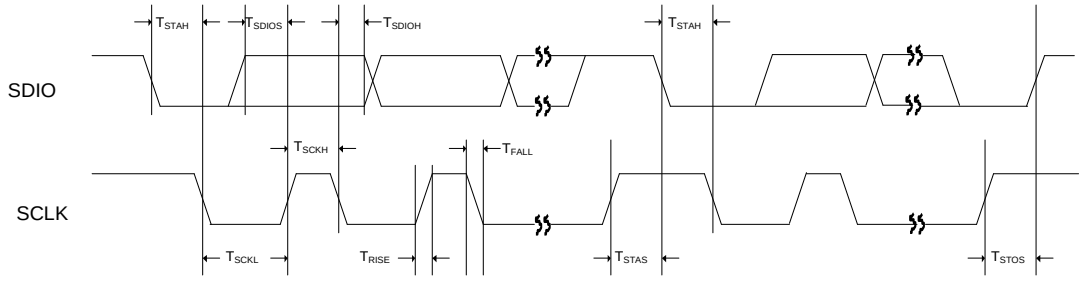


Figure 30: Two-wire Control Mode Timing

Symbol	Description	min	typ	max	unit
T_{STAH}	SCLK falling edge to SDIO falling edge hold timing in START / Repeat START condition	600	-	-	ns
T_{STAS}	SDIO rising edge to SCLK falling edge setup timing in Repeat START condition	600	-	-	ns
T_{STOS}	SDIO rising edge to SCLK rising edge setup timing in STOP condition	600	-	-	ns
T_{SCKH}	SCLK High Pulse Width	600	-	-	ns
T_{SCKL}	SCLK Low Pulse Width	1,300	-	-	ns
T_{RISE}	Rise Time for all 2-wire Mode Signals	-	-	300	ns
T_{FALL}	Fall Time for all 2-wire Mode Signals	-	-	300	ns
T_{SDIOS}	SDIO to SCLK Rising Edge DATA Setup Time	400	-	-	ns
T_{SDIOH}	SCLK falling Edge to SDIO DATA Hold Time	0	-	600	ns

Table 15: Two-wire Control Timing Parameters

9.8 Audio Interface Timing:

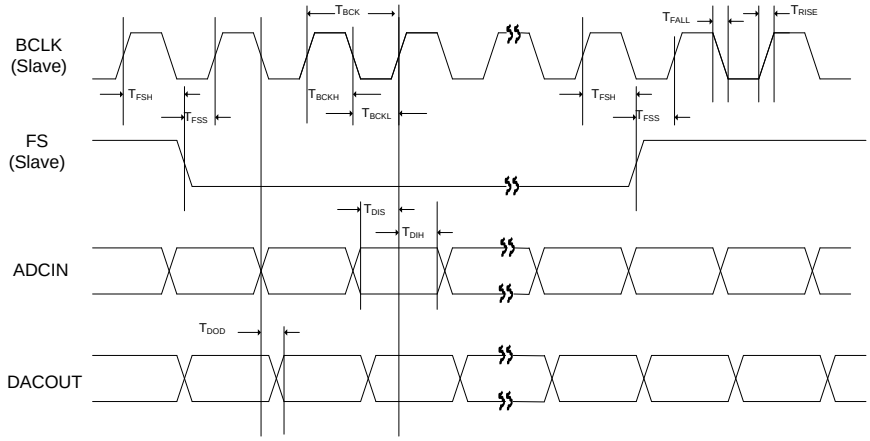


Figure 31: Digital Audio Interface Slave Mode Timing

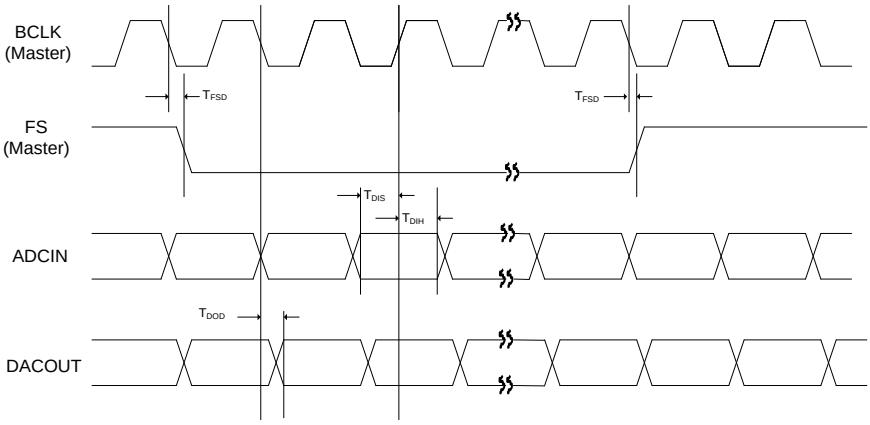


Figure 32: Digital Audio Interface Master Mode Timing

Symbol	Description	min	typ	max	unit
T_{BCK}	BCLK Cycle Time in Slave Mode	50	-	-	ns
T_{BCKH}	BCLK High Pulse Width in Slave Mode	20	-	-	ns
T_{BCKL}	BCLK Low Pulse Width in Slave Mode	20	-	-	ns
T_{FSS}	FS to BCLK Rising Edge Setup Time in Slave Mode	20	-	-	ns
T_{FSH}	BCLK Rising Edge to FS Hold Time in Slave Mode	20	-	-	ns
T_{FSD}	BCLK Falling Edge to FS Delay Time in Master Mode	-	-	10	ns
T_{RISE}	Rise Time for All Audio Interface Signals	-	-	$0.135T_{BCK}$	ns
T_{FALL}	Fall Time for All Audio Interface Signals	-	-	$0.135T_{BCK}$	ns
T_{DIS}	ADCIN to BCLK Rising Edge Setup Time	15	-	-	ns
T_{DIH}	BCLK Rising Edge to ADCIN Hold Time	15	-	-	ns

Table 16: Audio Interface Timing Parameters

10 Application Information

10.1 Typical Application Schematic

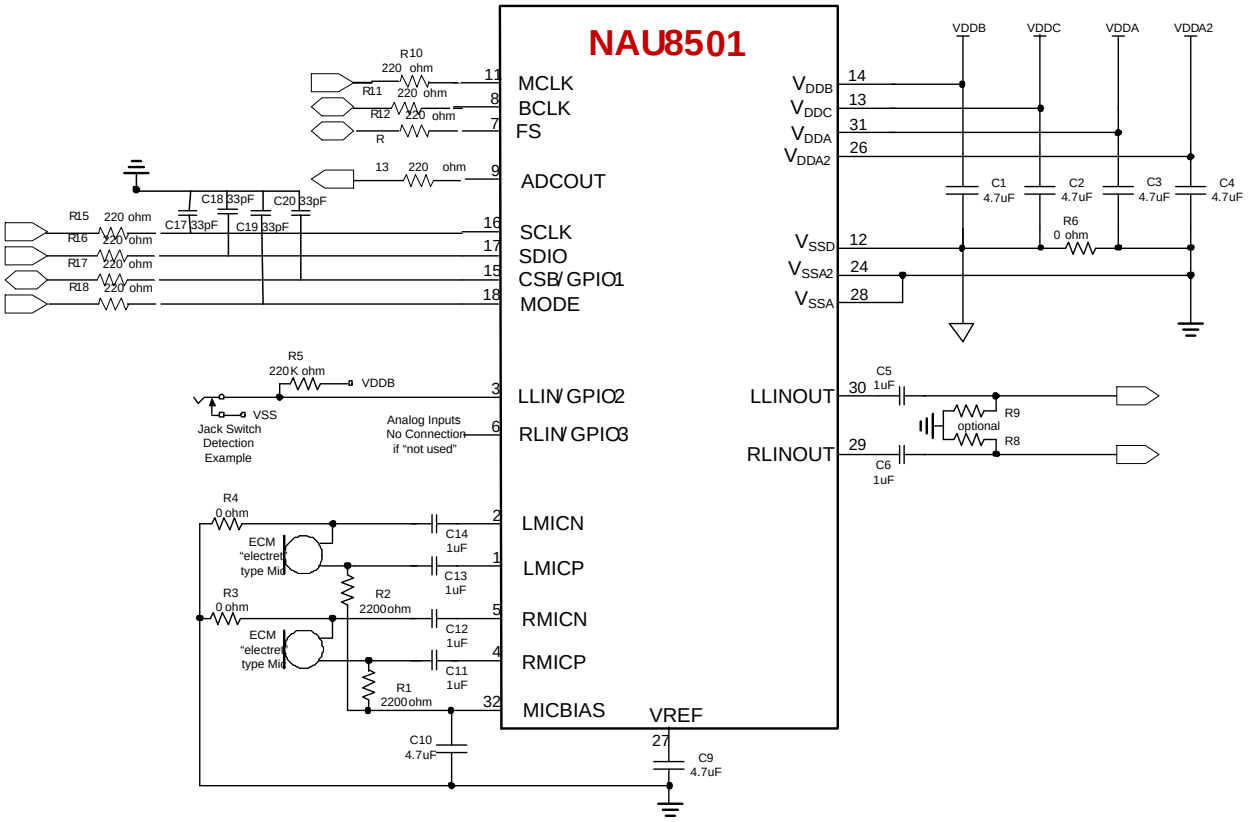


Figure 33: Schematic with recommended external components for typical application with AC-coupled headphones and stereo electret (ECM) style microphones.

Note 1: All non-polar capacitors are assumed to be low ESR type parts, such as with MLC construction or similar. If capacitors are not low ESR, additional 0.1ufd and/or 0.01ufd capacitors may be necessary in parallel with the bulk 4.7ufd capacitors on the supply rails.

Note 2: Load resistors to ground on outputs may be helpful in some applications to insure a DC path for the output capacitors to charge/discharge to the desired levels. If the output load is always present and the output load provides a suitable DC path to ground, then the additional load resistors may not be necessary. If needed, such load resistors are typically a high value, but a value dependent upon the application requirements.

Note 3: To minimize pops and clicks, large polarized output capacitors should be a low leakage type.

Note 4: Depending on the microphone device and PGA gain settings, common mode rejection can be improved by choosing the resistors on each node of the microphone such that the impedance presented to any noise on either microphone wire is equal.

Note 5: Unused analog input pins should be left as no-connection.

Note 6: Unused digital input pins should be tied to ground.

Note 7: R15-R18 and C17-C20 for low pass filter to filter glitch; the low pass filter corner frequency range is from 8MHz to 33MHz depending on PCB parasitics.

10.2 Recommended power up and power down sequences

To minimize pop and click noise, the NAU8501 should be powered up and down using the procedures in this section as guidance. The power-up procedure should be followed upon system power-up, or after any time that the NAU8501 has been issued a register reset command.

The strongest cause of pops and clicks in most systems is the sudden charging or discharging of capacitors used for AC-coupling to inputs and outputs. Any sudden change in voltage will cause a pop or click, with or without AC-coupling capacitors in the signal path. The general strategy for pop and click reduction is to allow such charging and discharging to happen slowly.

10.2.1 Power Up (and after a software generated register reset) Procedure Guidance

Turn on external power supplies and wait for supply voltages to settle. This amount of time will be dependent on the system design. Software may choose to test the NAU8501 to determine when it is no longer in an active reset condition. This procedure is described in more detail in the sections relating to power supplies.

As a general policy, it is a good idea to put any input or output driver paths into the "mute" condition any time internal register and data path configurations are being changed. Be sure at this time that all used inputs and outputs are in their muted/disconnected condition.

Next, the internal DC tie-off voltage buffers should be enabled:

R1 Bit 2, IOBUFEN, set to logic = 1
Value to be written to R1 = 0x104

At this point, the NAU8501 has been prepared to start charging any input/output capacitors to their normal operating mode charge state. If this is done slowly, then there will be no pops and clicks. One way to accomplish this is to allow the internal/external reference voltage to charge slowly by means of its internal coupling resistors. This is accomplished by:

R1 Bits 1, Bit 0, REFIMP set to 80kΩ setting
R1 Bit 2, ABIASEN, set to logic = 1
Value to be written to R1 = 0x10D

After this, the system should wait approximately 250ms, or longer, depending on the external components that have been selected for a given specific application.

Next, the outputs may be enabled, but with the audio input to the drivers still in the mute condition. Unless power management requires outputs to be turned off when not used, it is best for pops and clicks to leave outputs enabled at all times, and to use the output mute controls to silence the outputs as needed.

Finally, the NAU8501 can be programmed as needed for a specific application. The final step in most applications will be to unmute any outputs, and then begin normal operation.

10.2.2 Power Down

Powering down is more application specific. The most important step is to mute all outputs before any other steps. It then may be further helpful to disable all outputs just before the system power-down sequence is started.

10.2.3 Unused Input/Output Tie-Off Information

In audio and voice systems, any time there is a sudden change in voltage to an audio signal, an audible pop or click sound may be the result. Systems that change inputs and output configurations dynamically, or which are required to manage low power operation, need special attention to possible pop and click situations.

The NAU8501 includes many features which may be used to greatly reduce or eliminate pop and click sounds. The most common cause of a pop or click signal is a sudden change to an input or output voltage. This may happen in either a DC coupled system, or in an AC coupled system.

The strategy to control pops and clicks is similar for either a DC coupled system, or an AC coupled system. The case of the AC coupled system is the most common and the more difficult situation, and therefore, the AC coupled case will the focus for this information section.

When an input or output pin is being used, the DC level of that pin will be very close to ½ of the VDDA voltage that is present on the VREF pin.

In all cases, any input or output capacitors will become charged to the operating voltage of the used input or output pin. The goal to reduce pops and clicks is to insure that the charge voltage on these capacitors does not change suddenly at any time.

When an input or output is in a not-used operating condition, it is desirable to keep the DC voltage on that pin at the same voltage level as the DC level of the used operating condition. This is accomplished using special internal DC voltage sources that are at the required DC values. When an input or output is in the not-used condition, it is connected to the correct internal DC voltage as not to have a pop or click. This type of connection is known as a "tie-off" condition.

An internal DC voltage source is provided for making tie-off connections. This source has a DC level is equal to the VREF voltage value. All inputs and outputs are tied off to the VREF voltage value when in a "not used" configuration. To conserve power, this internal voltage buffer may be enabled/disabled using the R1 power management control register.

To better manage pops and clicks, there is a choice of impedance of the tie-off connection for unused outputs. The nominal values for this choice are 1kΩ and 30kΩ. The low impedance value will better maintain the desired DC level in the case when there is some leakage on the output capacitor or some DC resistance to ground at the NAU8501 output pin. A tradeoff in using the low-impedance value is primarily that output capacitors could change more suddenly during power-on and power-off changes.

Automatic internal logic determines whether an input or output pin is in the used or un-used condition. This logic function is always active. An output is determined to be in the un-used condition when it is in the disabled unpowered condition, as determined by the power management registers. An input is determined to be in the un-used condition when all internal switches connected to that input are in the "open" condition.

10.2.4 Unused Input/Output Tie-Off Diagram

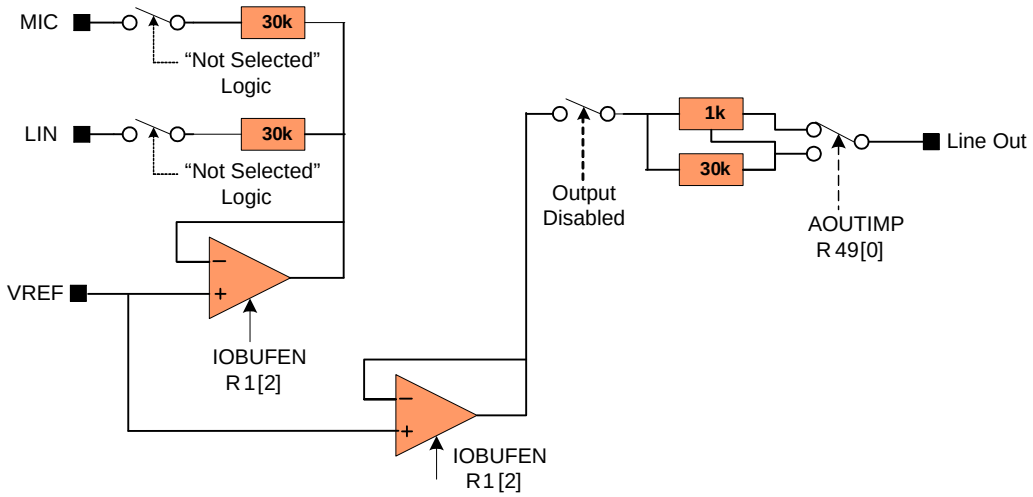


Figure 34: Tie-off Options for input and output pin examples

Register controls that directly affect the tie-off features are:

Register 1	Enable buffer for VREF tie-off
Register 49	Tie-off impedance selection

Note: Resistor tie-off resistor switches will open/close regardless of whether or not the associated internal DC buffer is in the enabled or disabled condition.

10.3 Power Consumption

The NAU8501 has flexible power management capability which allows sections not being used to be powered down, to draw minimum current in battery-powered applications. The following table shows typical power consumption in different operating conditions. The "off" condition is the initial power-on state with all subsystems powered down, and with no applied clocks.

Mode	Conditions	VDDA = 3V	VDDC = 1.8V	VDDB = 3V	Total Power
		mA	mA	mA	mW
OFF		0.008	0.001	0.0003	0.025
Sleep	VREF maintained @ 300kΩ, no clocks,	0.008	0.001	0.0003	0.025
	VREF maintained @ 75kΩ, no clocks,	0.014	0.001	0.0003	0.045
	VREF maintained @ 5kΩ, no clocks,	0.259	0.001	0.0003	0.781
Stereo Record	8kHz, 0.9Vrms input signal	6.44	1.07	0.10	21.5
	8kHz, 0.9Vrms input signal, PLL on	7.42	1.33	0.10	24.9

Table 17: Typical Power Consumption in Various Application Modes.

10.4 Supply Currents of Specific Blocks

The NAU8501 can be programmed to enable/disable various analog blocks individually, and the current to some of the major blocks can be reduced with minimum impact on performance. The table below shows the change in current consumed with different register settings. Sample rate settings affect current consumption of VDDC supply. Lower sampling rates draw lower current.

Register		Function	Bit	VDDA current increase/ Decrease when enabled
Dec	Hex			
1	01	Power Management 1	REFIMP[1:0]	+100µA for 80kΩ and 300kΩ +260µA for 3kΩ
			IOBUFEN[2]	+100µA
			ABIASEN[3]	+600µA
			MICBIASEN[4]	+540µA
			PLLEN[5]	+2.5 mA +1/5mA from VDDC with clocks applied
2	02	Power Management 2	LADCEN[0]	+2.3 mA with 64X OSR +3.3 mA with 128X OSR
			RADCEN[1]	+2.3 mA with 64X OSR +3.3 mA with 128X OSR
			LPGAEN[2]	+300µA
			RPGAEN[3]	+300µA
			LBSTEN[4]	+650µA
			RBSTEN[5]	+650µA
			SLEEP[6]	Same as PLLEN (R1[5])
			RLINEN[7]	+800µA
			LLINEN[8]	+800µA
			LBYPEN[2]	+250µA
			RBYPEN[3]	+250µA
58	3A	Power Management 4	IBIADJ[1:0]	-1.2mA with IBIADJ at 11
			REGVOLT[2:3]	
			MICBIASM[4]	
			LPADC[6]	-1.1mA with no SNR decrease @ 8kHz
			LPIPBST[7]	-600µA with no SNR decrease @ 8kHz
			LPDAC[8]	-1.1mA with 1.4dB SNR decrease @ 44.1kHz

Table 18: VDDA 3.3V Supply Current in Various Modes

11 Appendix A: Digital Filter Characteristics

Parameter	Conditions	Min	Typ	Max	Units
ADC Filter					
Passband	+/- 0.015dB	0		0.454	fs
	-6dB		0.5		fs
Passband Ripple				+/-0.015	dB
Stopband		0.546			fs
Stopband Attenuation	f > 0.546*fs	-60			dB
Group Delay			28.25		1/fs
ADC High Pass Filter					
High Pass Filter Corner Frequency	-3dB		3.7		Hz
	-0.5dB		10.4		Hz
	-0.1dB		21.6		Hz

Table 19: Digital Filter Characteristics

TERMINOLOGY

1. Stop Band Attenuation (dB) – the degree to which the frequency spectrum is attenuated (outside audio band)
2. Pass-band Ripple – any variation of the frequency response in the pass-band region
3. Note that this delay applies only to the filters and does not include other latencies, such as from the serial data interface

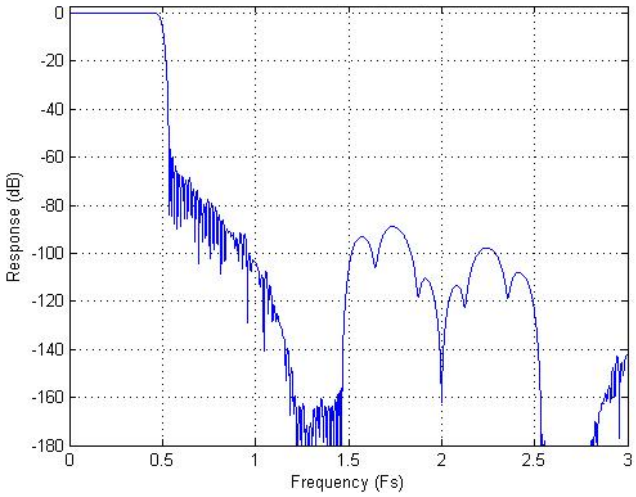


Figure 35: ADC Filter Frequency Response

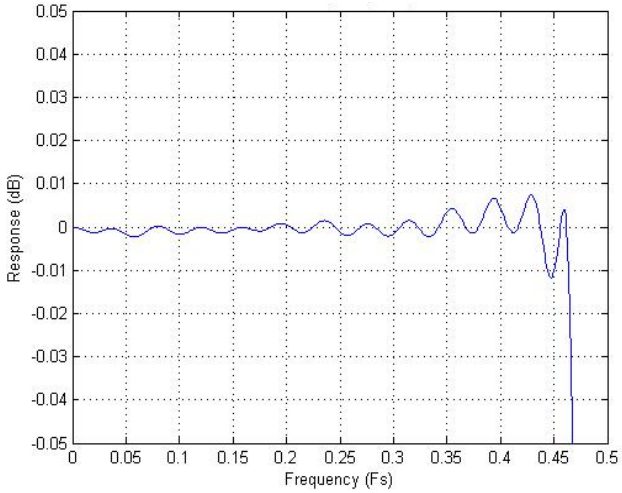


Figure 36: ADC Filter Ripple

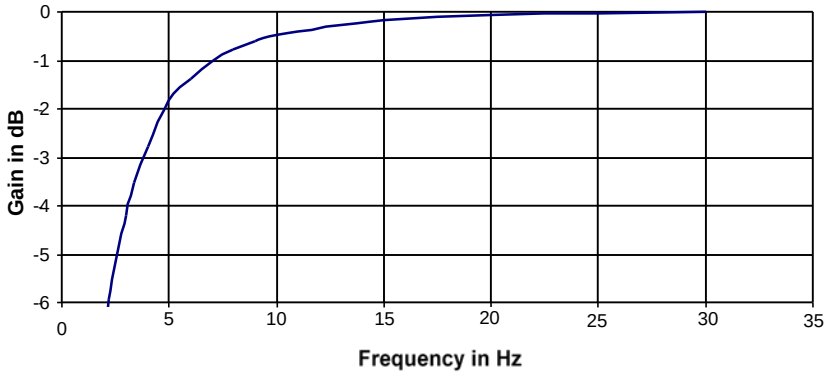


Figure 37: ADC Highpass Filter Response, Audio Mode

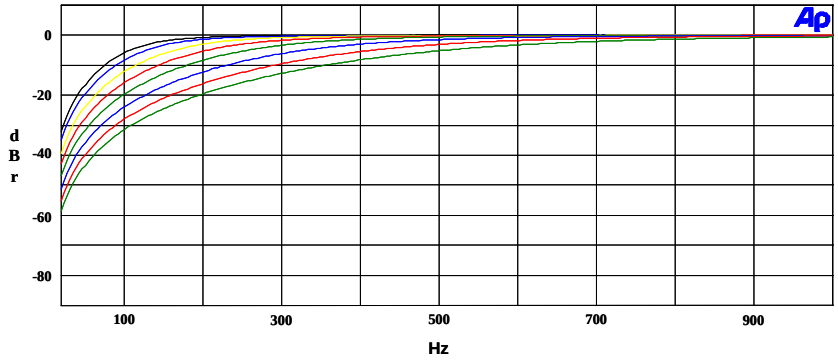


Figure 38: ADC Highpass Filter Response, HPF enabled, FS = 48kHz

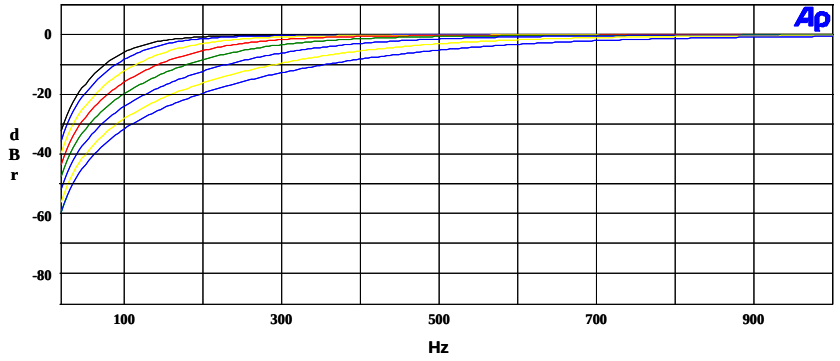


Figure 39: ADC Highpass Filter Response, HPF enabled, FS = 24kHz

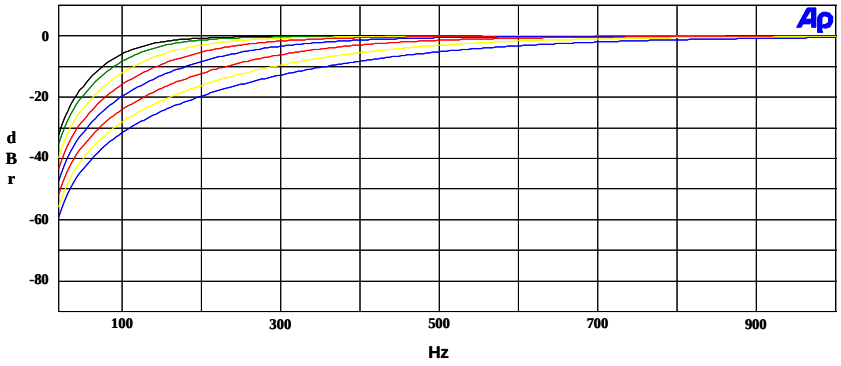


Figure 40: ADC Highpass Filter Response, HPF enabled, FS = 12kHz

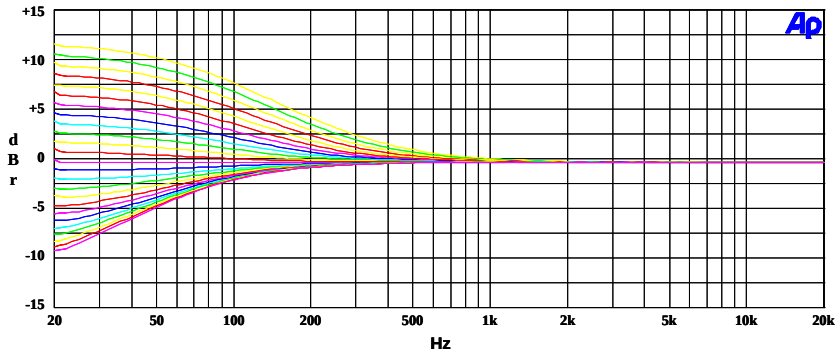


Figure 41: EQ Band 1 Gains for Lowest Cut-Off Frequency

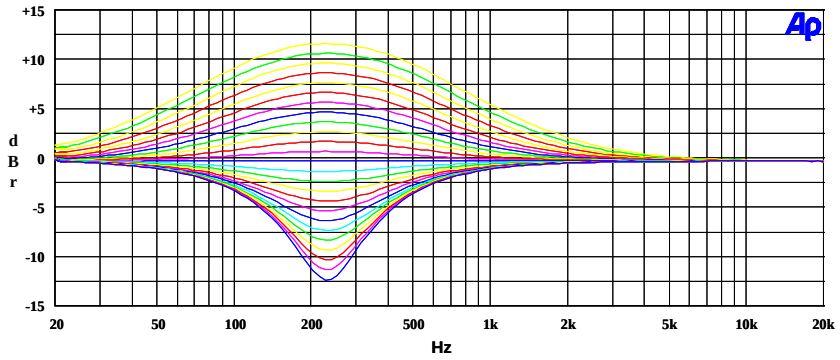


Figure 42: EQ Band 2 Peak Filter Gains for Lowest Cut-Off Frequency with EQ2BW = 0

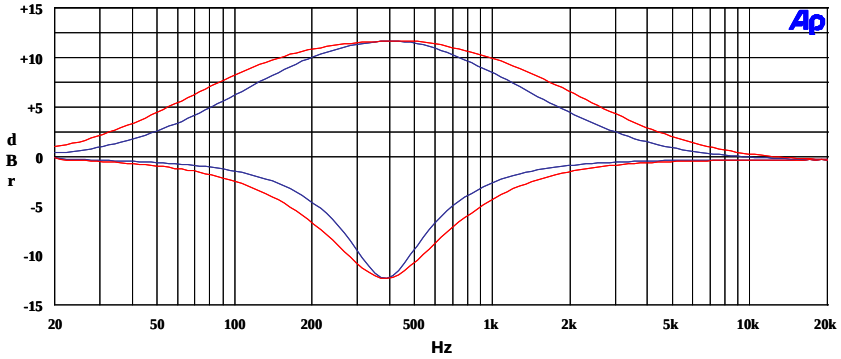


Figure 43: EQ Band 2, EQ2BW = 0 versus EQ2BW = 1

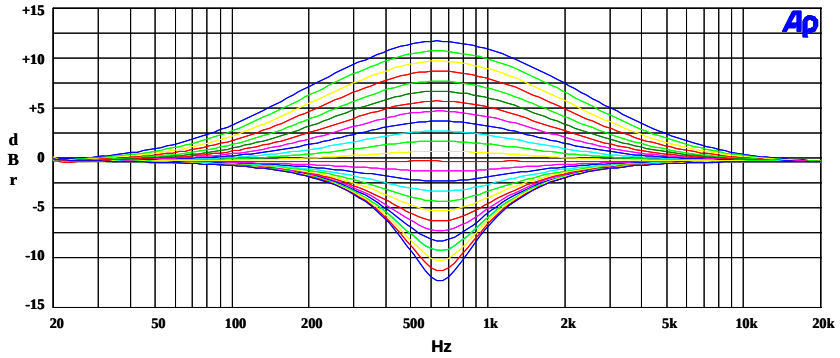


Figure 44: EQ Band 3 Peak Filter Gains for Lowest Cut-Off Frequency with EQ3BW = 0

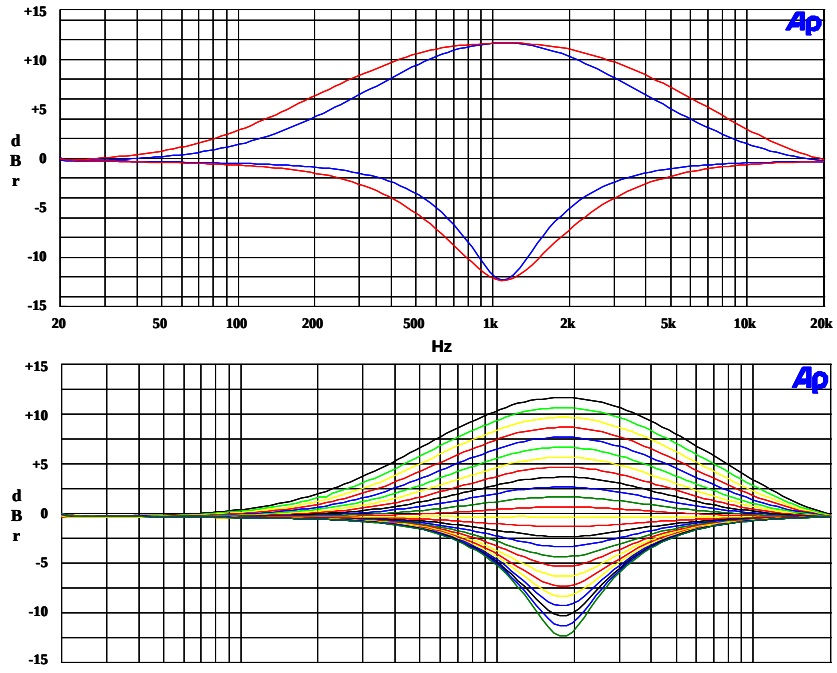


Figure 45: EQ Band 3, EQ3BW = 0 versus EQ3BW = 1

Figure 46: EQ Band 4 Peak Filter Gains for Lowest Cut-Off Frequencies with EQ4BW = 0

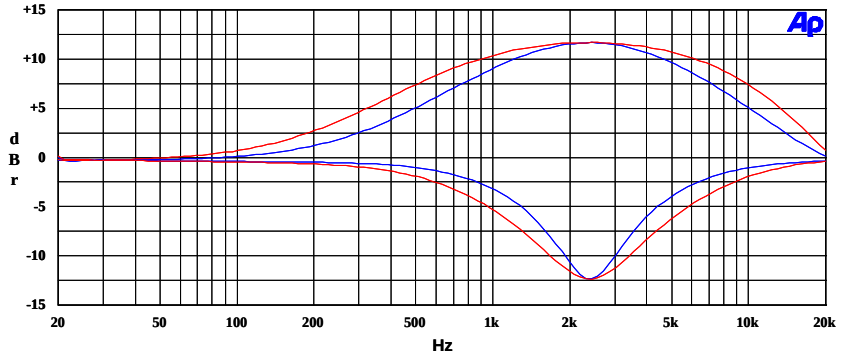


Figure 47: EQ Band 4, EQ4BW = 0 versus EQ4BW =1

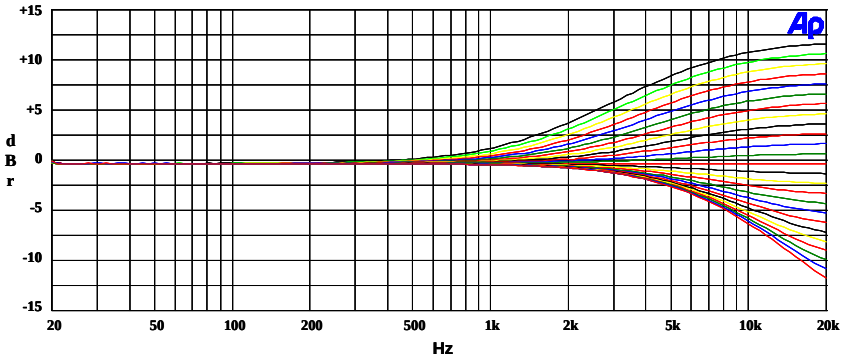


Figure 48: EQ Band 5 Gains for Lowest Cut-Off Frequency

12 Appendix B: Companding Tables

12.1 µ-Law / A-Law Codes for Zero and Full Scale

Level	µ-Law			A-Law		
	Sign bit (D7)	Chord bits (D6,D5,D4)	Step bits (D3,D2,D1,D0)	Sign bit (D7)	Chord bits (D6,D5,D4)	Step bits (D3,D2,D1,D0)
+ Full Scale	1	000	0000	1	010	1010
+ Zero	1	111	1111	1	101	0101
- Zero	0	111	1111	0	101	0101
- Full Scale	0	000	0000	0	010	1010

Table 20: Companding Codes for Zero and Full-Scale

12.2 µ-Law / A-Law Output Codes (Digital mW)

Sample	µ-Law			A-Law		
	Sign bit (D7)	Chord bits (D6,D5,D4)	Step bits (D3,D2,D1,D0)	Sign bit (D7)	Chord bits (D6,D5,D4)	Step bits (D3,D2,D1,D0)
1	0	001	1110	0	011	0100
2	0	000	1011	0	010	0001
3	0	000	1011	0	010	0001
4	0	001	1110	0	011	0100
5	1	001	1110	1	011	0100
6	1	000	1011	1	010	0001
7	1	000	1011	1	010	0001
8	1	001	1110	1	011	0100

Table 21: Companding Output Codes

13 Appendix C: Details of Register Operation

Register		Function	Name	Bit								Description
Dec	Hex			8	7	6	5	4	3	2	1	0	
0	00	Software Reset											Any write operation to this register resets all registers to default values
1	01	Power Management 1											Reserved
			PLLEN										Power control for internal PLL 0 = unpowered 1 = enabled
			MICBIASEN										Power control for microphone bias buffer amplifier (MICBIAS output, pin#32) 0 = unpowered and MICBIAS pin in high-Z condition 1 = enabled
			ABIASEN										Power control for internal analog bias buffers 0 = unpowered 1 = enabled
			IOBUFEN										Power control for internal tie-off buffer used in non-boost mode (-1.0x gain) conditions 0 = internal buffer unpowered 1 = enabled
			REFIMP										Select impedance of reference string used to establish VREF for internal bias buffers 00 = off (input to internal bias buffer in high-Z floating condition) 01 = 80kΩ nominal impedance at VREF pin 10 = 300kΩ nominal impedance at VREF pin 11 = 3kΩ nominal impedance at VREF pin
			Default >>	0	0	0	0	0	0	0	0	0	0x000 reset value
2	02	Power Management 2	RLINEN										Right Line Output driver Enable 0 = output pin in high-Z condition 1 = enabled
			LLINEN										Left Line Output driver Enabled 0 = output pin in high-Z condition 1 = enabled
			SLEEP										Sleep enable 0 = device in normal operating mode 1 = device in low-power sleep condition
			RBSTEN										Right channel input mixer, RADC Mix/Boost stage power control 0 = RADC Mix/Boost stage OFF 1 = RADC Mix/Boost stage ON
			LBSTEN										Left channel input mixer, LADC Mix/Boost stage power control 0 = LADC Mix/Boost stage OFF 1 = LADC Mix/Boost stage ON
			RPGAEN										Right channel input programmable amplifier (PGA) power control 0 = Right PGA input stage OFF 1 = enabled
			LPGAEN										Left channel input programmable amplifier power control 0 = Left PGA input stage OFF 1 = enabled
			RADCEN										Right channel analog-to-digital converter power control 0 = Right ADC stage OFF 1 = enabled
			LADCEN										Left channel analog-to-digital converter power control 0 = Left ADC stage OFF 1 = enabled
			Default >>	0	0	0	0	0	0	0	0	0	0x000 reset value
3	03	Power Management 3											Reserved
			RBYPEN										Right bypass buffer to Line Output 0 = bypass buffer disabled 1 = enabled
			LBYPEN										Left bypass buffer to Line Output 0 = bypass buffer disabled 1 = enabled
													Reserved
			Default >>	0	0	0	0	0	0	0	0	0	0x000 reset value

Register		Function	Name	Bit								Description
Dec	Hex			8	7	6	5	4	3	2	1	0	
4	04	Audio Interface	BCLKP										Bit clock phase inversion option for BCLK, pin#8 0 = normal phase 1 = input logic sense inverted
			LRP										Phase control for I2S audio data bus interface 0 = normal phase operation 1 = inverted phase operation PCMA and PCMB left/right word order control 0 = MSB is valid on 2nd rising edge of BCLK after rising edge of FS 1 = MSB is valid on 1st rising edge of BCLK after rising edge of FS
			WLEN										Word length (24-bits default) of audio data stream 00 = 16-bit word length 01 = 20-bit word length 10 = 24-bit word length 11 = 32-bit word length
			AIFMT										Audio interface data format (default setting is I2S) 00 = right justified 01 = left justified 10 = standard I2S format 11 = PCMA or PCMB audio data format option
													Reserved
			ADCPHS										ADC audio data left-right ordering 0 = left ADC data is output in left phase of LRP 1 = left ADC data is output in right phase of LRP (left-right reversed)
			MONO										Mono operation enable 0 = normal stereo mode of operation 1 = mono mode with audio data in left phase of LRP
			Default >>	0	0	1	0	1	0	0	0	0	0x050 reset value
5	05	Companding											Reserved
			CMB8										8-bit word enable for companding mode of operation 0 = normal operation (no companding) 1 = 8-bit operation for companding mode
													Reserved
			ADCCM										ADC companding mode control 00 = off (normal linear operation) 01 = reserved 10 = u-law companding 11 = A-law companding
													Reserved
			Default >>	0	0	0	0	0	0	0	0	0	0x000 reset value
6	06	Clock control 1	CLKM										master clock source selection control 0 = MCLK, pin#11 used as master clock 1 = internal PLL oscillator output used as master clock
			MCLKSEL										Scaling of master clock source for internal 256fs rate (divide by 2 = default) 000 = divide by 1 001 = divide by 1.5 010 = divide by 2 011 = divide by 3 100 = divide by 4 101 = divide by 6 110 = divide by 8 111 = divide by 12
			BCLKSEL										Scaling of output frequency at BCLK pin#8 when chip is in master mode 000 = divide by 1 001 = divide by 2 010 = divide by 4 011 = divide by 8 100 = divide by 16 101 = divide by 32 110 = reserved 111 = reserved
													Reserved

Register		Function	Name	Bit								Description
Dec	Hex			8	7	6	5	4	3	2	1	0	
			CLKIOEN										Enables chip master mode to drive FS and BCLK outputs 0 = FS and BCLK are inputs 1 = FS and BCLK are driven as outputs by internally generated clocks
			Default >>	1	0	1	0	0	0	0	0	0	0x140 reset value
			4WSPIEN										4-wire control interface enable
													Reserved
7	07	Clock control 2	SMPLR										Audio data sample rate indication (48kHz default). Sets up scaling for internal filter coefficients, but does not affect in any way the actual device sample rate. Should be set to value most closely matching the actual sample rate determined by 256fs internal node. 000 = 48kHz 001 = 32kHz 010 = 24kHz 011 = 16kHz 100 = 12kHz 101 = 8kHz 110 = reserved 111 = reserved
			SCLKEN										Slow timer clock enable. Starts internal timer clock derived by dividing master clock. 0 = disabled 1 = enabled
			Default >>	0	0	0	0	0	0	0	0	0	0x000 reset value
													Reserved
			GPIO1PLL										Clock divisor applied to PLL clock for output from a GPIO pin 00 = divide by 1 01 = divide by 2 10 = divide by 3 11 = divide by 4
			GPIO1PL										GPIO1 polarity inversion control 0 = normal logic sense of GPIO signal 1 = inverted logic sense of GPIO signal
8	08	GPIO	GPIO1SEL										CSB/GPIO1 function select (input default) 000 = use as input subject to MODE pin#18 input logic level 001 = reserved 010 = Temperature OK status output (logic 0 = thermal shutdown) 011 = Reserved 100 = output divided PLL clock 101 = PLL locked condition (logic 1 = PLL locked) 110 = output set to logic 1 condition 111 = output set to logic 0 condition
			Default >>	0	0	0	0	0	0	0	0	0	0x000 reset value
			JCKMIDEN										Automatically enable internal bias amplifiers on jack detection state as sensed through GPIO pin associated to jack detection function Bit 7 = logic 1: enable bias amplifiers on jack at logic 0 level Bit 8 = logic 1: enable bias amplifiers on jack at logic 1 level
			JACDEN										Jack detection feature enable 0 = disabled 1 = enable jack detection associated functionality
9	09	Jack detect 1	JCKDIO										Select jack detect pin (GPIO1 default) 00 = GPIO1 is used for jack detection feature 01 = GPIO2 is used for jack detection feature 10 = GPIO3 is used for jack detection feature 11 = reserved
													Reserved
			Default >>	0	0	0	0	0	0	0	0	0	0x000 reset value
10	0A	Reserved											
11	0B	Reserved											
12	0C	Reserved											

Register		Function	Name	Bit								Description
Dec	Hex			8	7	6	5	4	3	2	1	0	
13	0D	Jack detect 2											Reserved
			JCKDOEN1										Outputs drivers that are automatically enabled whenever the designated jack detection input is in the logic = 1 condition, and the jack detection feature is enabled Bit 4 = 0: no change to Left and Right Line Output drivers Bit 4 = 1: enable Left and Right Line Output drivers
													Reserved
			JCKDOEN0										Outputs drivers that are automatically enabled whenever the designated jack detection input is in the logic = 0 condition, and the jack detection feature is enabled Bit 0 = 1: enable Left and Right Line Output drivers Bit 1 = 1: no change to Left and Right Line Output drivers
			Default >>	0	0	0	0	0	0	0	0	0	0x000 reset value
14	0E	ADC control	HPFEN										High pass filter enable control for filter of ADC output data stream 0 = high pass filter disabled 1 = high pass filter enabled
			HPFAM										High pass filter mode selection 0 = normal audio mode, 1st order 3.7Hz high pass filter for DC blocking 1 = application specific mode, variable 2nd order high pass filter
			HPF										Application specific mode cutoff frequency selection <See text and table for detailed description>
			ADCOS										ADC oversampling rate selection (64X default) 0 = 64x oversampling rate for reduced power 1 = 128x oversampling for better SNR
													Reserved
			RADCPL										ADC right channel polarity control 0 = normal polarity 1 = sign of RADC output is inverted from normal polarity
			LADCPL										ADC left channel polarity control 0 = normal polarity 1 = sign of LADC output is inverted from normal polarity
			Default >>	1	0	0	0	0	0	0	0	0	0x100 reset value
15	0F	Left ADC volume	LADCVU										ADC volume update bit feature. Write-only bit for synchronized L/R ADC changes If logic = 0 on R15 write, new R15 value stored in temporary register If logic = 1 on R15 write, new R15 and pending R16 values become active
			LADCGAIN										ADC right digital volume control (0dB default attenuation value). Expressed as an attenuation value in 0.5dB steps as follows: 0000 0000 = digital mute condition 0000 0001 = -127.0dB (highly attenuated) 0000 0010 = -126.5dB attenuation - all intermediate 0.5 step values through maximum volume – 1111 1110 = -0.5dB attenuation 1111 1111 = 0.0dB attenuation (no attenuation)
			Default >>	0	1	1	1	1	1	1	1	1	0x0FF reset value
16	10	Right ADC volume	RADCVU										ADC volume update bit feature. Write-only bit for synchronized L/R ADC changes If logic = 0 on R16 write, new R16 value stored in temporary register If logic = 1 on R16 write, new R16 and pending R15 values become active
			RADCGAIN										ADC left digital volume control (0dB default attenuation value). Expressed as an attenuation value in 0.5dB steps as follows: 0000 0000 = digital mute condition 0000 0001 = -127.0dB (highly attenuated) 0000 0010 = -126.5dB attenuation - all intermediate 0.5 step values through maximum volume – 1111 1110 = -0.5dB attenuation 1111 1111 = 0.0dB attenuation (no attenuation)
			Default >>	0	1	1	1	1	1	1	1	1	0x0FF reset value

Register		Function	Name	Bit								Description
Dec	Hex			8	7	6	5	4	3	2	1	0	
17	11	Reserved											
18	12	EQ1 low cutoff	EQM										Equalizer and 3D audio processing block assignment. 0 = block operates on digital stream from ADC 1 = block operates on digital stream to DAC (default on reset)
													Reserved
			EQ1CF										Equalizer band 1 low pass -3dB cut-off frequency selection 00 = 80Hz 01 = 105Hz (default) 10 = 135Hz 11 = 175Hz
			EQ1GC										EQ Band 1 digital gain control. Expressed as a gain or attenuation in 1dB steps 01100 = 0.0dB default unity gain value 00000 = +12dB 00001 = +11dB - all intermediate 1.0dB step values through minimum gain – 11000 = -12dB 11001 and larger values are reserved
			Default >>	1	0	0	1	0	1	1	0	0	0x12C reset value
19	13	EQ2 – peak 1	EQ2BW										Equalizer Band 2 bandwidth selection 0 = narrow band characteristic (default) 1 = wide band characteristic
													Reserved
			EQ2CF										Equalizer Band 2 center frequency selection 00 = 230Hz 01 = 300Hz (default) 10 = 385Hz 11 = 500Hz
			EQ2GC										EQ Band 2 digital gain control. Expressed as a gain or attenuation in 1dB steps 01100 = 0.0dB default unity gain value 00000 = +12dB 00001 = +11dB - all intermediate 1.0dB step values through minimum gain – 11000 = -12dB 11001 and larger values are reserved
			Default >>	0	0	0	1	0	1	1	0	0	0x02C reset value
20	14	EQ3 – peak 2	EQ3BW										Equalizer Band 3 bandwidth selection 0 = narrow band characteristic (default) 1 = wide band characteristic
													Reserved
			EQ3CF										Equalizer Band 3 center frequency selection 00 = 650Hz 01 = 850Hz (default) 10 = 1.1kHz 11 = 1.4kHz

Register		Function	Name	Bit								Description
Dec	Hex			8	7	6	5	4	3	2	1 0	
			EQ3GC									EQ Band 3 digital gain control. Expressed as a gain or attenuation in 1dB steps 01100 = 0.0dB default unity gain value 00000 = +12dB 00001 = +11dB - all intermediate 1.0dB step values through minimum gain – 11000 = -12dB 11001 and larger values are reserved
			Default >>	0	0	0	1	0	1	1	0 0	0x02C reset value
21	15	EQ4 – peak 3	EQ4BW									Equalizer Band 4 bandwidth selection 0 = narrow band characteristic (default) 1 = wide band characteristic
												Reserved
			EQ4CF									Equalizer Band 4 center frequency selection 00 = 1.8kHz 01 = 2.4kHz (default) 10 = 3.2kHz 11 = 4.1kHz
			EQ4GC									EQ Band 4 digital gain control. Expressed as a gain or attenuation in 1dB steps 01100 = 0.0dB default unity gain value 00000 = +12dB 00001 = +11dB - all intermediate 1.0dB step values through minimum gain – 11000 = -12dB 11001 and larger values are reserved
			Default >>	0	0	0	1	0	1	1	0 0	0x02C reset value
22	16	EQ5 – high cutoff										Reserved
			EQ5CF									Equalizer Band 5 high pass -3dB cut-off frequency selection 00 = 5.3kHz 01 = 6.9kHz (default) 10 = 9.0kHz 11 = 11.7kHz
			EQ5GC									EQ Band 5 digital gain control. Expressed as a gain or attenuation in 1dB steps 01100 = 0.0dB default unity gain value 00000 = +12dB 00001 = +11dB - all intermediate 1.0dB step values through minimum gain – 11000 = -12dB 11001 and larger values are reserved
			Default >>	0	0	0	1	0	1	1	0 0	0x02C reset value
23	17	Reserved										
24	18	Reserved										
25	19	Reserved										
26	1A	Reserved										

Register		Function	Name	Bit								Description
Dec	Hex			8	7	6	5	4	3	2	1	0	
27	1B	Notch filter 1	NFCU1										Update bit feature for simultaneous change of all notch filter parameters. Write-only bit. Logic 1 on R27 register write operation causes new R27 value and any pending value in R28, R29, or R30 to go into effect. Logic 0 on R27 register write causes new value to be pending an update bit event on R27, R28, R29, or R30.
			NFCEN										Notch filter control bit 0 = disabled 1 = enabled
			NFCA0[13:7]										Notch filter A0 coefficient most significant bits. See text and table for details.
			Default >>	0	0	0	0	0	0	0	0	0	0x000 reset value
28	1C	Notch filter 2	NFCU2										Update bit feature for simultaneous change of all notch filter parameters. Write-only bit. Logic 1 on R28 register write operation causes new R28 value and any pending value in R27, R29, or R30 to go into effect. Logic 0 on R28 register write causes new value to be pending an update bit event on R27, R28, R29, or R30.
													Reserved
			NFCAO[6:0]										Notch filter A0 coefficient least significant bits. See text and table for details.
			Default >>	0	0	0	0	0	0	0	0	0	0x000 reset value
29	1D	Notch filter 3	NFCU3										Update bit feature for simultaneous change of all notch filter parameters. Write-only bit. Logic 1 on R29 register write operation causes new R29 value and any pending value in R27, R28, or R30 to go into effect. Logic 0 on R29 register write causes new value to be pending an update bit event on R27, R28, R29, or R30.
													Reserved
			NFCA1[13:7]										Notch filter A1 coefficient most significant bits. See text and table for details.
			Default >>	0	0	0	0	0	0	0	0	0	0x000 reset value
30	1E	Notch filter 4	NFCU4										Update bit feature for simultaneous change of all notch filter parameters. Write-only bit. Logic 1 on R30 register write operation causes new R30 value and any pending value in R27, R28, or R29 to go into effect. Logic 0 on R30 register write causes new value to be pending an update bit event on R27, R28, R29, or R30.
													Reserved
			NFCA1[6:0]										Notch filter A1 coefficient least significant bits. See text and table for details.
			Default >>	0	0	0	0	0	0	0	0	0	0x000 reset value
31	1F	Reserved											
32	20	ALC control 1	ALCEN										Automatic Level Control function control bits 00 = right and left ALCs disabled 01 = only right channel ALC enabled 10 = only left channel ALC enabled 11 = both right and left channel ALCs enabled
													reserved
			ALCMXGAIN										Set maximum gain limit for PGA volume setting changes under ALC control 111 = +35.25dB (default) 110 = +29.25dB 101 = +23.25dB 100 = +17.25dB 011 = +11.25dB 010 = +5.25dB 001 = -0.75dB 000 = -6.75dB
			ALCMNGAIN										Set minimum gain value limit for PGA volume setting changes under ALC control 000 = -12dB (default) 001 = -6.0dB 010 = 0.0dB 011 = +6.0dB 100 = +12dB 101 = +18dB 110 = +24dB 111 = +30dB
			Default >>	0	0	0	1	1	1	0	0	0	0x038 reset value
33	21												Reserved

Register		Function	Name	Bit								Description
Dec	Hex			8	7	6	5	4	3	2	1	0	
		ALC control 2	ALCHT										Hold time before ALC automated gain increase 0000 = 0.00ms (default) 0001 = 2.00ms 0010 = 4.00ms - time value doubles with each bit value increment – 1001 = 512ms 1010 through 1111 = 1000ms
			ALCSL										ALC target level at ADC output 1111 = -1.5dB below full scale (FS) 1110 = -1.5dB FS (same value as 1111) 1101 = -3.0dB FS 1100 = -4.5dB FS 1011 = -6.0dB FS (default) - target level varies 1.5dB per binary step throughout control range – 0001 = -21.0dB FS 0000 = -22.5dB FS (lowest possible target signal level)
			Default >>	0	0	0	0	0	1	0	1	1	0x00B reset value
34	22	ALC control 3	ALCM										ALC mode control setting 0 = normal ALC operation 1 = Limiter Mode operation
			ALCDCY										ALC decay time duration per step of gain change for gain increase of 0.75dB of PGA gain. Total response time can be estimated by the total number of steps necessary to compensate for a given magnitude change in the signal. For example, a 6dB decrease in the signal would require eight ALC steps to compensate. Step size for each mode is given by: Normal Mode Limiter Mode 0000 = 500us 0000 = 125us 0001 = 1.0ms 0001 = 250us 0010 = 2.0ms (default) 0010 = 500us (default) ------- time value doubles with each binary bit value -------- 1000 = 128ms 1000 = 32ms 1001 = 256ms 1001 = 64ms 1010 through 1111 = 512ms 1010 through 1111 = 128ms
			ALCATK										ALC attack time duration per step of gain change for gain decrease of 0.75dB of PGA gain. Total response time can be estimated by the total number of steps necessary to compensate for a given magnitude change in the signal. For example, a 6dB increase in the signal would require eight ALC steps to compensate. Step size for each mode is given by: Normal Mode Limiter Mode 0000 = 125us 0000 = 31us 0001 = 250us 0001 = 62us 0010 = 500us (default) 0010 = 124us (default) ------- time value doubles with each binary bit value -------- 1000 = 26.5ms 1000 = 7.95ms 1001 = 53.0ms 1001 = 15.9ms 1010 through 1111 = 128ms 1010 through 1111 = 31.7ms
			Default >>	0	0	0	1	1	0	0	1	0	0x032 reset value
35	23	Noise gate	Reserved										Reserved

Register		Function	Name	Bit								Description
Dec	Hex			8	7	6	5	4	3	2	1	0	
			ALCNEN										ALC noise gate function control bit 0 = disabled 1 = enabled
			ALCNTH										ALC noise gate threshold level 000 = -39dB (default) 001 = -45dB 010 = -51dB 011 = -57dB 100 = -63dB 101 = -69dB 110 = -75dB 111 = -81dB
			Default >>	0	0	0	0	1	0	0	0	0	0x010 reset value
36	24	PLL N											Reserved
			PLLMCLK										Control bit for divide by 2 pre-scale of MCLK path to PLL clock input 0 = MCLK divide by 1 (default) 1 = MCLK divide by 2
			PLLN										Integer portion of PLL input/output frequency ratio divider. Decimal value should be constrained to 6, 7, 8, 9, 10, 11, or 12. Default decimal value is 8. See text for details.
			Default >>	0	0	0	0	0	1	0	0	0	0x008 reset value
37	25	PLL K 1											Reserved
			PLLK[23:18]										High order bits of fractional portion of PLL input/output frequency ratio divider. See text for details.
			Default >>	0	0	0	0	0	1	1	0	0	0x00C reset value
38	26	PLL K 2	PLLK[17:9]										Middle order bits of fractional portion of PLL input/output frequency ratio divider. See text for details.
			Default >>	0	1	0	0	1	0	0	1	1	0x093 reset value
39	27	PLL K 3	PLLK{8:0}										Low order bits of fractional portion of PLL input/output frequency ratio divider. See text for details.
			Default >>	0	1	1	1	0	1	0	0	1	0x0E9 reset value
40	28	Reserved											Reserved

41	29	3D control											Reserved
			3DDEPTH										3D Stereo Enhancement effect depth control 0000 = 0.0% effect (disabled, default) 0001 = 6.67% effect 0010 = 13.3% effect - effect depth varies by 6.67% per binary bit value – 1110 = 93.3% effect 1111 = 100% effect (maximum effect)
			Default >>	0	0	0	0	0	0	0	0	0	0x000 reset value
42	2A	Reserved											
43	2B	Reserved											
44	2C	Input control	MICBIASV										Microphone bias voltage selection control. Values change slightly with R40 MISBIAS mode selection control. Open circuit voltage on MICBIAS pin#32 is shown as follows as a fraction of the VDDA pin#31 supply voltage. Normal Mode Low Noise Mode 00 = 0.9x 00 = 0.85x 01 = 0.65x 01 = 0.60x 10 = 0.75x 10 = 0.70x 11 = 0.50x 11 = 0.50x
			RLINRPGA										RLIN right line input path control to right PGA positive input 0 = RLIN not connected to PGA positive input (default) 1 = RLIN connected to PGA positive input
			RMICNRPGA										RMICN right microphone negative input to right PGA negative input path control 0 = RMICN not connected to PGA negative input (default) 1 = RMICN connected to PGA negative input

Register		Function	Name	Bit								Description
Dec	Hex			8	7	6	5	4	3	2	1	0	
			RMICPRPGA										RMICP right microphone positive input to right PGA positive input enable 0 = RMICP not connected to PGA positive input (default) 1 = RMICP connected to PGA positive input
													Reserved
			LLINLPGA										LLIN right line input path control to left PGA positive input 0 = LLIN not connected to PGA positive input (default) 1 = LLIN connected to PGA positive input
			LMICNLPGA										LMICN left microphone negative input to left PGA negative input path control 0 = LMICN not connected to PGA negative input (default) 1 = LMICN connected to PGA negative input
			LMICPLPGA										LMICP left microphone positive input to left PGA positive input enable 0 = LMICP not connected to PGA positive input (default) 1 = LMICP connected to PGA positive input
			Default >>	0	0	0	1	1	0	0	1	1	0x033 reset value
45	2D	**Left input PGA gain**	LPGAU										PGA volume update bit feature. Write-only bit for synchronized L/R PGA changes If logic = 0 on R45 write, new R45 value stored in temporary register If logic = 1 on R45 write, new R45 and pending R46 values become active
			LPGAZC										Left channel input zero cross detection enable 0 = gain changes to PGA register happen immediately (default) 1 = gain changes to PGA happen pending zero crossing logic
			LPGAMT										Left channel mute PGA mute control 0 = PGA not muted, normal operation (default) 1 = PGA in muted condition not connected to LADC Mix/Boost stage
			LPGAGAIN										Left channel input PGA volume control setting. Setting becomes active when allowed by zero crossing and/or update bit features. 01 0000 = 0.0dB default setting 00 0000 = -12dB 00 0001 = -11.25dB - volume changes in 0.75dB steps per binary bit value – 11 1110 = +34.50dB 11 1111 = +35.25dB
			Default >>	0	0	0	0	1	0	0	0	0	0x010 reset value
			RPGAU										PGA volume update bit feature. Write-only bit for synchronized L/R PGA changes If logic = 0 on R46 write, new R46 value stored in temporary register If logic = 1 on R46 write, new R46 and pending R45 values become active
			RPGAZC										Right channel input zero cross detection enable 0 = gain changes to PGA register happen immediately 1 = gain changes to PGA happen pending zero crossing logic
			RPGAMT										Right channel mute PGA mute control 0 = PGA not muted, normal operation (default) 1 = PGA in muted condition not connected to RADC Mix/Boost stage
46	2E	**Right input PGA gain**	RPGAGAIN										Right channel input PGA volume control setting. Setting becomes active when allowed by zero crossing and/or update bit features. 01 0000 = 0.0dB default setting 00 0000 = -12dB 00 0001 = -11.25dB - volume changes in 0.75dB steps per binary bit value – 11 1110 = +34.50dB 11 1111 = +35.25dB
			Default >>	0	0	0	0	1	0	0	0	0	0x010 reset value
47	2F	**Left ADC boost**	LPGABST										Left channel PGA boost control 0 = no gain between PGA output and LPGA Mix/Boost stage input 1 = +20dB gain between PGA output and LPGA Mix/Boost stage input

Register		Function	Name	Bit								Description
Dec	Hex			8	7	6	5	4	3	2	1	0	
													Reserved
			LPGABSTGAIN										Gain value between LLIN line input and LPGA Mix/Boost stage input 000 = path disconnected (default) 001 = -12dB 010 = -9.0dB 011 = -6.0dB 100 = -3.0dB 101 = 0.0dB 110 = +3.0dB 111 = +6.0dB
													Reserved
			Default >>	1	0	0	0	0	0	0	0	0	0x100 reset value
48	30	Right ADC boost	RPGABST										Right channel PGA boost control 0 = no gain between PGA output and RPGA Mix/Boost stage input 1 = +20dB gain between PGA output and RPGA Mix/Boost stage input
													Reserved
			RPGABSTGAIN										Gain value between RLIN line input and RPGA Mix/Boost stage input 000 = path disconnected (default) 001 = -12dB 010 = -9.0dB 011 = -6.0dB 100 = -3.0dB 101 = 0.0dB 110 = +3.0dB 111 = +6.0dB
													Reserved
			Default >>	1	0	0	0	0	0	0	0	0	0x100 reset value
49	31	Output control											Reserved
			TSEN										Thermal shutdown enable protects chip from thermal destruction on overload 0 = disable thermal shutdown (engineering purposes, only) 1 = enable (default) strongly recommended for normal operation
			AOUTIMP										Output resistance control option for tie-off of unused or disabled outputs. Unused outputs tie to internal voltage reference for reduced pops and clicks. 0 = nominal tie-off impedance value of 1kΩ (default) 1 = nominal tie-off impedance value of 30kΩ
			Default >>	0	0	0	0	0	0	0	1	0	0x002 reset value
50	32	Left mixer											Reserved
			LBYPCTRL										Configure bypass path from LADC Mix/Boost output to LMAIN left output mixer. 00001 = path not connected 10110 = path connected
			Default >>	0	0	0	0	0	0	0	0	1	0x001 reset value
51	33	Right mixer											Reserved
			RBYPCTRL										Configure bypass path from RADC Mix/Boost output to LMAIN left output mixer. 00001 = path not connected 10110 = path connected
			Default >>	0	0	0	0	0	0	0	0	1	0x001 reset value
52	34	Left LineOut Volume	LOUTVU										Line output volume update bit feature. Write-only bit for synchronized changes of left and right line output amplifier output settings If logic = 0 on R52 write, new R52 value stored in temporary register If logic = 1 on R52 write, new R52 and pending R53 values become active
			LOUTZC										Left channel input zero cross detection enable 0 = gain changes to left line output happen immediately (default) 1 = gain changes to left line output happen pending zero crossing logic
			LOUTMUT										Left line output mute control 0 = line output not muted, normal operation (default) 1 = line in muted condition

Register		Function	Name	Bit								Description
Dec	Hex			8	7	6	5	4	3	2	1	0	
			LOUTVOL										Left line output output volume control setting. Setting becomes active when allowed by zero crossing and/or update bit features. 11 1001 = 0.0dB default setting 00 0000 = -57dB 00 0001 = -56dB - volume changes in 1.0dB steps per binary bit value – 11 1110 = +5.0dB 11 1111 = +6.0dB
			Default >>	0	0	0	1	1	1	0	0	1	0x039 reset value
53	35	**Right Line Out Volume**	ROUTVU										Line output volume update bit feature. Write-only bit for synchronized changes of left and right line output amplifier output settings If logic = 0 on R53 write, new R53 value stored in temporary register If logic = 1 on R53 write, new R53 and pending R52 values become active
			ROUTZC										Right channel input zero cross detection enable 0 = gain changes to right line output happen immediately (default) 1 = gain changes to right line output happen pending zero crossing logic
			ROUTMUT										Right line output mute control 0 = output not muted, normal operation (default) 1 = output in muted condition
			ROUTVOL										Right line output output volume control setting. Setting becomes active when allowed by zero crossing and/or update bit features. 11 1001 = 0.0dB default setting 00 0000 = -57dB 00 0001 = -56dB - volume changes in 1.0dB steps per binary bit value – 11 1110 = +5.0dB 11 1111 = +6.0dB
			Default >>	0	0	0	1	1	1	0	0	1	0x039 reset value
54	**36**	**Reserved**											
55	**37**	**Reserved**											
56	**38**	**Reserved**											
57	**39**	**Reserved**											
58	**3A**	**Power Management 4**											Reserved
			LPIPBST										Reduce ADC Mix/Boost amplifier supply current 50% in low power operating mode 0 = normal supply current operation (default) 1 = 50% reduced supply current mode
			LPADC										Reduce ADC supply current 50% in low power operating mode 0 = normal supply current operation (default) 1 = 50% reduced supply current mode
													Reserved
			MICBIASM										Microphone bias optional low noise mode configuration control 0 = normal configuration with low-Z micbias output impedance 1 = low noise configuration with 200-ohm micbias output impedance

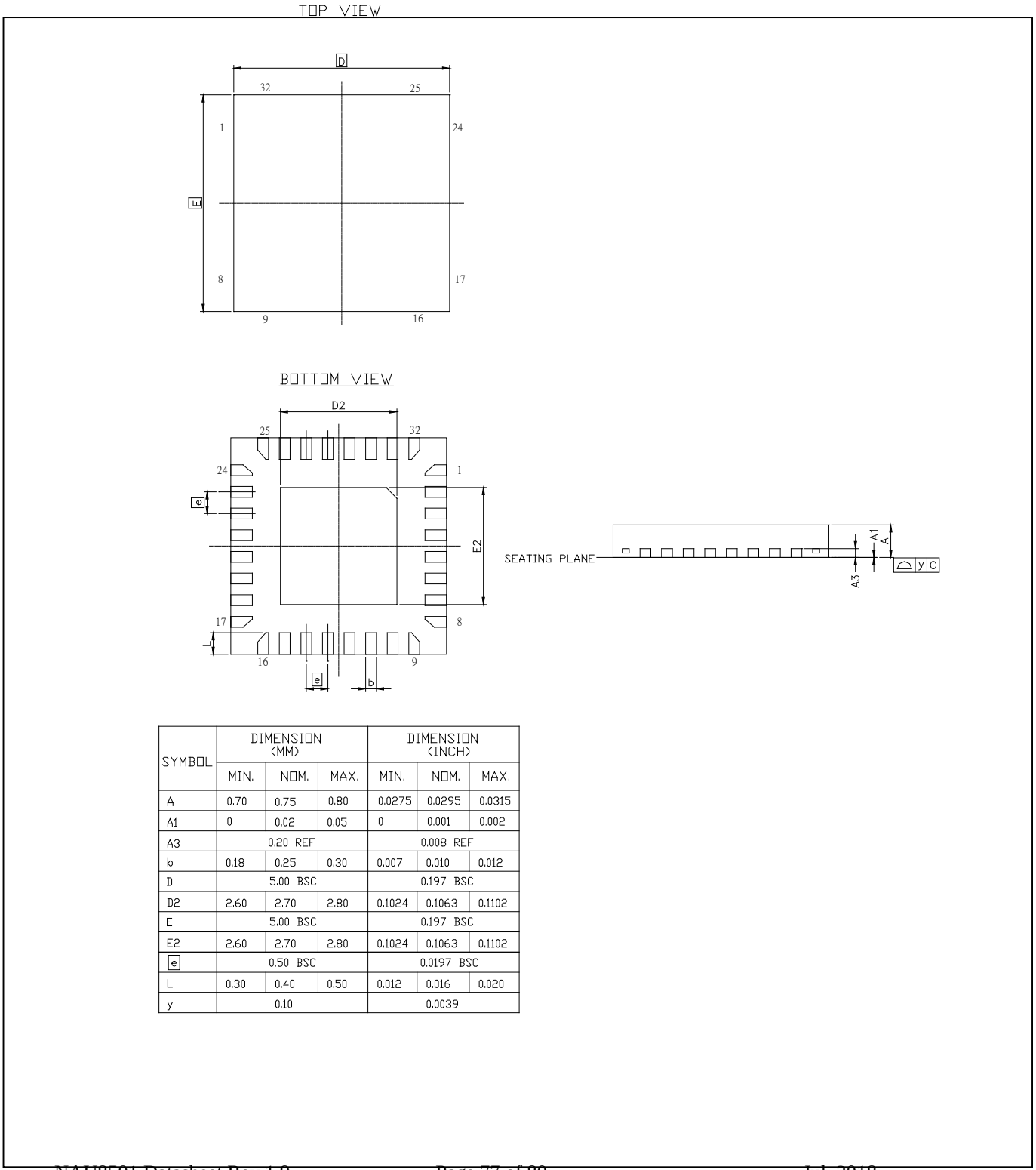
Register		Function	Name	Bit								Description
Dec	Hex			8	7	6	5	4	3	2	1	0	
			REGVOLT										Regulator voltage control power reduction options 00 = normal 1.80Vdc operation (default) 01 = 1.61Vdc operation 10 = 1.40 Vdc operation 11 = 1.218 Vdc operation
			IBADJ										Master bias current power reduction options 00 = normal operation (default) 01 = 25% reduced bias current from default 10 = 14% reduced bias current from default 11 = 25% reduced bias current from default
			Default >>	0	0	0	0	0	0	0	0	0	0x000 reset value
59	3B	Left time slot	LTSLOT[8:0]										Left channel PCM time slot start count: LSB portion of total number of bit times to wait from frame sync before clocking audio channel data. LSB portion is combined with MSB from R60 to get total number of bit times to wait.
			Default >>	0	0	0	0	0	0	0	0	0	0x000 reset value
60	3C	Misc.	PCMTSEN										Time slot function enable for PCM mode.
			TRI										Tri state ADC out after second half of LSB enable
			PCM8BIT										8-bit word length enable
			PUDEN										ADCOUT output driver 1 = enabled (default) 0 = disabled (driver in high-z state)
			PUDPE										ADCOUT passive resistor pull-up or passive pull-down enable 0 = no passive pull-up or pull-down on ADCOUT pin 1 = passive pull-up resistor on ADCOUT pin if PUDPS = 1 1 = passive pull-down resistor on ADCOUT pin if PUDPS = 0
			PUDPS										ADCOUT passive resistor pull-up or pull-down selection 0 = passive pull-down resistor applied to ADCOUT pin if PUDPE = 1 1 = passive pull-down resistor applied to ADCOUT pin if PUDPE = 1
													Reserved
			RTSLOT[9]										Right channel PCM time slot start count: MSB portion of total number of bit times to wait from frame sync before clocking audio channel data. MSB is combined with LSB portion from R61 to get total number of bit times to wait.
			LTSLOT[9]										Left channel PCM time slot start count: MSB portion of total number of bit times to wait from frame sync before clocking audio channel data. MSB is combined with LSB portion from R59 to get total number of bit times to wait.
			Default >>	0	0	0	1	0	0	0	0	0	0x020 reset value
61	3D	Right time slot	RTSLOT[8:0]										Right channel PCM time slot start count: LSB portion of total number of bit times to wait from frame sync before clocking audio channel data. LSB portion is combined with MSB from R60 to get total number of bit times to wait.
			Default >>	0	0	0	0	0	0	0	0	0	0x000 reset value
62	3E	Device Revision Number											Reserved
			REV										Device Revision Number for readback over control interface = read-only value
			Default >>	0	0	1	1	1	1	1	0	1	0x0FD for RevC silicon
63	3F	Device ID#		0	0	0	0	1	1	0	1	0	0x01A Device ID equivalent to control bus address = read-only value

14 Appendix D: Register Overview

DEC	HEX	NAME	Bit 8	Bit 7	Bit 6	Bit5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
0	00	Software Reset	RESET (SOFTWARE)									
1	01	Power Management 1	Reserved			PLLEN	MICBIASEN	ABIASEN	IOBUFEN	REFIMP		000
2	02	Power Management 2	RLINEN	LLINEN	SLEEP	RBSTEN	LBSTEN	RPGAEN	LPGAEN	RADCEN	LADCEN	000
3	03	Power Management 3	Reserved					RBYPEN	LBYPEN	Reserved		
General Audio Controls												
4	04	Audio Interface	BCLKP	LRP	WLEN		AIFMT		Reserved	ADCPHS	MONO	050
5	05	Companding	Reserved			CMB8	Reserved		ADCCM		Reserved	000
6	06	Clock Control 1	CLKM	MCLKSEL			BCLKSEL			Reserved	CLKIOEN	140
7	07	Clock Control 2	4WSPIEN	Reserved				SMPLR			SCLKEN	000
8	08	GPIO	Reserved			GPIO1PLL		GPIO1PL	GPIO1SEL			000
9	09	Jack Detect 1	JCKMIDEN		JCKDEN	JCKDIO		Reserved				000
10	0A	Reserved	Reserved									000
11	0B	Reserved	Reserved									0FF
12	0C	Reserved	Reserved									0FF
13	0D	Jack Detect 2	Reserved	JCKDOEN1				JCKDOEN0				000
14	0E	ADC Control	HPFEN	HPFAM	HPF			ADCOS	Reserved	RADCPL	LADCPL	100
15	F	Left ADC Volume	LADCVU	LADCGAIN								0FF
16	10	Right ADC Volume	RADCVU	RADCGAIN								0FF
17	11	Reserved										
Equalizer												
18	12	EQ1-low cutoff	EQM	Reserved	EQ1CF		EQ1GC					12C
19	13	EQ2-peak 1	EQ2BW	Reserved	EQ2CF		EQ2GC					02C
20	14	EQ3-peak 2	EQ3BW	Reserved	EQ3CF		EQ3GC					02C
21	15	EQ4-peak3	EQ4BW	Reserved	EQ4CF		EQ4GC					02C
22	16	EQ5-high cutoff	Reserved		EQ5CF		EQ5GC					02C
23	17	Reserved										
Notch Filter												
27	1B	Notch Filter 1	NFCU1	NFCEN	NFCA0[13:7]							000
28	1C	Notch Filter 2	NFCU2	Reserved	NFCA0[6:0]							000
29	1D	Notch Filter 3	NFCU3	Reserved	NFCA1[13:7]							000
30	1E	Notch Filter 4	NFCU4	Reserved	NFCA1[6:0]							000
31	1F	Reserved										
ALC and Noise Gate Control												
32	20	ALC Control 1	ALCEN		Reserved	ALCMXGAIN		ALCMNGAIN				038
33	21	ALC Control 2	Reserved	ALCHT				ALCSL				00B
34	22	ALC Control 3	ALCM	ALCDCY				ALCATK				032
35	23	Noise Gate	Reserved				ALCTBLSEL	ALCNEN	ALCNTH			010
Phase Locked Loop												
36	24	PLL N	Reserved				PLLMCLK	PLLN				008
37	25	PLL K 1	Reserved			PLLK[23:18]						00C
38	26	PLL K 2	PLLK[17:9]									093
39	27	PLL K 3	PLLK[8:0]									0E9
40	28	Mic Bias Mode	Reserved								MICBIASM	000
Miscellaneous												
41	29	3D control	Reserved					3DDEPTH				000
42	2A	Reserved										
43	2B	Reserved										
44	2C	Input Control	MICBIASV		RLINRPGA	RMICNRPGA	RMICPRPGA	Reserved	LLINLPGA	LMICNLPGA	LMICPLPGA	033
45	2D	Left Input PGA Gain	LPGAU	LPGAZC	LPGAMT	LPGAGAIN						010
46	2E	Right Input PGA Gain	RPGAU	RPGAZC	RPGAMT	RPGAGAIN						010
47	2F	Left ADC Boost	LPGABST	Reserved	LPGABSTGAIN			Reserved				100
48	30	Right ADC Boost	RPGABST	Reserved	RPGABSTGAIN			Reserved				100
49	31	Output Control	Reserved							TSEN	AOUTIMP	002
50	32	Left Bypass Control	Reserved				LBYPCTRL					001
51	33	Right Bypass Control	Reserved				RBYPCTRL					001
52	34	L Line Out Volume	LOUTVU	LOUTZC	LOUTMUT	LOUTVOL						039
53	35	R Line Out Volume	ROUTVU	ROUTZC	ROUTMUT	ROUTVOL						039
54	36	Reserved										
55	37	Reserved										
56	38	Reserved										
57	39	Reserved										
58	3A	Power Management 4	Reserved	LPIPBST	LPADC	Reserved	MICBIASM	REGVOLT		IBADJ		000
PCM Time Slot and ADCOUT Impedance Option Control												
59	3B	Left Time Slot	LTSLOT[8:0]									000
60	3C	Misc	PCMTSEN	TRI	PCM8BIT	PUDEN	PUDPE	PUDPS	Reserved	RTSLOT[9]	LTSLOT[9]	020
61	3D	Right Time Slot	RTSLOT[8:0]									000
Silicon Revision and Device ID												
62	3E	Device Revision #	Reserved	REV-C								0FD
63	3F	Device ID	ID									01A

15 Package Dimensions

32-lead plastic QFN 32L; 5X5mm^2, 0.8mm thickness, 0.5mm lead pitch



SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0275	0.0295	0.0315
A1	0	0.02	0.05	0	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D	5.00 BSC			0.197 BSC		
D2	2.60	2.70	2.80	0.1024	0.1063	0.1102
E	5.00 BSC			0.197 BSC		
E2	2.60	2.70	2.80	0.1024	0.1063	0.1102
e	0.50 BSC			0.0197 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
y	0.10			0.0039		

16 Ordering Information

Part Number	Dimension	Package	Package Material
NAU8501YG	4x4 mm	QFN-32	Green

NAU8501 _ _

Package Material:

G = Pb-free Package

Package Type:

Y = 32-Pin QFN Package

REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
0.6	July 29, 2009	n/a	Draft Release
1.0	Nov. 07, 2009	n/a	Draft Release
1.1	June 30, 2010	n/a	First Release
1.2	July 20, 2010	n/a	Major revision and update
1.3	July 22, 2010	All	Change name to “data sheet”
1.4	October, 2013	48 6	Corrected 2 wire interface timing diagram Corrected Digital I/O voltage levels from DCVDD to DBVDD
1.5	Feb, 2014	5, 6, 38, 39, 49, 50	Replaced VDDSPK by VDDA2 Replaced AVDD by VDDA Modified application diagram Modified Figure 17 (Byte Write Sequence) Modified Figure 18 (2-Wire Read Sequence) Corrected rising/fall time specification of I2S
1.6	Nov. 2014	48	Corrected Tsdios setup time
1.7	Jan 2015	1	Updated AECQ100 description
1.8	March 2016	34	Revise f1 equation from * to /
1.9	July 2018	50	I2C filter

Table 22: Revision History

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.