Product/Process Change Notice - PCN 16_0028 Rev. A

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*** * * * * * * * ATTENTION: THIS PCN IS BEING CANCELLED! * * * * * * * ***

This notice is to inform you of a change that will be made to certain ADI products (see Appendix A) that you may have purchased in the last 2 years. **Any inquiries or requests with this PCN (additional data or samples) must be sent to ADI within 30 days of publication date.** ADI contact information is listed below.

Note: Revised fields are indicated by a red field name. See Appendix B for revision history.

PCN Title: AD9559 Die revision

Publication Date: 16-May-2016

Effectivity Date: Effective upon publication.

Revision Description:

A new problem has been identified that was introduced in the silicon revision. Because of this, we are cancelling this change.

Description Of Change

Circuitry has been added to improve functionality and fix 9 issues:
1. A reset on the RF Divider was added to ensure that the RF Divider always powers up in a known state.
2. The state machine that interfaces with the EEPROM was redesigned to ensure EEPROM data is properly loaded.
3. Synchronization circuitry was implemented that properly syncs the SDM on the correct phase of the internal clock on exit of power-down state.
4. The internal clock relationships were properly gated between the TDCs and System Clock in order to ensure proper DPLL startup.
5. The DPLL divider was limited to 23 bits in Frac/Mod (rather than 24-bits), so a register was modified to handle the sign-bit correctly.
6. VCO calibration fixes to prevent APLL calibration failure and enhance the accuracy of the calibration.
7. APLL VCO design changed to allow more margin over temp with less jitter variation.
8. Unintended connection between 1.8V and 3.3V supplies resulted in a current flow during power up. Logic changes and POR enhancements were added to address this.
9. APLL lock detector changed to avoid potential false "loss of lock" indication.

Reason For Change

Items 1-4: The RF Divider, EEPROM interface, SDM timing, and DPLL start-up were not functionally robust.
Item 5: In the case of the DPLL divider, the device was originally intended to have a 24-bit fractional divider.
Item 6: The APLL calibration fails in a very small number of cases on existing silicon, requiring the user to reissue a calibration.
Item 7: To enhance the robustness of the part over temperature and guarantee more consistent jitter performance.
Item 8: The feed through caused the other supply to hold a non-zero voltage when it should have been at ground. In one customer's case, this voltage was high enough to turn on the chip that was sharing the supply with the AD9559, disrupting the power supply sequencing for their board.
Item 9: Analysis of the APLL lock detector circuit revealed potential for declaration of false “unlock” events due to a metastable event.

Impact of the change (positive or negative) on fit, form, function & reliability

There is no change to either the fit or the form for all AD9559 applications.

For Item #1, In the rare cases where the user wishes to change the RF Divider setting without reissuing an APLL recalibration, the user should check Revision D of the AD9559 datasheet for details on how to do so. However, nearly all AD9559 applications will not require any modification to the device programming.

Functionality of the DPLL 24-bit fractional divider has been corrected to match the original design objective of the part.

Reliability of the RF Divider, EEPROM interface, SDM timing, and DPLL start-up has improved.

Product Identification *(this section will describe how to identify the changed material)*

Read-only Register 0x000A will have the value of 0x41.
Previous versions will have a value < 0x41 in Register 0x000A

Additionally, ADI will be able to differentiate by date code and lot number. the earliest date code for new material will be 1551, it is not yet known what the last date code for old material will be

Summary of Supporting Information

Qualification has been performed per Industry Standard Test Methods. See attached Qualification Results Summary.

Supporting Documents

Attachment 1: Type: Qualification Results Summary

ADI_PCN_16_0028_Rev_A_PCN Qualification Plan Summary of AD9559 Die Revision D Qualification.pdf

For questions on this PCN, please send an email to the regional contacts below or contact your local ADI sales representatives.					
Americas:	PCN_Americas@analog.com	**Europe:**	PCN_Europe@analog.com	**Japan:**	PCN_Japan@analog.com
				Rest of Asia:	PCN_ROA@analog.com

Appendix A - Affected ADI Models				
Existing Parts - Product Family / Model Number (4)				
AD9559 / AD80341BCPZ	AD9559 / AD80341BCPZ-REEL7	AD9559 / AD9559BCPZ	AD9559 / AD9559BCPZ-REEL7	

Appendix B - Revision History			
Rev	**Publish Date**	**Effectivity Date**	**Rev Description**
Rev. -	13-Apr-2016	12-Jul-2016	Initial Release
Rev. A	16-May-2016	16-May-2016	A new problem has been identified that was introduced in the silicon revision. Because of this, we are cancelling this change.